

Jet Propulsion Laboratory

**Commercial Off-The-Shelf
(COTS)**

**The Next Generation of
Electronic Parts for Space**

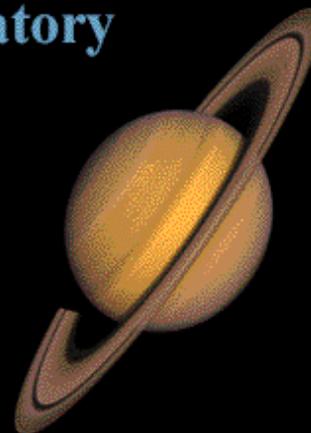
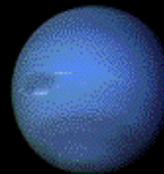
Mike Sandor

JPL



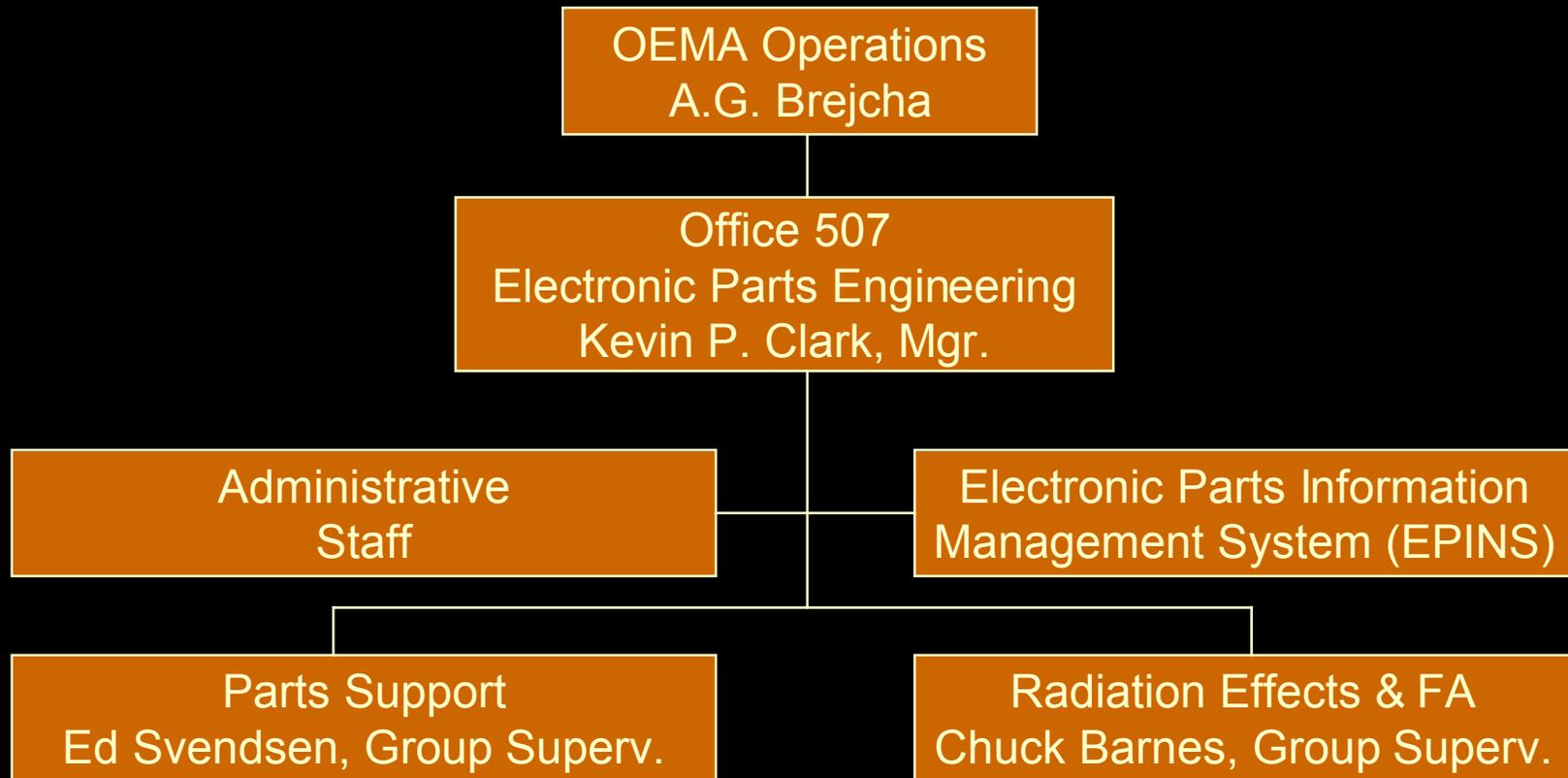
National Aeronautics and Space Administration
California Institute of Technology

Jet Propulsion Laboratory





Organization





Agenda

Introduction to COTS

Methodology/Evaluation for Risk Assessment

COTS Work Plan/Status

COTS Work (Examples)

Summary



The COTS Program

Develop a *methodology* to evaluate & select COTS that-

- Minimizes the cost of part risk management
- Uses an engineering-based approach vs “rule’ based
- Stimulates gaining new knowledge and experience
- Establishes a systematic approach to evaluation
- Uses Mfr. and other pre-existing data as much as possible
- Provides optimized evaluation & test path per part
- Allows trade-off assessment with high reliability parts
- Establishes COTS guidelines for Space Applications



The Meaning of COTS

- “Buy and Fly”
- “Procuring via catalog part number to QML-V standards”
- “Procurement is performed without formal specification”
- “The usage of any COTS equipment does not constitute any waiver to fundamental applicable requirements”

Our Interpretation:

- COTS are parts whose specification is manufacturer -controlled as opposed to traditional “Hi-Rel” parts whose specification was Government or customer-controlled



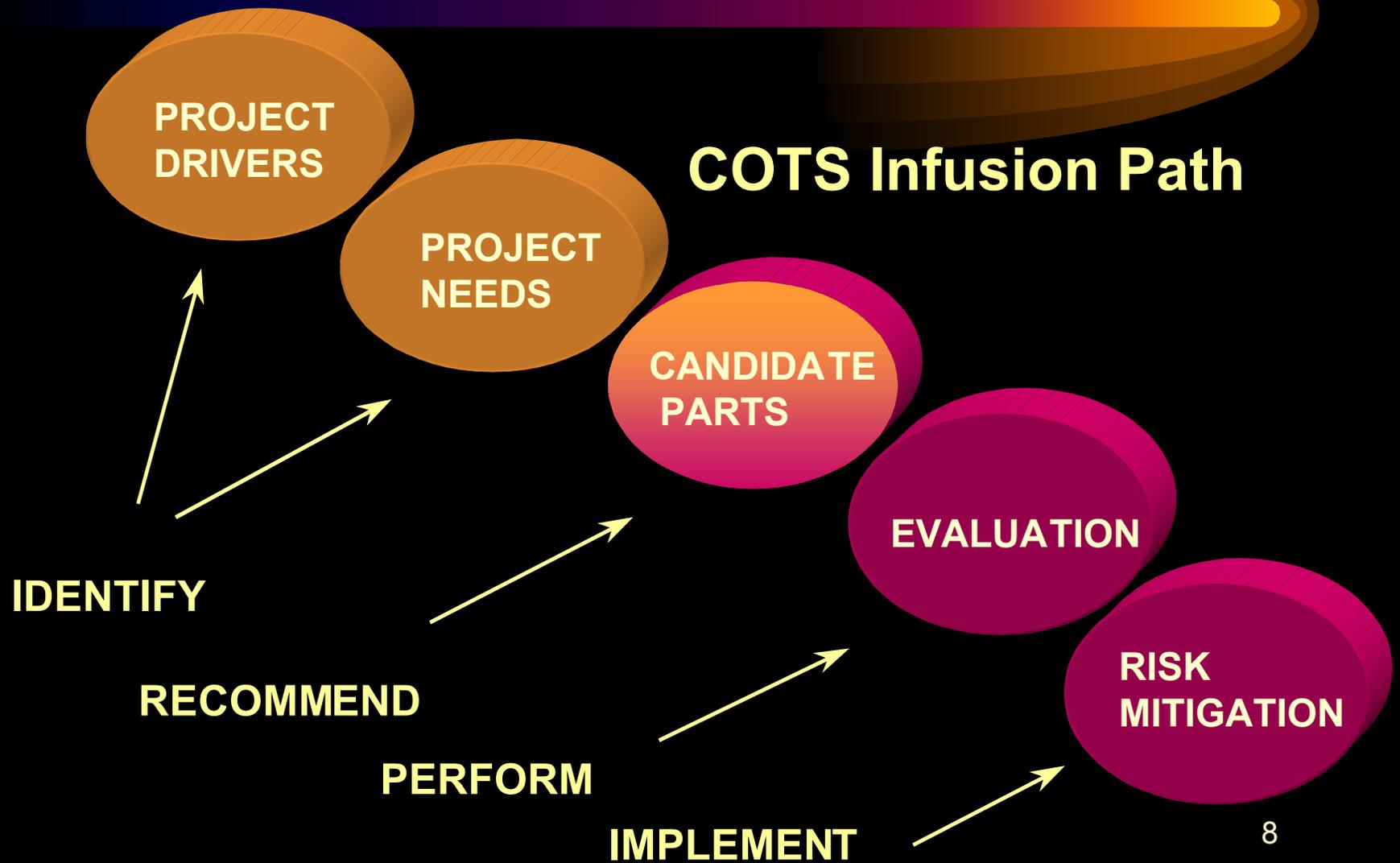
Why Put COTS in Space ?

- 1. The availability of COTS parts is proliferating.**
- 2. COTS parts performance capabilities continue to increase (e.g. processing power & high density memories)**
- 3. A new generation of leading COTS IC technologies is introduced every 3 years.**
- 4. COTS parts typically cost much less than radiation hardened counterparts; by using radiation tolerant parts the cost advantage can be preserved.**
- 5. Some COTS parts have been reported to demonstrate good to excellent reliability.**

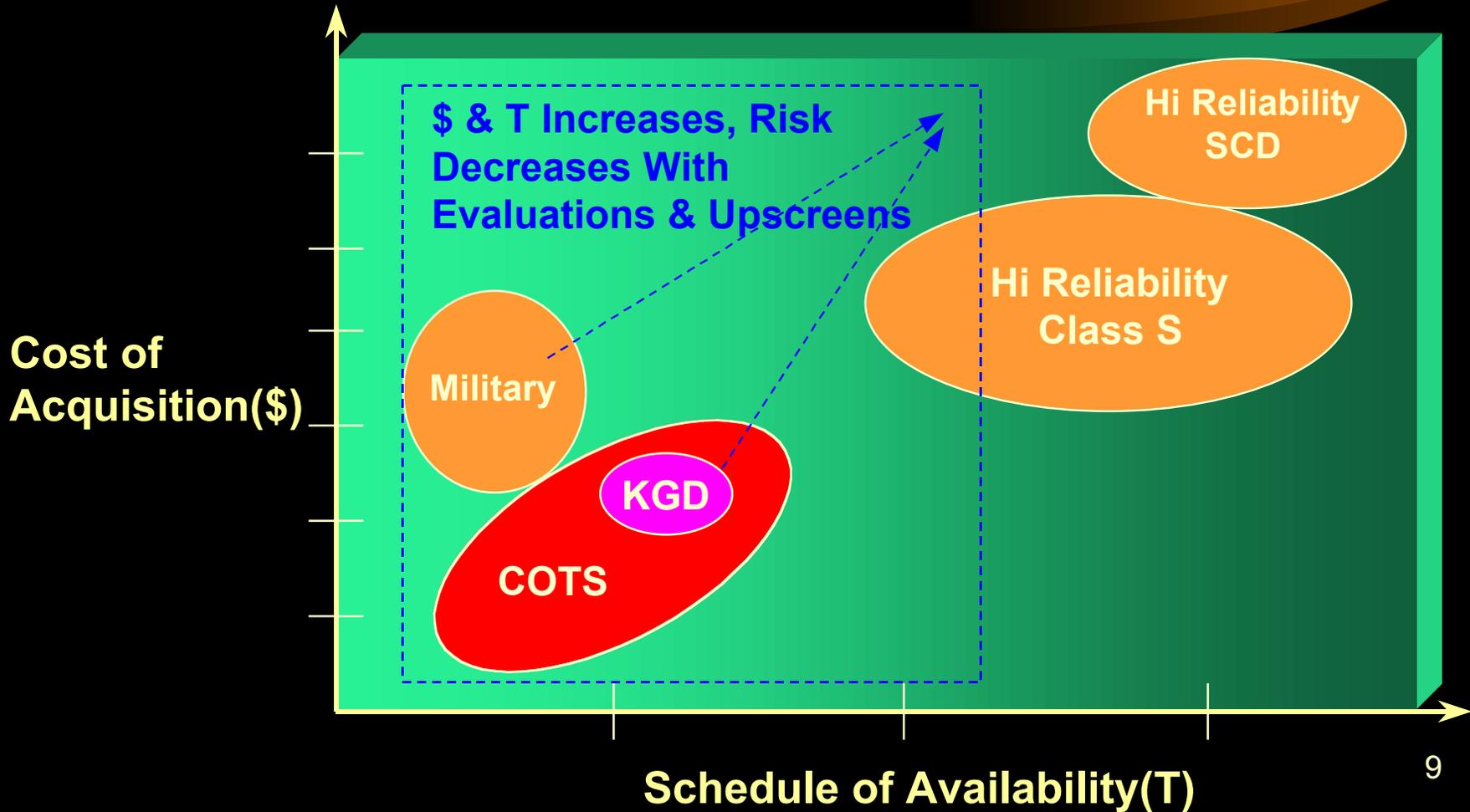


Concerns About Using COTS

- **Life Cycle is Determined by Market Demand**
- **Process/Designs Change Frequently**
- **Narrow Temperature Range**
- **Non Rad Hard Designed (maybe Rad Tolerant)**
- **Reliability of PEMS vs Ceramic**



Off-The-Shelf Part Tradeoffs





A COTS Methodology for Evaluating Parts

- **Define critical part criteria for evaluation**
- **List the best risk indicators for the part type**
- **Gather data for each indicator with minimum \$**
- **Augment part data when necessary (+\$)**
- **Find mitigating solutions for the high risk indicators**
- **Perform final part risk assessment for the application**



COTS Evaluations That Can Cost Little:

- Process
- Reliability
- Quality
- Package
- Performance

COTS Evaluations That Can Cost More:

- DPA
- Test/Burn-In
- Radiation



**Examples of Risk Indicators & Their
Relative Costs for a Plastic Package:**

• Temperature Humidity	→	Corrosion	(\$)
• Temperature Cycling	→	Assembly Defects	(\$)
• Moisture Absorption	→	Popcorning	(\$\$)
• Radiation	→	TID Degradation	(\$\$\$\$)
• Outgassing	→	Condensables	(\$\$)
• Glass Transition	→	Stability	(\$\$)



Criteria Selected for Risk Assessment of Flash Memory

List of criteria used for COTS	Current Status	Evaluation
1. Vendor	Information Complete	Accept
2. Part	Information Complete	Accept
3. Wafer Fab Technology (Process)	Partial Information Received	Accept
4. Design	No Information Available	Unknown
5. Reliability Assurance	Partial Information Received	Warning
6. Quality Assurance	No Information Available	Unknown
7. Testing	No Information Available	Unknown
8. Screening	No Information Available	Unknown
9. Performance	Partial Information Received	Accept
10. Package	Partial Information Received	Warning
11. Radiation	Partial Information Received	Unknown
12. Known Good Die	N/A	N/A
13. JPL Chip Overview	Information Complete	Accept
14. JPL DPA (Package)	Information Complete	Accept
15. JPL DPA (Die Cross Section)	Information Complete	Accept
7a. JPL Testing/Burn-In	Information Complete	Warning



Risk Indicators Selected for Reliability Assurance

A. Infant Mortality

B. Dynamic Life

C. Program Erase Cycle

	Vendor's Data	Information Received	For JPL Use Only (Quality/Risk Evaluation)				
			Unknown	Low	High	Waived	Accept
A.	Ten lots were tested at 6.5v and 125C. Results are 0/2002 after 48 hrs. and 0/2002 after 168 hrs. Intel Report 12/29/95.	X					Accept
B.	Four lots were tested at 6.5V and 125C. Results are 0/249 after 500 hrs. and 2/249 after 1000 hrs. 2 rejs are lccs due to gate oxide breakdown. Intel Report 12/29/95.	X			Burn-In Required		
C.	Four lots were tested at 0C at 100cyc.; 1K cyc.; 5K.; 10K.; and 50K. Results are 1/530 at 15,010 cycles. There were no additional failures when tested at 70C. Intel Report 12/29/95.	X		Low risk (1 failure out of 50K cyc.)			



COTS Work- Plan/Status

Known Good Die	Plastic Packages	Part Family Evaluations	LPSEP
Vendor Surveys	Moisture Absorption	Flash Memory	Characterization
Vendor Screens	Outgassing	A/D & D/A	Reliability
User Risk	Radiation	Logic	Radiation
	Delamination	Others	

Legend:

- Completed (Orange)
- Planning (Pink)
- In Progress (Magenta)



COTS Work- KGD Vendors Reviewed:

MCM Assemblies Rely on KGD for Meeting Their Operational Requirements

- National Semiconductor
- Intel
- Motorola
- Elmo Semiconductor *
- Harris Semiconductor
- Hamilton Hallmark *
- Texas Instruments
- Micron Technology
- Linear Technology
- Maxim
- Others

* Distributors - Hamilton Hallmark is a distributor that offers die solutions for the Commercial & Military World - Program is called "DieProsm"



COTS Work- MCM Risk

Assumptions

- MCM Yield (with die) = Die yield_{Vendor A} [^] No. of die Vendor A x
- A MCM yield of 1.0 means the die are tested to the same level as the package part for quality, reliability, and performance --> (KGD)
- The MCM assembly yield (w/o die) is assumed equal to 1.0
- Rework of MCMs due to faulty die is costly, hard to trouble shoot, and causes delay in schedules - it should be avoided
- Vendors who supply KGD offer many screening options

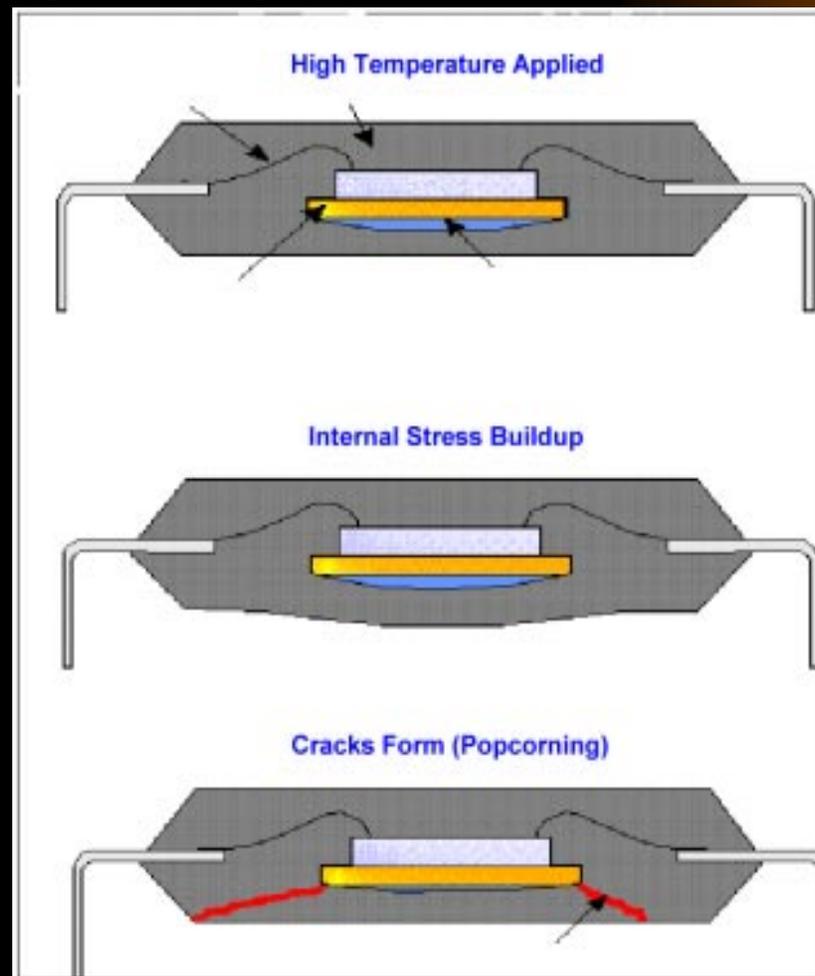
Illustration of MCM Risk of Failure vs KGD Upscreen Level



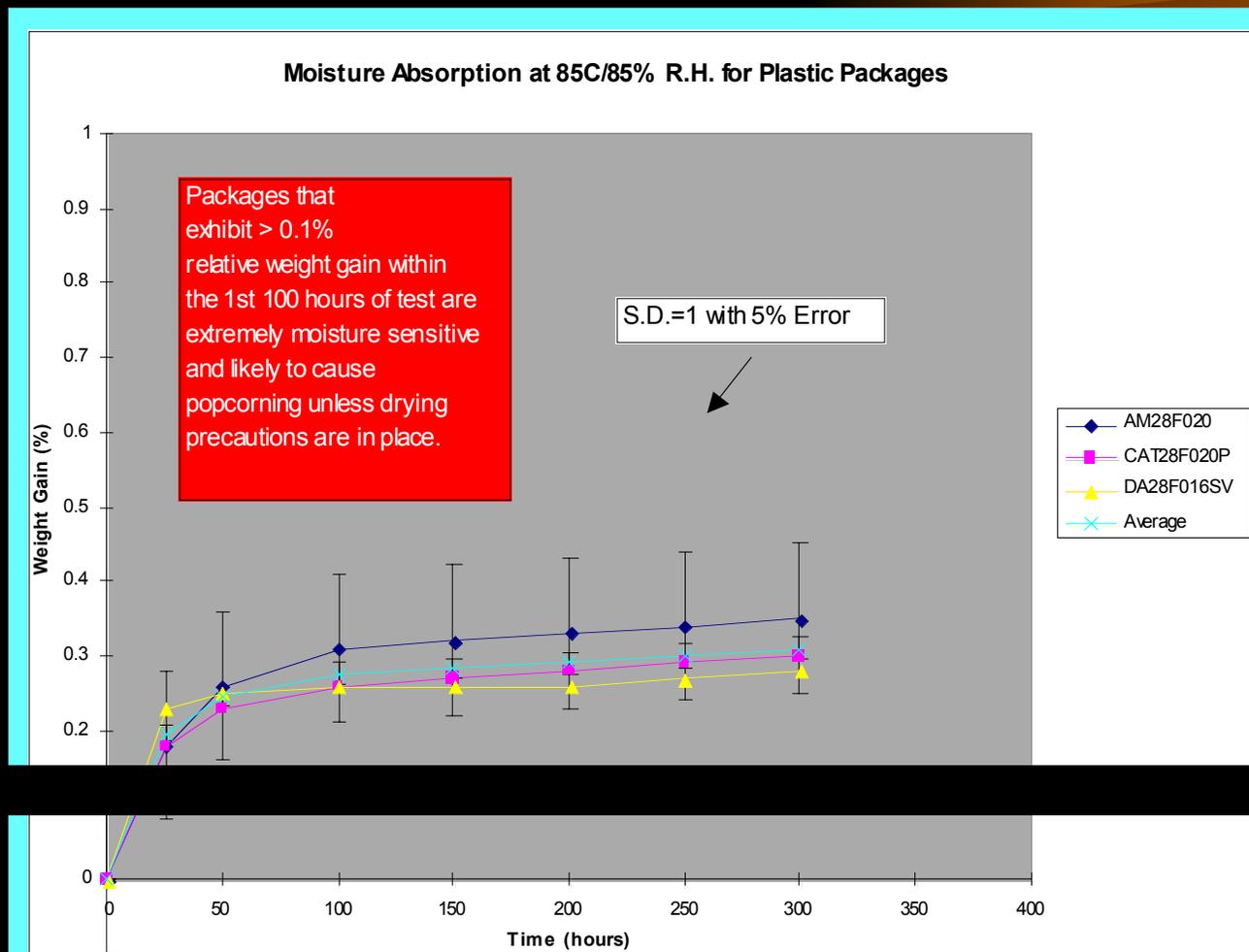
■ MCM with 5 die

Note: Die yield=88% @ L1

COTS Work - Popcorning of PEM SMDs



COTS Work - Moisture Absorption of Flash Memories in Plastic





COTS Work - Outgassing of Flash Memories in Plastic

All four packages passed specification of (TML=1.0%; CVCM = 0.1%).

Material	MCR			7612382FBA, E24, DA28F016SV, K8055, U6240332			AM28F020-150PC, 9618FBB			CSI, CAT28F020F, 1-15 09550B		
Part	Motorola SCR			Intel 16 M Flash Memory			AMD 2M Flash Memory			Catalyst 2M Flash Memory		
Sample No.	5	6	avg	7	8	avg	9	10	avg	11	24	avg
WT. Loss %	0.45	0.46	0.45	0.23	0.22	0.22	0.41	0.45	0.43	0.40	0.41	0.40
Water Vapor Recovered, WVR,	0.28	0.25	0.26	0.14	0.11	0.12	0.19	0.17	0.18	0.21	0.18	0.19
%TML (WT, LOSS-WVR) %	0.17	0.21	0.19	0.09	0.11	0.10	0.22	0.28	0.25	0.19	0.23	0.21
CVCM %	0.04	0.08	0.06	0.02	0.01	0.01	0.03	0.05	0.04	0.04	0.04	0.04
DEPOSIT on CP	Opaque			Negligible			Opaque			Opaque		
FTIR Results	Amine cured epoxy			Anhydride cured epoxy			Amine cured epoxy			Amine cured epoxy		



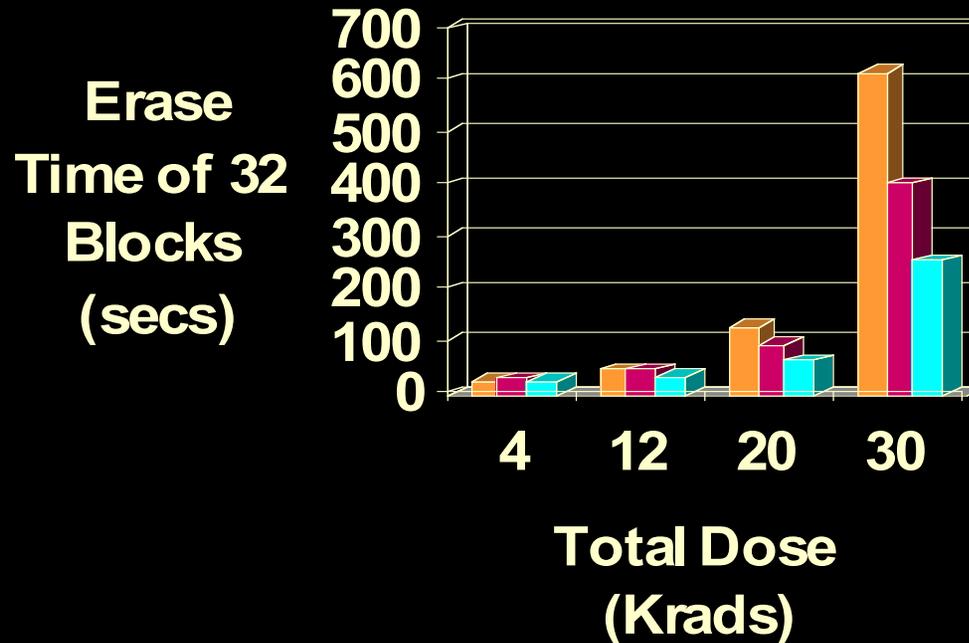
COTS Work - Radiation Levels

Electronic Parts Comparison



Commercial Part	Rad-Tolerant Part	EPI CMOS Part	SOI CMOS Part	Rad-Hard Part
Hardness limited by inherent process and design; customer's risk	Hardness offered as a by-product of the design & process	Hardness offered as a by-product of the design & process	Hardness offered as a by-product of the design & process	Designed & processed for specific hardness level
Total Dose : 2 krad to 10 krad (typical)	Total Dose : 20 krad to 50 krad (typical)	Total Dose : > 50 krad (typical)	Total Dose : >100 krad (typical)	Total Dose : >200 krad to 1 Mrad or more (typical)
SEU : threshold LET: 5 Mev/mg/cm2 (typical)	SEU : threshold LET: 20 Mev/mg/cm2 (typical)	SEU : threshold LET: 30 Mev/mg/cm2 (typical)	SEU : threshold LET: 120 Mev/mg/cm2 (typical)	SEU : threshold LET: 80-150 Mev/mg/cm2 (typical)
SEU error rate :10E-5 errors/bit-day (typical)	SEU error rate :10E-7 to 10E-8 errors/bit-day (typical)	SEU error rate :10E-9 to 10E-10 errors/bit-day (typical)	SEU error rate :10E-9 to 10E-10 errors/bit-day (typical)	SEU error rate :10E-10 to 10E-12 errors/bit-day (typical)
Latchup : Customer evaluation and risk	Latchup : Customer evaluation and risk	Latchup : Varies by process and EPI thickness	Latchup : Eliminated	Latchup : SOS, BiPolar Technologies; Eliminated
Guarantees: None	Guarantees: None	Guarantees: None	Guarantees: None	Guarantees: High

TID Response of Intel 16M Flash Memory In Plastic Package



■ 85C/85%RH ■ No Precond. ■ 100C Bake for 44 hr.



COTS Work- Reports

Published

- **PCA for Intel DA28F016SV**
- **Part/Package Analysis for Intel DA28F016SV**
- **Part/Package Analysis for AMD AM28F020**
- **Part/Package Analysis for Catalyst CAT28F020P**
- **Electrical Performance for Intel DA28F016SV with Temperature**
- **Burn-In Results for Intel DA28F016SV**

In Writing:

- **Total Dose for Intel DA28F016SV**
- **Moisture Absorption/Desorption for Plastic Packages**
- **Outgassing Characteristics for Plastic Packages**
- **Methodology & Criteria for Risk Assessment of COTS Parts**



COTS Work- 507 Data Base

UTILITIES:

DATA (Parts, Vendors, Surveys, etc..)

INFORMATION (Generic, Plastics, KGD, etc..)

ASSESSMENT (Parts, Technology, etc.)

ANALYSIS (DPA, CA, SEM, etc..)

TOOLS (what if analysis for KGD yield, etc.,)

FORMATS:

EXCEL , WORD, PDF, HTML, PowerPoint



In Summary

- Using COTS parts without understanding their pedigree can lead to mission delay or worst ➔ **mission failure**
- A methodology is in place in Office 507 to help JPL users of COTS parts ascertain their risk and acceptance for Space Application
- Work is underway in Office 507 to evaluate all risk factors of using COTS parts (quality, reliability, radiation, package, and device performance)

JET PROPULSION LABORATORY
Electronic Parts Engineering Office



**For Further COTS
Information Contact:**

Mike Sandor
x 4- 0681

Shri Agarwal
x 4-5598 or
818-795-4928 x 203