



**JPL Technical Infrastructure Program-
Commercial Off-The-Shelf (COTS)
Low Power Space Electronic Parts (LPSEP)**

A report on

**Low Power Evaluation
of COTS 4M Static Rams for
Space Applications**

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Abstract

The work described herein was performed under the auspices of LPSEP (Low Power Space Electronic Parts) task whose objective is to identify flight worthy 3.3V state-of-art devices. 5V commercial 4-megabit static random access memories (4Meg SRAMs) from Sony, Hitachi and Motorola were characterized for operation at 3.3V. This work was done in collaboration with Space Electronics, Inc. (SEI). Based on the test results and the fact that they already sell a 5V radiation tolerant 4Meg SRAM with Hitachi die, SEI has offered to make a 3.3V Hitachi version for the Space community.

Introduction

The CMOS Revolution

Ever since its inception in 1963, the CMOS technology has revolutionized the world of electronics. Because of their low power feature, the CMOS parts have been extremely popular among NASA designers. They have been successfully used at JPL: Taking digital logic parts as an example, Voyager used the RCA CD4000A series that operated at 12V, Galileo used the RCA CD4000B series that operated at 10V and Cassini used the Harris HCS/ACS family that operated at 5V. Thus, over the last 20 years, similar to trends in the industry, the operational voltage in JPL flight applications has been coming down. The new projects are willing to use parts at 3.3V if we can find them. Figure 1 shows the forecasted migration of low power designs at JPL vs industry.

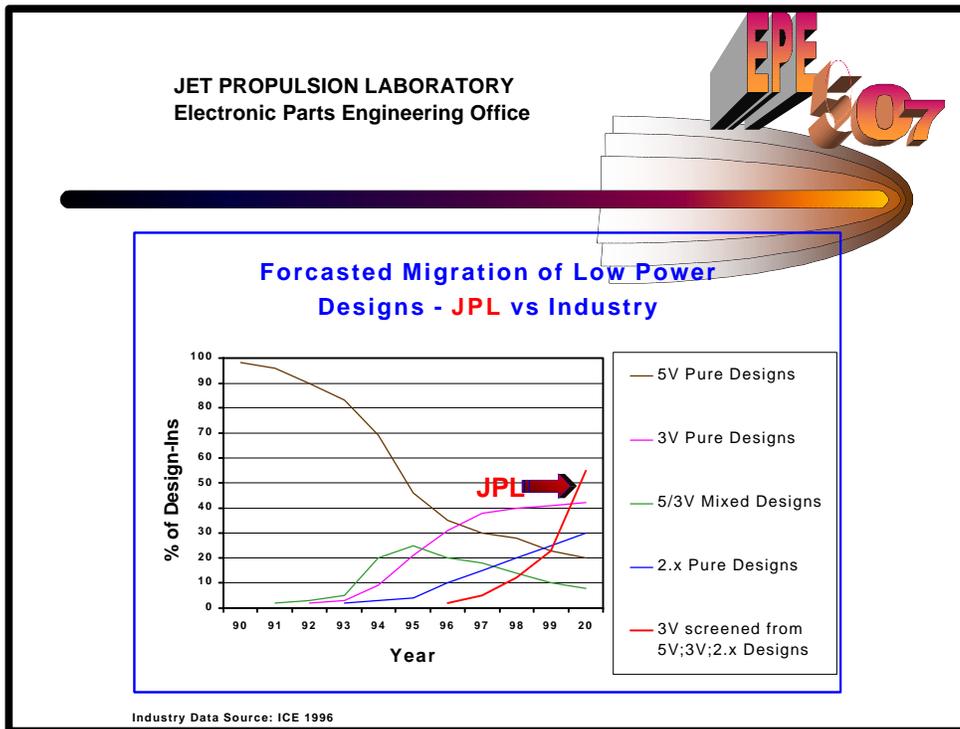


Figure 1

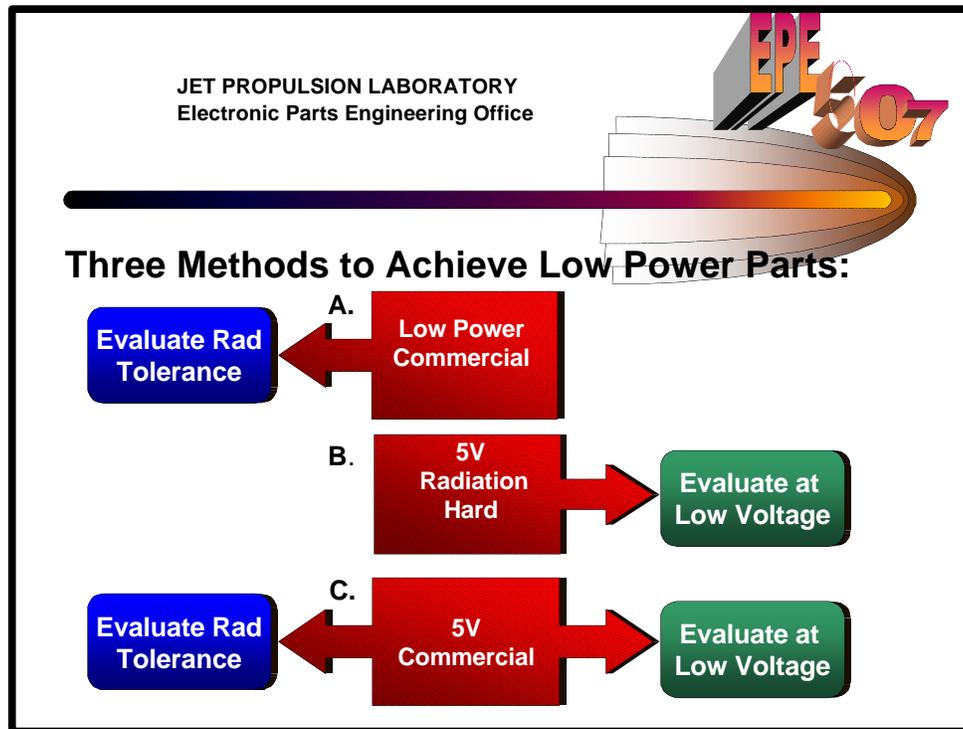


Figure 2

An “Accelerated” CMOS Revolution

In recent years the low power feature of the CMOS technology has been exploited for portable or hand-held commercial applications. For such applications, lower voltages translate directly into less battery drain and hence longer battery life. Therefore, there is a tremendous push in the commercial industry to develop parts that work at lower and lower voltages, the goal being operation at single battery cell voltage of 1.5V by the year 2000.

Low Power Space Electronic Parts (LPSEP) Task

The objective of the LPSEP task is to identify flight worthy 3.3V state-of-art parts. As shown in figure 2, the approach can be divided into three groups. A discussion of evaluation done for each of the groups follows:

A. LPSEP evaluation of low power commercial parts

Up until now, the LMX23XX family of monolithic low power, high-speed phase locked loop (PLL) frequency synthesizers from National Semiconductor have been available as commercial parts in 20 pin plastic packages. These parts are built on state-of-the-art BiCMOS processes. JPL performed construction analysis and radiation characterization. The evaluation for radiation included high and

low dose rate total dose testing, and testing with protons and heavy ions. Based on the results of JPL evaluation, their own evaluation and interest from other Space users, National has announced that selected PLL products will be offered as radiation tolerant QML parts in 20-pin surface mountable ceramic packages. The JPL evaluation was done for the EOS-MLS project who will be using the QML version.

B. LPSEP evaluation of 5V rad hard parts

United Technologies (UTMC) was selected for performance assessment at 3.3V because they offer a broad spectrum of QML certified, radiation-hardened, cell based standard 5V MSI/LSI/VLSI products. The low voltage characterization of representative MSI functions by JPL, and of ASICs by the supplier, suggested that the parts would work at 3.3V.

C. LPSEP evaluation of 5V commercial parts

The subject of this report is the LPSEP evaluation of 5V commercial parts.. It has a two-fold focus: (i) Will a 5V state-of-the-art commercial part operate at some lower voltage such as 3.3V, and (ii) Will the supplier or a third party offer a 3.3V radiation tolerant reliable version that the JPL/NASA projects can use. 5V commercial 4-Meg SRAMs from three different suppliers were characterized for operation at 3.3V. Given below is a brief review of components of power dissipation followed by the details of the SRAM low voltage characterization.

Components of Power Dissipation in Digital CMOS Circuits

Power dissipation in CMOS digital circuits can be simply categorized into two main components: the first is called static power and the second is called dynamic power. The two significant sources for static power are leakage currents of reversed-biased PN junctions and sub-threshold MOS current transport. The source for dynamic power is due to short circuit currents flowing from Vdd to Gnd and capacitive power switching of internal circuit nodes. Therefore the total power dissipation for CMOS digital circuits is the sum of the static and dynamic power.

In typical CMOS operation the dynamic power is dominant over the static power. One can expect dynamic power to make up to 90% of total power and static power to make up the other 10%. Since dynamic power is the majority of power consumption, it is where the most power reduction can be realized using some controls. Two controls that can be changed by a user are the setting of the Vdd supply operation voltage and the clock frequency and clock cycle. In particular the Vdd operating supply voltage greatly influences the capacitive power and the short circuit power according to the following equation.

$$P_T = n_p * C_L * V_{dd} * f + I_{sc} * V_{dd}$$

Therefore by controlling (reducing) the Vdd operating supply voltage, the two contributing factors to the power dissipation can be reduced. The average power savings is illustrated in figure 3 below.

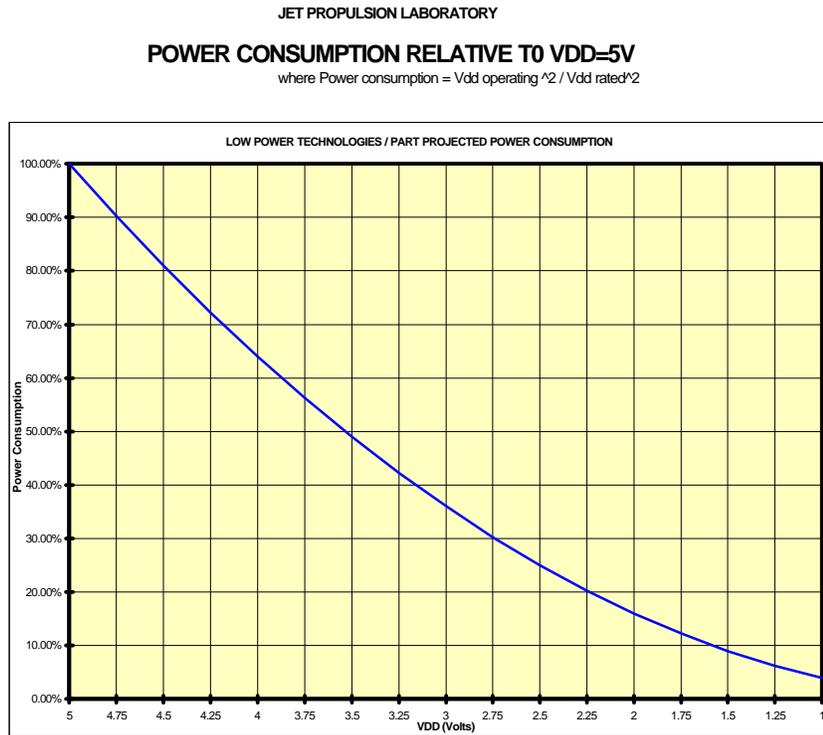


Figure 3

Because of this relationship between power and Vdd control, it was the logical approach taken to evaluate how Commercial Off-The-Shelf (COTS) 5V CMOS SRAMs could potentially realize a power savings operating at a lower Vdd. If nominally designed 5V parts could operate at some lower Vdd such as 3V, a potential savings of >50% would be realized according to the above figure. This approach is considered as an alternative when there are no low power devices available (e.g. 3V designs) that meet the performance or functional requirements of a mission.

This methodology, called upsampling, is not supported by any known supplier of commercial products. Taking this approach is totally at the risk of the user and caution must be observed. Some of the risk issues to consider when one follows this approach are:

- ❑ Speed degradation
- ❑ Realized average power savings vs theoretical
- ❑ Performance over temperature range
- ❑ Radiation effects
- ❑ Reliability issues, etc.

5V Commercial 4-Meg SRAM Test Data

The work described herein only considered the electrical performance of commercial SRAMS under different Vcc operating supply voltages, and at the same time extending the commercial operating temperature range to a military temperature range. For this work three different SRAMS were chosen. They were:

1. Hitachi, part number HM628512LFP-5, 512-kword x 8-bit
2. Sony, part number CXK584000TM-5511, 512-kword x 8-bit
3. Motorola, part number MCM6246WJ20, 512-kword x 8-bit

The access time specification for the Motorola part is 20ns, and 55ns for Sony and Hitachi. At these access times, the Motorola part draws 10 times more power than the other two. All three parts have basically the same pin assignment (19 addresses, 8 data I/O's, 2 power pins and 3 controls), except that the Motorola parts have two additional power pins.

Six parts were randomly selected from a lot of 20 parts from each of the above suppliers. Three test software programs were generated to characterize access time, functionality, output voltage, and power supply current for Vcc from 3 volt to 5.5 volt. Built-in patterns of spiral complement march, walk row bar, checker board compliment, and surround disturb were used to characterize the functionality of the devices. The functional characterization and parametric tests included Vcc vs temperatures of 25°C, 70°C, 125°C, 0°C, -20°C, and -55°C. The parts were tested using a 20 MHz Sentry digital tester. It must be pointed out that setup timing parameters often times are adjusted during test to put devices in proper readout. These timing changes if required must be noted when using parts outside their nominal operating manufacturing specifications.

A summary of functional test results, typical supply currents, and access times is given on the following pages.

Note: Additional raw test data is available upon request.

Functional Test* Results at Vcc = 3V and 3.6V

Temp	Sony		Hitachi		Motorola	
	@3V	@3.6V	@3V	@3.6V	@3V	@3.6V
+125C	6/6	6/6	6/6	6/6	0/6	6/6
+70C	6/6	6/6	4/6	6/6	0/6	6/6
+25C	6/6	6/6	4/6	6/6	0/6	6/6
0C	6/6	6/6	4/6	6/6	0/6	5/6
-20C	6/6	6/6	4/6	6/6	0/6	5/6
-55C	6/6	6/6	0/6	6/6	0/6	5/6

Table 1

* Included running the following test patterns: Spiral complement march, walk row bar, checker board compliment, and surround disturb.

Sony was the best performer; it worked over 3.3V+/-10% and -55C to +125C. However, there is no radiation data on Sony.

Hitachi was the next best performer. It worked over 3.3V+/-10% and -20C to +125C. As is evident from the above data, some yield loss is expected to occur at 3V. The temperature performance could be further refined by taking additional data at temperatures below -20C and above -55C. Based on these test results and because they already sell a 5V radiation tolerant 4Meg SRAM with Hitachi die, SEI has offered to make a 3.3V Hitachi version for the Space community.

Motorola did not meet their own spec for TAA; spec is 20ns, the parts read 34ns (see table 3). Moreover, they did not pass all test patterns at 3V (see table 1). For these reasons, the evaluation of the Motorola parts was not pursued any further.

Typical Dynamic (I_{dn}) and Stand-by Currents at Room Temperature					
Manufacturer	Vcc = 5.5V		Vcc = 3.6V		Avg. Power Savings
	I_{dn}	I_{sb}	I_{dn}	I_{sb}	
Sony	12.7mA	345uA	6.0mA	23ua	69%
Hitachi	11.5mA	680ua	5.6mA	45.6ua	68%
Motorola	121mA	6.74mA	49.4mA	1.13mA	73%

Table 2

Typical Access Times (TAA) at Room Temperature			
Manufacturer	Vcc = 4.5V	Vcc = 3.0V	Speed Penalty
	Sony	39.22ns	
Hitachi	45.16ns	65.94ns	20.78ns
Motorola	34.84ns	48.44ns	13.60ns

Table 3

Conclusion

Of all methods available to reduce power consumption in Space hardware, the selection and evaluation of 5V parts down to their lowest and safest operating voltage can bring immediate and high returns as shown in Table 2. It is probably the path least considered and pursued by many JPL projects. Many existing parts (functions) have the potential to be operated at lower than nominally specified voltages and realizing power savings by at least 50%. However, the number of parts that can be evaluated is constrained by funding and to some level in identifying real part candidates for specific JPL projects. This alternative method to reducing power consumption should be considered for its value to capitalize on using existing technologies (commercial or rad hard). It may even cost less than designing a power reducing custom circuit.

Acknowledgement

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