Reliability of Compound Semiconductor Devices for Space Applications

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Abstract

Application of semiconductor devices in high reliability space systems requires a thorough understanding of the reliability and failure mechanisms associated with the selected devices. This paper provides a description of the reliability and qualification issues related to the application of compound semiconductor devices in critical space systems. A discussion of common failure mechanisms, radiation effects and other reliability concerns is provided along with a discussion of methods for technology qualification for high reliability space applications.

Introduction

The recent growth of the compound semiconductor industry has resulted in substantial improvements in processing methods, fabrication yield, and overall quality of commercially viable compound semiconductor devices. This coupled with large volume production and the utilization of statistical process control has greatly reduced the infant mortality population without having to impose traditional high reliability part specifications. However, reproducibility of a product does not guarantee reliability in the intended application. For critical space applications where the success or failure of a mission hinges on the lifetime and performance of a single device; it is critical that all aspects of the reliability and the various known failure modes and mechanisms be addressed prior to the insertion of the component in the application [1].

The selection and application of microelectronic components in high reliability space systems requires knowledge of the component design, fabrication process, and applicable tests. In addition, reliability analysis and detailed knowledge of the application environment is necessary in order to determine the suitability of the selected component for the application. These issues are of particular importance for the application of compound semiconductor devices in high reliability systems due to the need for the utilization of large numbers of these devices at the upper limit of their performance and stress capabilities.

The user of compound semiconductor devices must gain an understanding of not only the technology performance capabilities but also of the limitations of the technology and must employ methods to utilize it in a reliable fashion. The user must also understand that many of the failure mechanisms associated with silicon devices do not apply to GaAs and other compound semiconductors, and new device structures bring new failure mechanisms. In addition, many of the traditional assumptions for mean-time failure rate predictions do not hold for those new devices. Thus, today's high reliability user must be more aware of measurement based predictions of long term failure rate over calculation based predictions.

This article provides a brief overview of reliability issues relating to compound semiconductor devices and some common practices for determining suitability of these devices for application in high reliability space systems.

Reliability and Qualification for Space Applications

Device reliability involves probability statistics, time, and a definition of failure. Given a failure criterion, the most direct way to determine reliability is to submit a large number of samples to actual use conditions and monitor their performance against the failure criteria over time. Since most applications require device lifetimes of many years, this approach is not

practical. To acquire device reliability data in a reasonable amount of time, an accelerated life test at high temperatures is used. This type of accelerated test is based on the observation that most failure mechanisms are thermally activated. By exposing the devices to elevated temperatures, it is possible to reduce the time to failure of a component, thereby enabling data to be obtained in a shorter time than would otherwise be required. Such a technique is known as "accelerated testing" and is widely used throughout the semiconductor industry. The rate at which many chemical processes take place is governed by the Arrhenius equation:

$$R = A \exp(-Ea/kT)$$

Where
R = rate of the process
A = a proportional multiplier
E_a = activation energy, a constant
K = Boltzman's constant, 8.6×10^{-5} (eV/K)
T = Absolute temperature in Kelvin

This equation has been adopted by the semiconductor industry as a guideline by which the operation of devices under varying temperature conditions can be monitored. Experimental data obtained from life tests at elevated temperatures are processed via the Arrhenius equation to obtain a model of device behavior at normal operating temperatures. Rearranging the Arrhenius equation allows the temperature dependence of component failure to be modeled as follows:

$$\ln t_2/t_1 = E_a/k\,(1/T_2 - 1/T_1)$$

where

$t_{1,2}$ = time to failure
E_a = activation energy in electron volts
T = absolute temperature in Kelvin

Qualification can be defined as the verification that a particular component's design, fabrication, workmanship, and application are suitable and adequate to assure the operation and survivability under the required environmental and performance conditions.

Traditional qualification methods require extensive test and characterization of the specific component using a predetermined set of tests and characterization conditions. This approach has been very costly in schedule and expense and typically results in very little interaction between the device manufacturer and the user.

A methodology for qualification based on continual interaction between the device manufacturer and the user is described in this paper. This interaction results in a detailed understanding of the device design, fabrication, and limitations along with the specific application conditions and expected operating environment. The methodology is divided into three main categories; Process Qualification, Product Qualification, and Product Acceptance.

Process Qualification: Is a set of procedures the manufacturer follows to demonstrate the control of the entire process of design and fabrication using a specific technology (MESFET, HEMT, HBT, etc.). It addresses all aspects of the process including the acceptance of starting materials, documentation of procedures, implementation of handling procedures and the establishment of lifetime and failure data for devices fabricated using the process. Since the goal of process qualification is to provide assurance that a particular process is under control and known to produce reliable parts, it needs to be performed only once, although routine monitoring of the production line is standard. In addition, any significant changes in the process may require re-qualification of the process. It is critical to remember that only the process and basic circuit components are being qualified. No reliability information is obtained for particular component designs.

Although process qualification is intended to qualify a defined fabrication procedure and device family, it must be understood that the technology is constantly evolving, and this technology evolution requires the continual change of fabrication procedures. Thus, strict application of the commonly used phrase, "freezing the production process," does not apply.

The qualification process also involves a series of tests designed to characterize the technology being qualified. This includes the electrical as well as the reliability characteristics of components fabricated on the line. Some of these tests are performed at wafer level and include the characterization of Process Monitors (PM), and Technology Characterization Vehicles (TCV). Others tests require the mounting of circuits or elements into carriers. Figure 1 provides a

summary of the steps necessary for process qualification.

Figure 1

In reality, the manufacturer will already have an existing and defined process with established reliability and qualification procedures and practices. Therefore, it is the user's responsibility to become knowledgeable of these practices, get involved in the activities of the Technology Review Board (TRB), and to become aware of the necessary qualification steps. All of these tests and the applicable procedures are an integral part of the qualification program and provide valuable reliability and performance data at various stages in the manufacturing process.

Product Qualification: is the verification that a component will satisfy the design and application requirements under the specified conditions. The information sought after in this approach is design specific and applies to devices fabricated on qualified process lines. This qualification step is composed of Design Verification and Product Characterization.

Design Verification is one of the best ways of reducing engineering costs and improving reliability. Design reviews with the participation of the device manufacturer and the device user are a means of accomplishing this verification of model or simulation and layout of the design prior to fabrication. Figure 2 shows a typical design flow and the necessary interaction points. Verification of circuit design is only applicable to custom designs and requires detailed knowledge of the design tools, device physics , layout tools, fabrication , and test which requires the participation of personnel from the various disciplines.

Figure 2

Product characterization is another important aspect of product qualification. Thermal analysis and test to determine the thermal characteristics of the design, along with ESD sensitivity tests, voltage ramp tests, and temperature ramp tests are all essential in obtaining an understanding of the limitations and characteristics of the design. These characterizations are applicable to both custom and standard designs and are an accepted practice for establishing product qualification. Figure 3 shows a typical design validation flow.

Figure 3

Product Acceptance: Although devices may be designed by highly qualified personnel, fabricated on a process qualified production line, and verified through measurements to meet the design goals; parts with poor reliability characteristics still may exist. This may be due to variations in the fabrication process, or material flaws that were undetected, or, as is more often the case, to the device package and stress imposed on the device during packaging. Regardless of the cause, these weak devices must be found and removed before they are integrated into the system. Therefore, manufacturers of high reliability systems require the devices to pass a series of product acceptance screens, whose sole purpose is to increase the confidence in the reliability of the devices. This step in the qualification methodology is the major difference between space-qualified devices and commercial grade devices.

The level of testing performed under product acceptance is a function of the form of the deliverable. For example, the first level of acceptance testing, called "wafer acceptance test" is performed at the wafer level to assure the uniformity and reliability of the fabrication process through a wafer to wafer comparison. "Lot acceptance test for die" is a second level of testing that provides further reliability information, but only on a sample of the devices because of the difficulty in performing full characterization on non-packaged devices. "Packaged device screen" is performed on 100% of the devices if the deliverable is a packaged product.

COTS for Space Applications

In order to reduce the overall system costs associated with high reliability space applications, systems are being designed with a significant number of Commercial-Off-The-Shelf (COTS) components. This approach can provide for a reduced initial cost of the components and may facilitate faster system design and fabrication schedules. However, attention to the reliability aspects of the applications and the maturity of the COTS components must also be taken into consideration.

Determining the suitability of COTS components for application in high reliability space systems represents a significant challenge to the reliability engineer, where it is necessary to have a detailed understanding of the failure mechanisms associated with each technology and

device design. Therefor, it is critical for the reliability engineer to understand and validate the results of reliability tests conducted by the device manufacturer. In addition, it may be necessary to conduct additional device evaluation and characterization tests to qualify the devices for the intended application and environment, a process referred to as "up-screening".

Failure Modes and Mechanisms

Failures in electronic devices can be classified as either catastrophic failures or degradation failures. The exact mechanism, which causes the failure is normally dependent on the material structure, processing methods, application, and stress conditions. Device bias, resultant channel temperature, passivation, and material interactions may all cause or contribute to different failure mechanisms. Furthermore, device handling, choice of materials for packaging and the application environment may also cause failures[2]. Some common failure mechanisms affecting the device at die level:

Gate-Metal Sinking: The performance of GaAs-based devices relies heavily on the quality of the active channel area of the device. The Schottky gate metal-to-semiconductor interface directly influences the device electrical parameters, such as the drain saturation current and reverse breakdown. The gate structures are based on the industry standard multi-layer Au/Pt/Ti or Au/Pd/Ti on GaAs. Inter-diffusion of gate metal with GaAs results in a reduction of the active channel depth and a change in the effective channel doping. This effect is termed "gate sinking." This process is affected by the surface conditions of the GaAs material at the time of deposition, the deposition parameters, and the choice of deposited materials [3,4].

Ohmic Contact Degradation: The most common system for ohmic contacts is AuGe/Ni, which is alloyed into the GaAs at temperatures in excess of 400°C to provide the necessary low contact resistance (0.1 to 0.5 Ω/mm). A thick Au layer is then deposited on top of the alloyed contacts to provide conduction. This structure, employed at the drain and source contacts, has been shown to degrade at elevated temperatures (>150 °C). The degradation is the result of Ga out-diffusion into the top Au layer and the diffusion of Au into the GaAs causing an increase in the contact resistance. The Ni layer used in the ohmic contact is intended as a Au- and Ga-diffusion barrier. Some other materials such as Cr, Ag, Pt, Ta, and Ti have been used as barrier materials with varying degrees of success[16]. The activation energy associated with ohmic contact degradation varies between 0.5 eV and 1.8 eV. This activation energy may provide reasonable contact life at low operating temperatures (<100 °C) but it also indicates rapid deterioration at elevated temperatures [5].

Channel Degradation: Degradation observed in device parameters can sometimes be attributed to changes in the quality and purity of the active channel area and a reduction in the carrier concentration beneath the gate Schottky contact area. These changes have been postulated to be a result of diffusion of dopants out of the channel or diffusion of impurities or defects from the substrate to the channel. Deep level traps have also been postulated to cause similar degradation in MESFETs [17].

HEMT devices, being strongly dependent on the properties of the interface of the AlGaAs/GaAs heterostructure, can suffer a related failure mechanism. A decrease in electron concentration in the channel, caused by a de-confinement of the 2-Dimensional Electron Gas (2DEG), was postulated to be the cause of the observed failure mechanism.

HEMT devices can also suffer from metal-diffusion-related mechanisms, which are manifested as channel-related degradation. Lateral diffusion of Al into the gate recess region changes the conduction band discontinuity and consequently the confinement of the channel electrons. Gold diffusion from the ohmic contact into the active channel region under the gate can also cause similar degradation. Lastly, vertical diffusion of Al from the AlGaAs donor layer and Si from the n^+ AlGaAs layer into the channel layer causes an increase in the impurity scattering in the undoped GaAs, thus deteriorating the high electron mobility of the 2DEG [6].

Surface State Effects: The performance of GaAs-based devices depends highly on the quality of the interface between metal and GaAs or the passivation layer (Si_3N_4 or SiO_2) and GaAs. The quality of the interface can depend on the surface cleaning materials and procedures, the deposition method and conditions, and the composition of the passivation layer. As shown in Fig. 4, the

main effect of an increase in surface state density is the lowering of the effective electric field at the drain/gate region, which results in an increase in the depletion region and a change in the breakdown voltage.

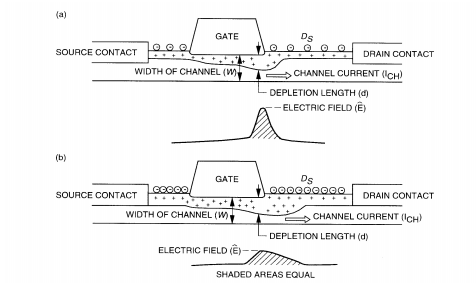

Figure 4. Schematic cross section of a MESFET with different surface charges. (a) with low density of surface states, and (b) with high density of surface states[13].

Unpassivated devices can be susceptible to surface oxidation and loss of arsenic, which may result in an increase in gate leakage current and a reduction of the breakdown voltage. Devices passivated using SiO_2 may experience surface erosion due to the interaction of SiO_2 with GaAs [7].

Electromigration: The movement of metal atoms along a metallic strip due to momentum exchange with electrons is termed electromigration. Since the mechanism is dependent on momentum transfer from electrons, electromigration is dependent on the temperature and number of electrons. Therefore, this failure mechanism is generally seen in narrow gates and in power devices where the current density is greater than $2x10^5$ A/cm^2, which is normally used as a threshold current density for electromigration to occur. As shown in Fig. 5, this effect is observed both perpendicular and along the source and drain contact edges and also at the interconnect of multilevel metallizations.

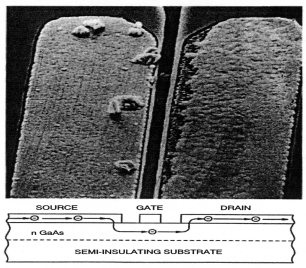

Figure 5. Depletion and accumulation of material in AuGeIn source and drain ohmic contacts induced by electromigration.

The metal atoms that migrate along the line tend to accumulate at the grain boundaries. The accumulation of metal at the end of the gate or drain contact can create fingers of metal that can short the device. Material accumulation and void formation perpendicular to the source and drain contacts can cause hillock formation over the gate structure. This may result in shorting the gate to the source or drain which may result in catastrophic failure.

Hot Electron Trapping: Under RF drive, hot electrons are generated near the drain end of the channel where the electrical field is the highest. A few electrons can accumulate sufficient energy to tunnel into the Si_3N_4 passivation to form permanently changed traps. As shown in Fig. 6, these traps can result in lower open-channel drain current, transconductance, and higher knee voltage, leakage current, and breakdown voltage. Since the traps are located above the channel, there is usually little change in the dc or small signal parameters near the quiescent point. Further, since the traps are located beside the channel, Schottky-barrier height and the ideality factor often remain constant. This selective change in device characteristics helps distinguish hot-electron effects from thermal or environmental effects [8].

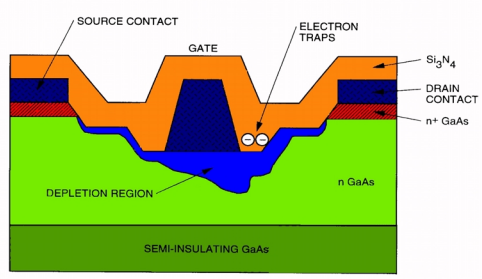

Figure 6. Schedmatic cross section of a degraded MESFET showing hot-electron-induced traps in the SiN passivation layer.

Hydrogen Effects: Degradation in I_{DSS}, V_p, g_m, and output power was observed on GaAs and InP devices tested in hermetically sealed packages or

under hydrogen atmosphere. The source of the degradation has been attributed to hydrogen gas desorbed from the package metals (Kovar, plating, etc.). The exact mechanism by which hydrogen degrades the device performance and the path by which hydrogen reaches the active area of a device are not known and have been under investigation [9].

Earlier research, [18], on GaAs transistors identified the diffusion of atomic hydrogen directly into the channel area of the device where it neutralizes the silicon donors as the possible mechanism. It is believed that atomic hydrogen diffuses into the GaAs channel and forms Si-H, thereby neutralizing the donors. Experiments have shown that exposure of Si-doped GaAs to RF hydrogen plasma results in neutralization of the Si donors. Infrared spectroscopy data have also given evidence of $(SiAs_3)As$-H complexes[19].

The neutralization of donors can decrease the carrier concentration in the channel, which, in turn, can decrease the drain current, transconductance, and gain of the device. Hydrogen effects in FETs with either Pt or Pd gate metals have been observed. Recent research has concluded that the diffusion of hydrogen may occur at the Pt side-walls and not at the Au surface of the Au/Pt/Ti gate metal[20].

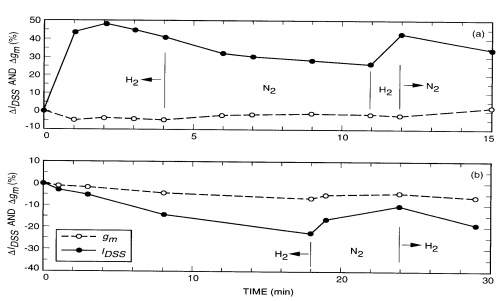

Figure 7. Changes in peak transconductance, g_m, and drain current at zero bias, I_{dss}, of (a) InP HEMT and (b) GaAs PHEMT under nitrogen and 4% hydrogen treatment at 270°C[21].

Other research, an example of which is shown in Fig. 7, on GaAs PHEMT and InP HEMT in a hydrogen atmosphere has shown that the drain current may increase in some cases. This observation has led to the conclusion that the hydrogen diffuses into the semiconductor surface where it is thought to change the metal-semiconductor built-in potential.

Manufacturers and users of GaAs devices used in hermetically sealed packages are currently pursuing an acceptable solution to this problem. Some of the possible solutions include thermal treatment of the packaging materials to reduce the amount of desorbed hydrogen after the seal, the use of hydrogen getter materials in hermetically sealed packages, and the use of barrier materials that do not contain the Pt/Ti or Pd/Ti structure. These solutions have limitations and possible instability problems that must be fully understood prior to implementation in high reliability systems.

Packaging Effects: The package serves to integrate all the components required for a system application in a manner that minimizes size, cost, mass and complexity. In doing so, the package must provide for mechanical support, protection from the environment, a stable thermal dissipation path, and electrical connection to other system components. For compound semiconductors, the package must satisfy all these characteristics and allow for reliable device performance over a wide range of conditions.

Understanding the packaging effects on the reliability of compound semiconductors is essential to attaining a reliable space system. In most applications, packaging of compound semiconductor devices is similar to that developed for silicon based technologies. However, the choice of packaging materials plays more of a critical role due to differences in the coefficient of thermal expansion. In addition, compound semiconductors are more fragile and may exhibit mechanical stresses causing device degradation and failure.

The stability and reliability of the die attach is largely determined by the ability of the structure to withstand the thermomechanical stress created by the difference in the Coefficient of Thermal Expansion (CTE) between the die and the packaging material. These stresses are concentrated at the interface between the die and the die-attach material and the interface between the die-attach material and the package[12]. The Coffin-Manson relation relates the number of thermal cycles a die attachment can withstand before failure:

$$Nf \propto \gamma^m \{2*t/L*\Delta CTE*\Delta T\}$$

Where;

γ = shear strain for failure
m = constant dependent on the material
L = diagonal length of the die
t = die-attach material thickness

The number of thermal cycles before failure can be significantly reduced by the presence of voids in the die attach material, since voids cause areas of concentrated localized stress which can lead to premature die delamination. In addition, voids cause localized heating which in turn causes an increase in the thermal resistance of the die attach material leading to device degradation and possible catastrophic failure.

Infrared imaging techniques can provide for a qualitative and sometimes a quantitative measure of the adequacy of the thermal path and a visual representation and mapping of possible void locations. Figure 8 shows a comparison of an optical and an Infrared image of the same die.

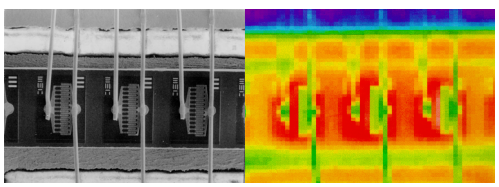

Figure 8. Optical(left) and IR image (Right) of the same die. The IR image shows thermal gradient and location of hot spots and possible void locations.

Radiation Effects: The use of microelectronic devices in both civilian and military spacecraft requires that these devices preserve their functionality in the hostile space environment throughout the mission life. An important feature of this environment is the presence of radiation of various types, including that from man-made sources. Unlike other aspects of reliability, radiation is unique and is not a requirement for nearly all other high-reliability applications, such as automotive, medical and terrestrial communications. Thus, because of the distinctive nature of the radiation environment, it is important to understand the effects of radiation on microelectronic devices and circuits used in space systems.

From the radiation point of view, the most important feature of GaAs is the lack of SiO_2 dielectric layers as gate insulators or as isolation insulators. In addition, the very high surface state densities typically found in the AlGaAs/GaAs system pin the Fermi level at the surface and effectively prevent radiation-induced surface inversion and its associated leakage currents from occurring. These differences result in GaAs devices being immune to total dose effects until very high doses are reached where the rare displacement damage events caused by Compton electrons formed from Co^{60} gamma rays finally have an effect. GaAs being a direct band gap material, leads to the minority carrier lifetimes in GaAs being much less than those for Si. Thus, more displacement damage is required to affect GaAs devices that depend on minority carrier lifetime for their successful operation. The best example of this is the increased radiation hardness of GaAs solar cells relative to Si solar cells. In addition, the ability to perform "band gap engineering" in which layers of various materials can be grown on each other with little change in lattice constant, provides increased flexibility in the case of III-V materials relative to Si [10].

Ionizing Radiation Effects: As noted above, GaAs devices in general are relatively immune to total dose effects resulting from the deposition of ionizing energy. This is due to the absence of an oxide that can trap charge and alter the operation of the device. Tests have shown immunity to total dose effects up to 100 Mrad (GaAs). In contrast with the relative immunity of GaAs devices to total-dose effects, transient, high-dose-rate pulses can severely affect these devices. GaAs devices and circuits are typically fabricated on semi-insulating GaAs substrates, which afford a natural isolation between individual transistors on the chip. However, in a transient radiation environment, this attractive feature becomes a liability because the transient photocurrents generated in the substrate are much larger than the transients generated elsewhere in the device as shown in Figure 9. In addition, if the semi-insulating substrate contains significant densities of deep traps, transient photo current effects can persist for a very long time.

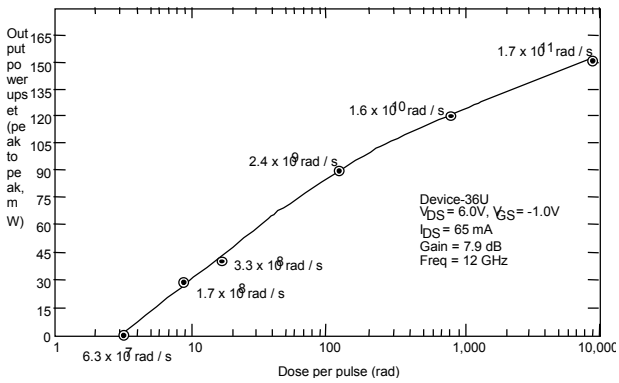

Figure 9. Response of MMIC amplifiers to transient electron pulses [14].

During the ionizing pulse, the large excess carrier densities that are generated in the semi-insulating substrate temporarily cause it to be a good conductor, allowing shunting of the transient photocurrent across transistor sources and drains. Under these conditions, upset levels in GaAs devices can be of the order of 10^{10} rad (GaAs)/s, or even less. Fortunately, these effects can be minimized by properly placing bonding pads and metal interconnects, and using various types of blocking layers [11].

Displacement Damage Effects: As pointed out earlier, GaAs devices are relatively insensitive to displacement damage effects when compared to Si devices. Generally, this is due to the shorter minority carrier lifetimes and higher doping levels found in GaAs devices and circuits. Since displacement damage introduction into the semiconductor material reduces the minority carrier lifetime, the mobility, and the carrier concentration, device properties that depend on these parameters will be affected by displacement damage. Generally, the longer the lifetime, the higher the mobility, and the smaller the carrier concentration the more effective displacement damage is in altering these parameters. Thus, semiconductor devices with short lifetimes, low mobility, and high carrier concentrations will be relatively immune to displacement damage effects. GaAs has the characteristics of short lifetimes and high mobility. Therefore, we can expect GaAs device to suffer from reduction in mobility and carrier concentration as a result of displacement damage. Note, however, that greater amounts of displacement damage are usually required to cause carrier removal and mobility degradation.

Single Event Effects: Studies of charge collection in GaAs devices have shown the charge generated by a single particle can be collected by a greater variety of mechanisms than in Si devices. In GaAs MESFETs, the collection from deep within the device is limited because the recombination rate in GaAs is high and because the diffusion length is short due to small minority carrier lifetimes. However, relative to Si, this is offset by the fact that more regions of the device are sensitive than in the case of a Si MOSFET. In a GaAs MESFET, the source and drain regions are sensitive to upset as well as the gate region. Collection mechanisms for the various regions in the device are shown in Figure 10 and include a back channel turn-on mechanism, a bipolar source-drain collection mechanism, and an ion shunt mechanism. Fortunately, as in the case of photocurrent transients mentioned above, "band gap engineering" through the deposition of various blocking layers can minimize single event effects.

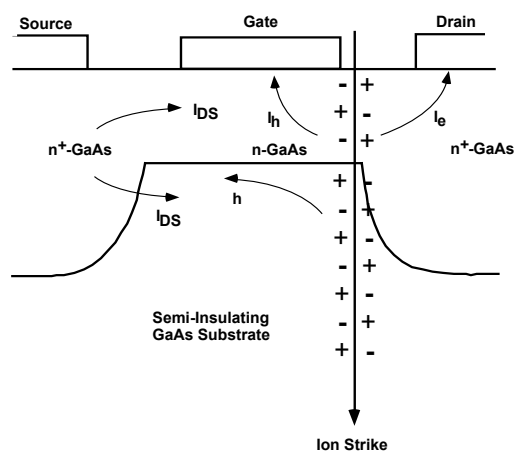

Figure 10. Single-particel-induced charge collection mechanisms in a GaAs MESFET [15].

Summary

The reliability and application of compound semiconductor devices in high reliability space systems requires a thorough understanding of the technology's reliability issues, failure mechanisms, relevance to the application, and methods for risk mitigation and qualification. Failure mechanisms related to materials, processes, environments and application of the devices should be considered. Also, an understanding of the effects of the radiation environment and the implementation of a

meaningful qualification program is essential to assure successful insertion of this technology.

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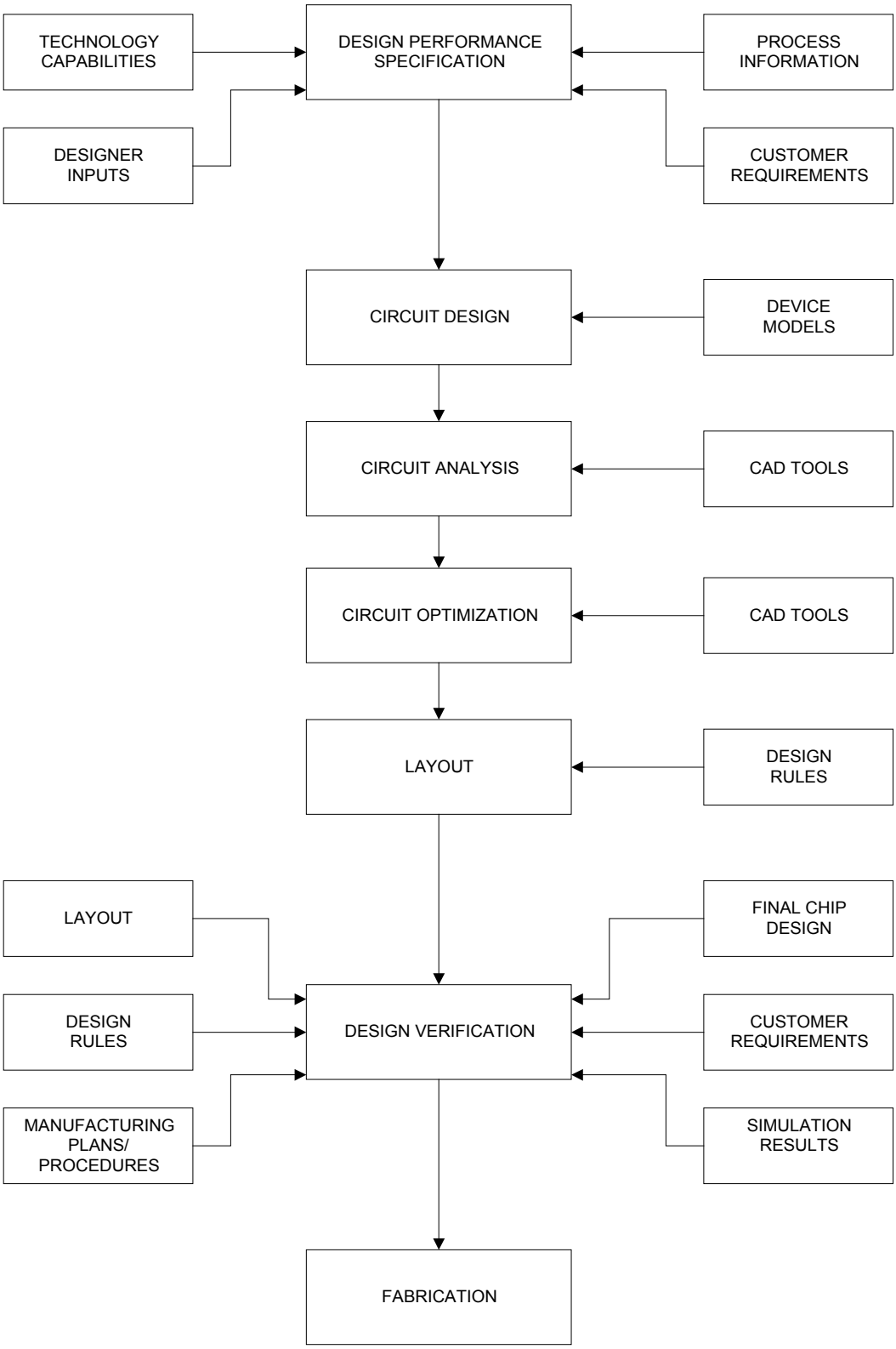

Figure 1. Typical Design Flow

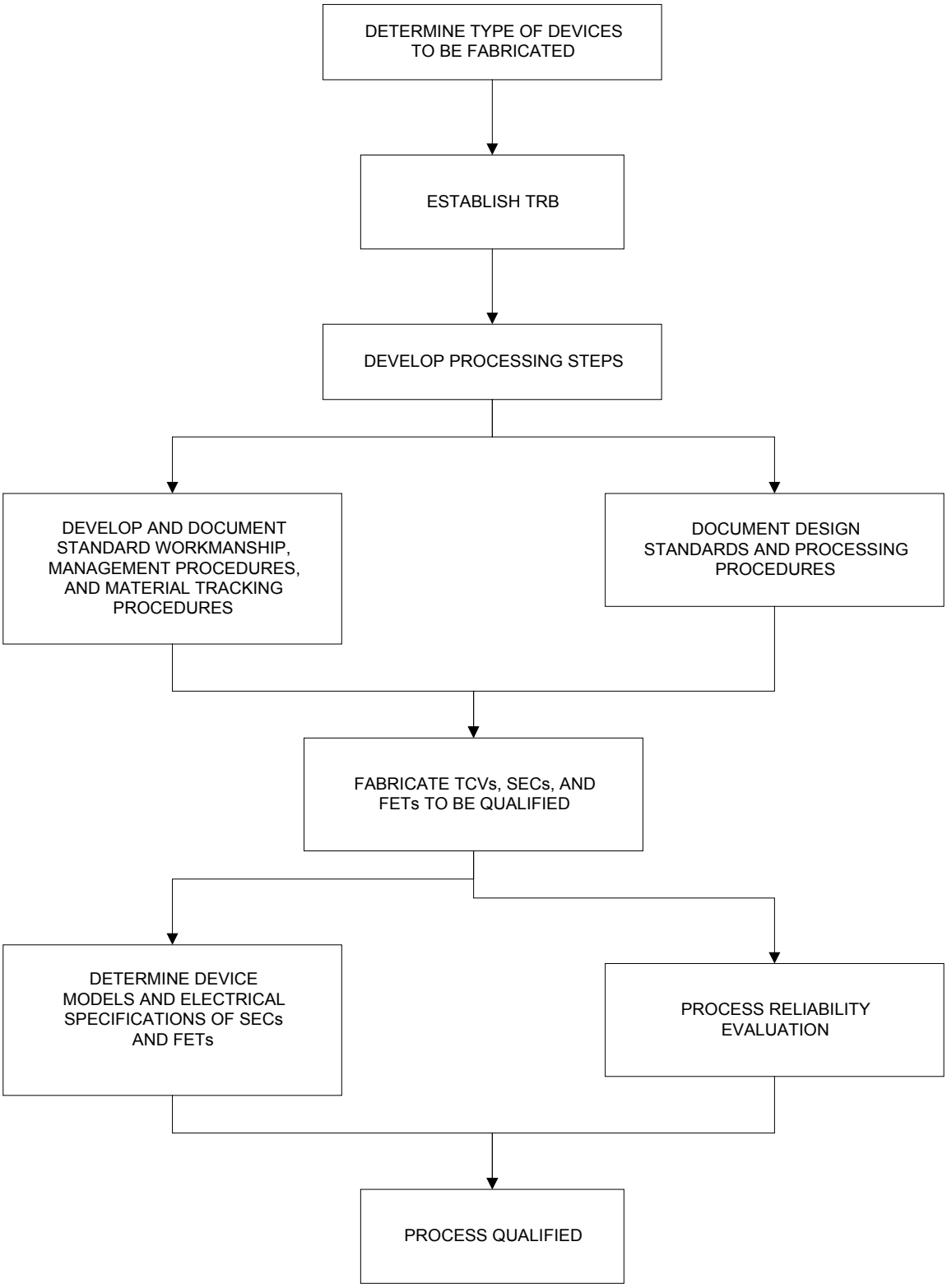

Figure 2. Typical Process Qualification

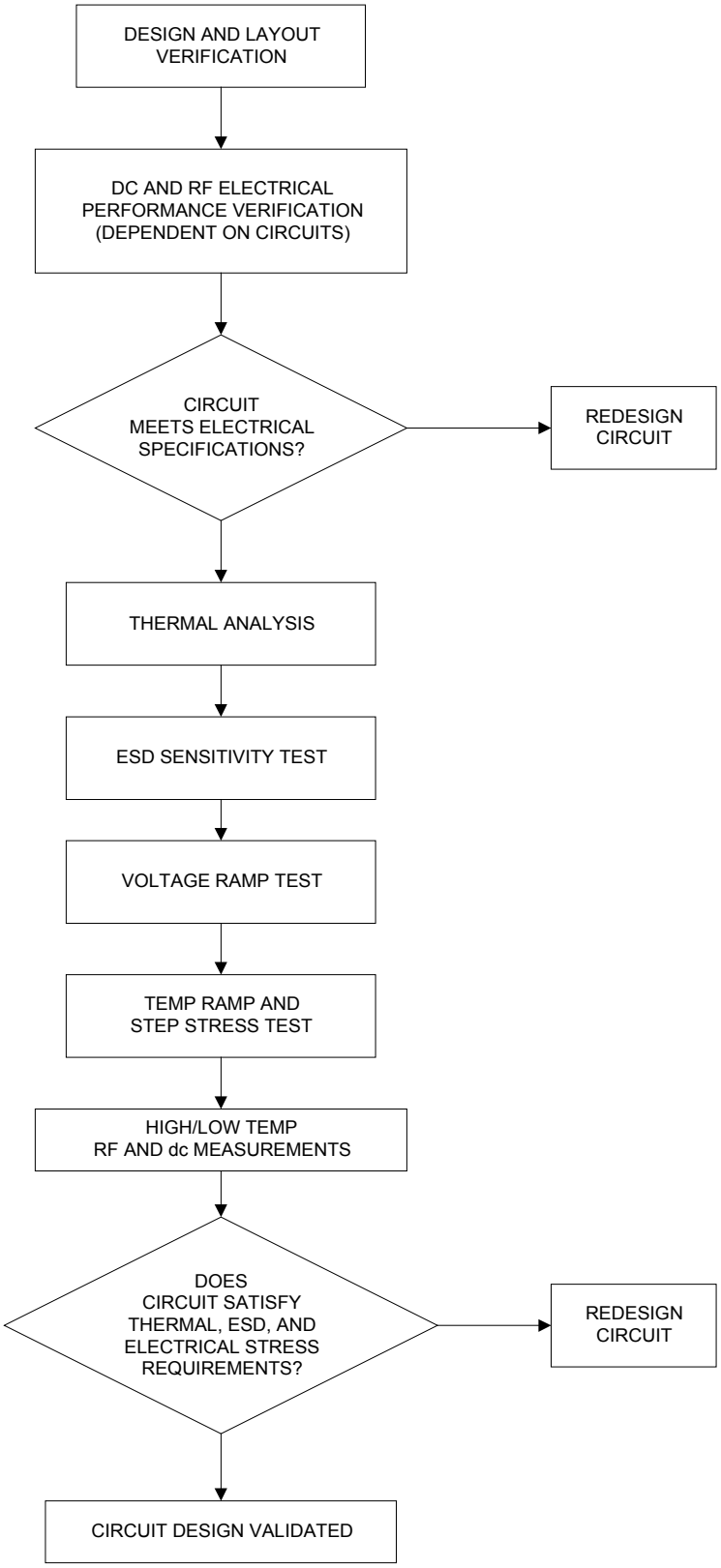

Figure 3. Typical Design Validation Flow