Space Radiation Effects on Microelectronics

Presented by the Radiation Effects Group

Section 514
Sammy Kayali, Section Manager

Radiation Effects in Space

Radiation Is a Discriminating Environment for JPL Missions

Dealing with Potential Radiation Problems Is Critical for Mission Success

- Complex problem, made worse by evolving technology
- Past mission performance illustrates how JPL can be successful in space
- Learning from previous mistakes and oversights is also important

This Course Is Intended to Increase Awareness of Radiation Issues

- Attended by designers and spacecraft operational personnel
- Limited in scope
  - Not intended to make everyone an expert
  - Provides basic information and points of contact

Examples of Radiation Problems in Spacecraft

Special Redesign of 2901 Microprocessor for Galileo

- Problem identified during design and evaluation
- Potential “show stopper” for Galileo mission

Resets in Hubble Space Telescope after Upgrade in 1996

- Caused by transients from optocouplers
- Occurred when spacecraft flew through South Atlantic anomaly

Failures of Optocouplers on Topex-Poseidon

Resets in Power Control Modules on Cassini

High Multiple-Bit Error Rate in Cassini Solid-State Recorder

Available Resources at JPL

Laboratory Facilities and Test Technology

- Cobalt-60 test cell
- Frequent off-site tests at accelerators

Experienced, Knowledgeable Personnel

- Aware of project needs
- Continual evaluation and modeling of new technologies

RADATA Data Base

Reports and Technical Papers

Key Contacts for Radiation Effects Issues

Allan Johnston, Acting Group Supervisor

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Course Outline

Introduction

Overview of Radiation Environments

Recoverable Single-Event Upset Effects

Non-Recoverable Single-Event Upset Effect

Total Dose Effects

Displacement Damage and Special Issues for Optoelectronics

Summary

Section II: Overview of Radiation Environments

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Radiation Environments

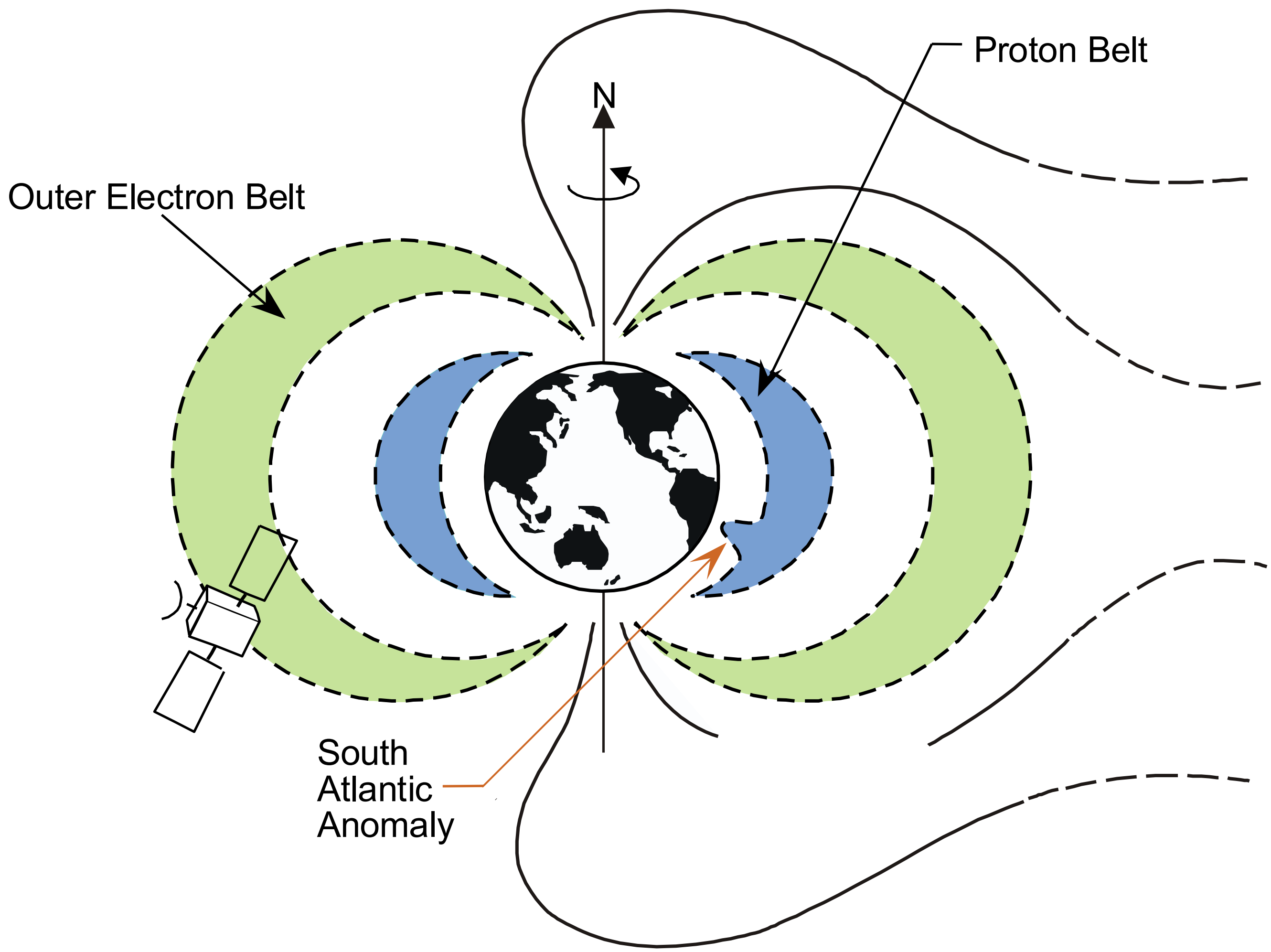
Energetic Particles Causing Single-Event Upset

- Galactic cosmic rays
- Cosmic solar particles (heavily influenced by solar flares)
- Trapped protons in radiation belts

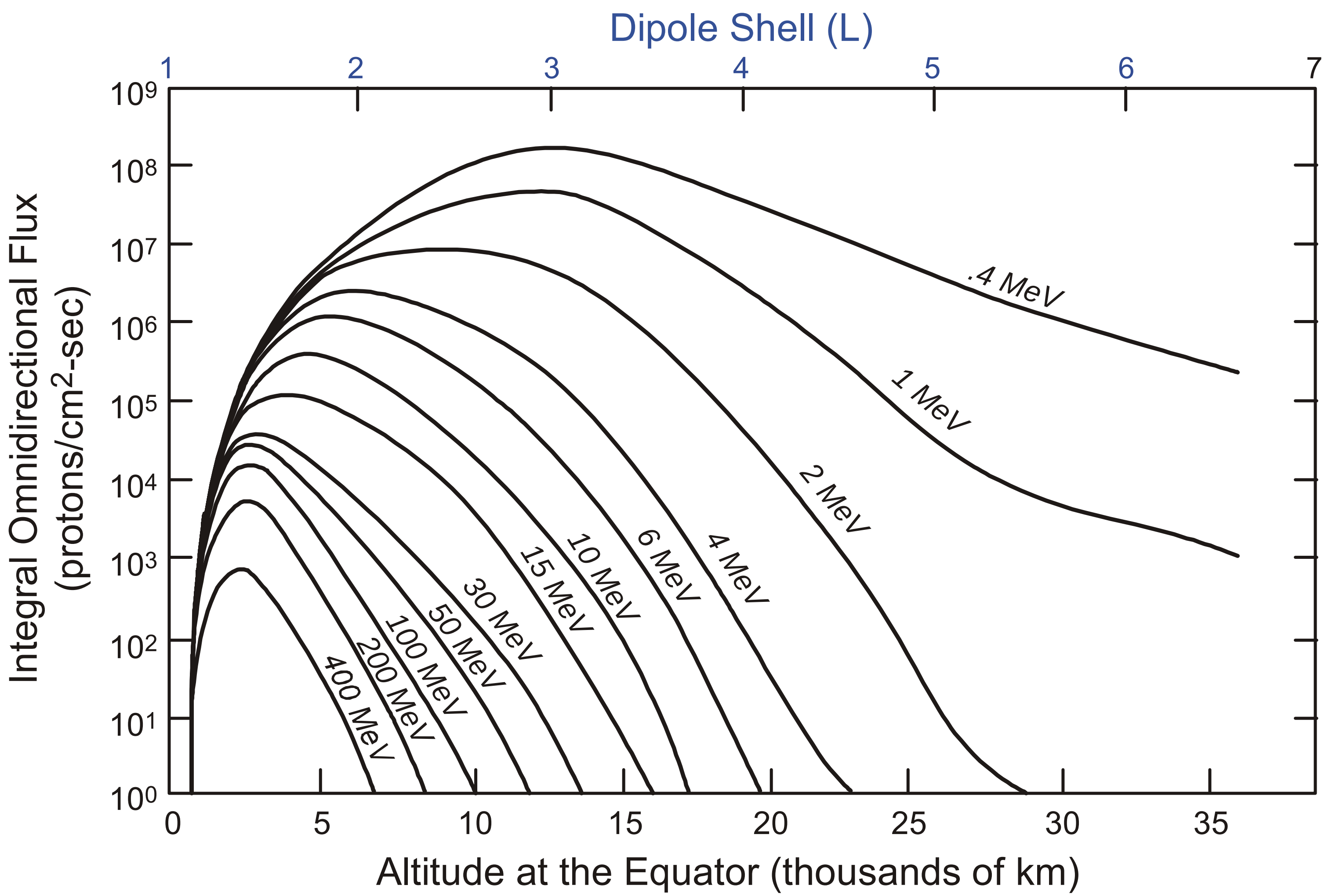
Radiation Causing “Global” Radiation Damage

- Trapped protons in radiation belts
- Trapped electrons in radiation belts
- Protons from solar flares

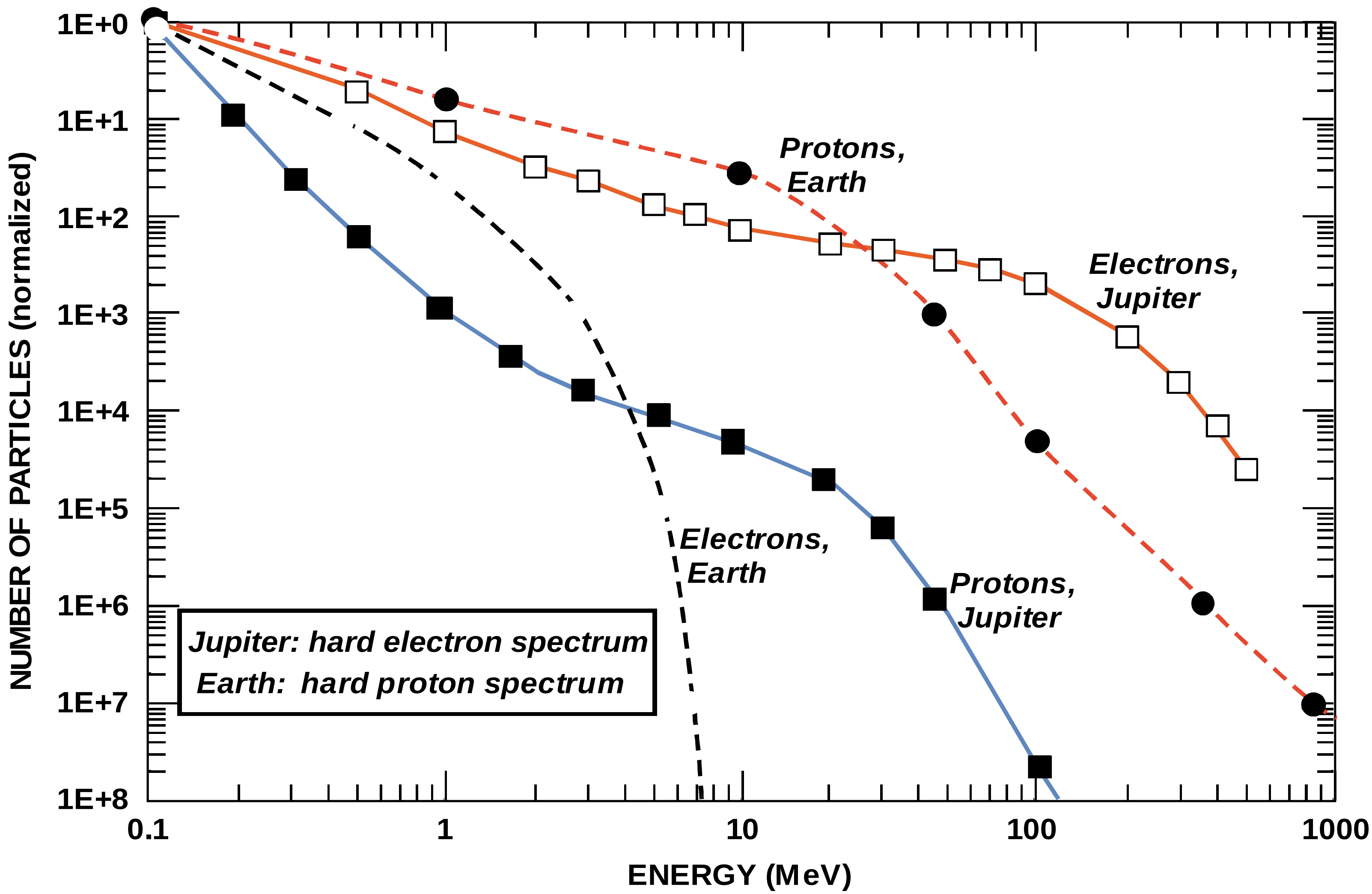
Trapped Radiation Belts around Earth



Energy Distribution in the Earth's Proton Belt



Trapped Belt Energy Distributions on Jupiter and Earth



Space Systems at JPL

Interplanetary Missions

- Jupiter and Saturn
  - Intense radiation belts
  - Very high radiation levels [> 1 Mrad(Si)]
- Mars Missions
  - Orbiters
  - Landers
- Asteroids, Comets and Solar Probes

Earth Orbiting Missions

- Typical radiation levels < 20 krad(Si)
  - Depends on altitude and inclination
  - Affected by south Atlantic anomaly
- Less margin between specified radiation environment and reality

Solar Flares

Solar Cycle Has Eleven-Year Periodicity

Solar Flares Produce Heavy Ions and Protons

- Heavy ion spectrum is less energetic than galactic cosmic ray spectrum
- Protons from solar flares are important for earth orbiting and deep space programs
  - Protons from a single flare produce fluences up to ~ 2×10^{10} p/cm^2
  - Shielding can be effective for lower energies

Solar Flare Intensity Varies Over a Wide Range

- JPL "design-case" flare usually used for specifications
- Many systems never experience a large flare

Mechanisms for Global Permanent Damage

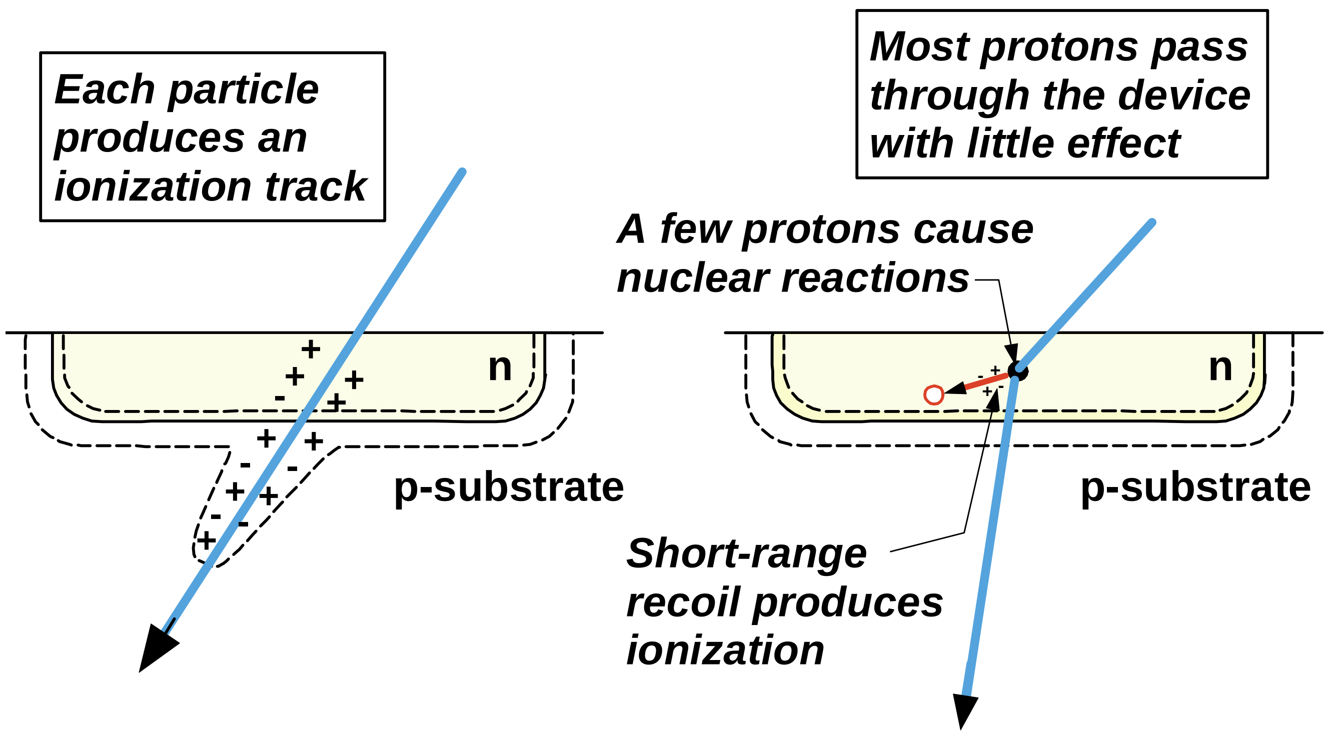
Electrons and Protons Produce Ionization in Semiconductors

- Ionization excites carriers from conduction to valence band
- Charge is trapped at interface regions
- Units: rad(material) *1 rad = 100 ergs/g of material*
- Depends on bias conditions and device technology
- Typical effect: threshold shift in MOS transistors

Displacement Damage Also Occurs

- "Collision" between incoming particle and lattice atom
- Lattice atom is moved out of normal position
- Degrades minority carrier lifetime
- Typical effect: degradation of gain and leakage current in bipolar transistors

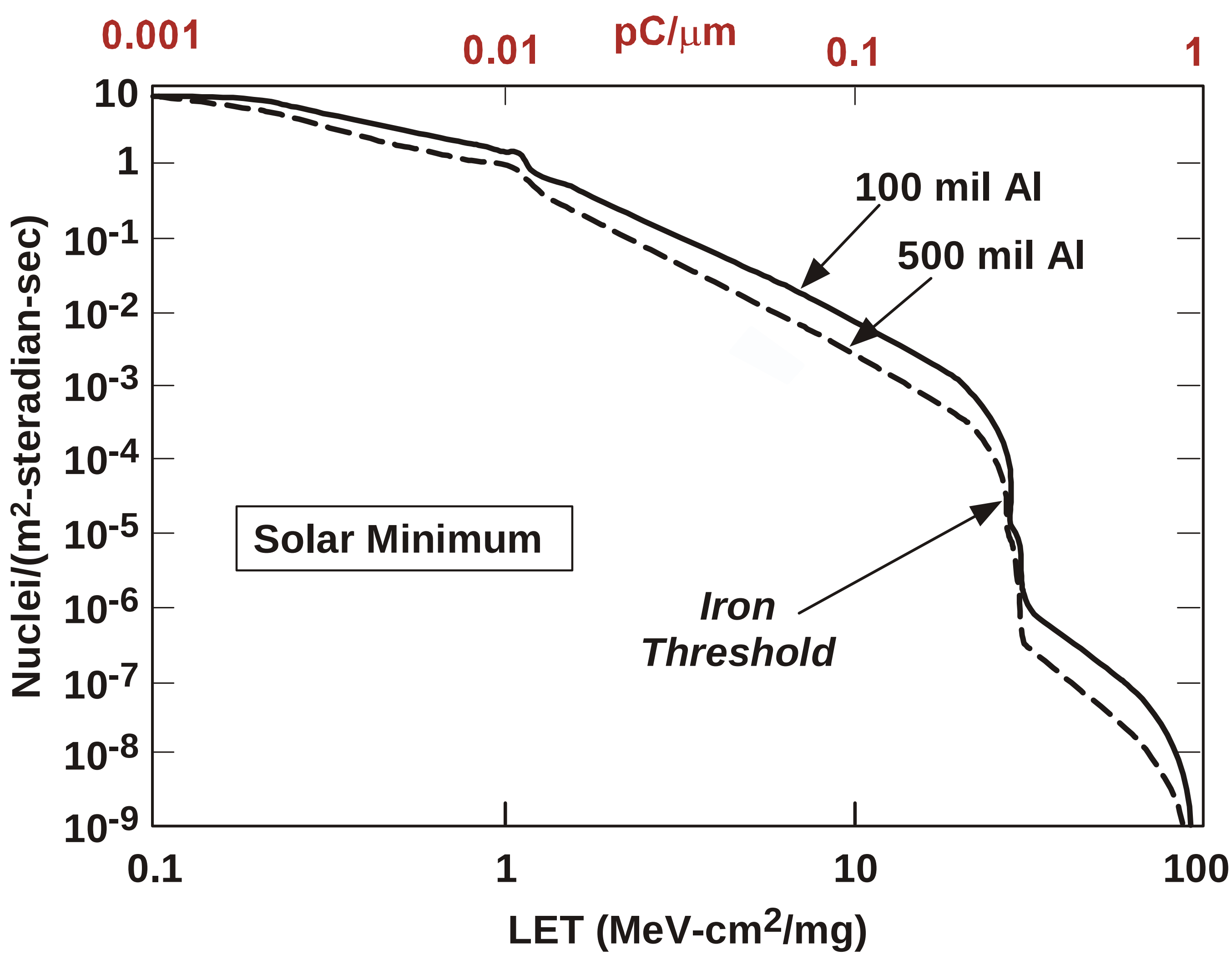
Mechanisms for Heavy Ion and Proton SEU Effects



a) Heavy Ions *(ionization by each particle)*

b) Protons *(nuclear reaction needed to produce recoil)*

Integral Cosmic Ray Spectra



SEE Sensitivity Benchmarks

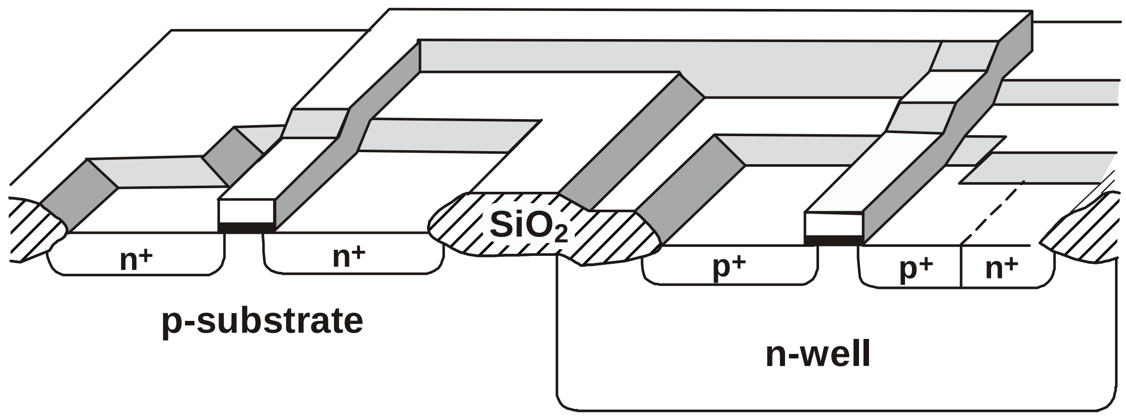
Heavy Ion Susceptibility

- Spectrum falls sharply above 30 MeV-cm^2/mg
- Effective threshold for concern is much higher, 75 MeV-cm^2/mg
  - Charge produced by ions depends on total path length
  - Increases as $1/(\cos \theta)$

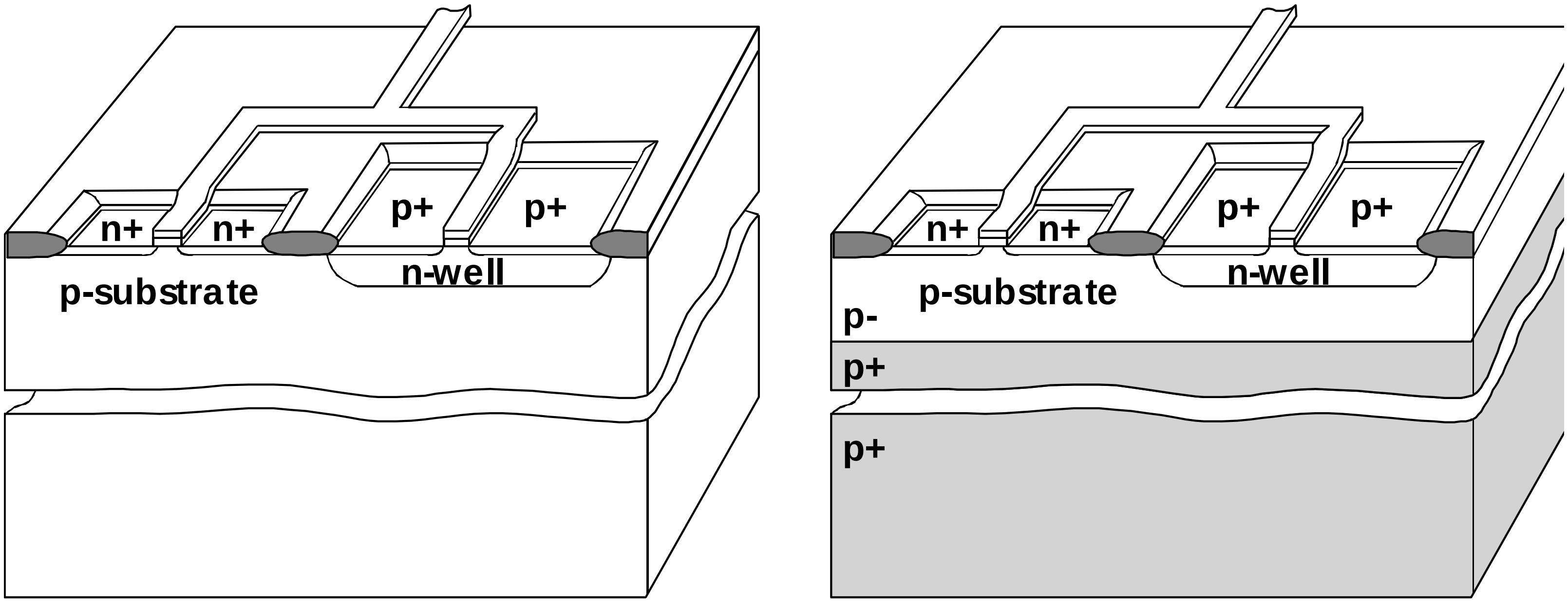
Proton Susceptibility

- Proton upset is possible for devices with $LET_{th} < 15$ MeV-cm^2/mg
- Proton testing should be done for all devices with thresholds below that level

CMOS Technology

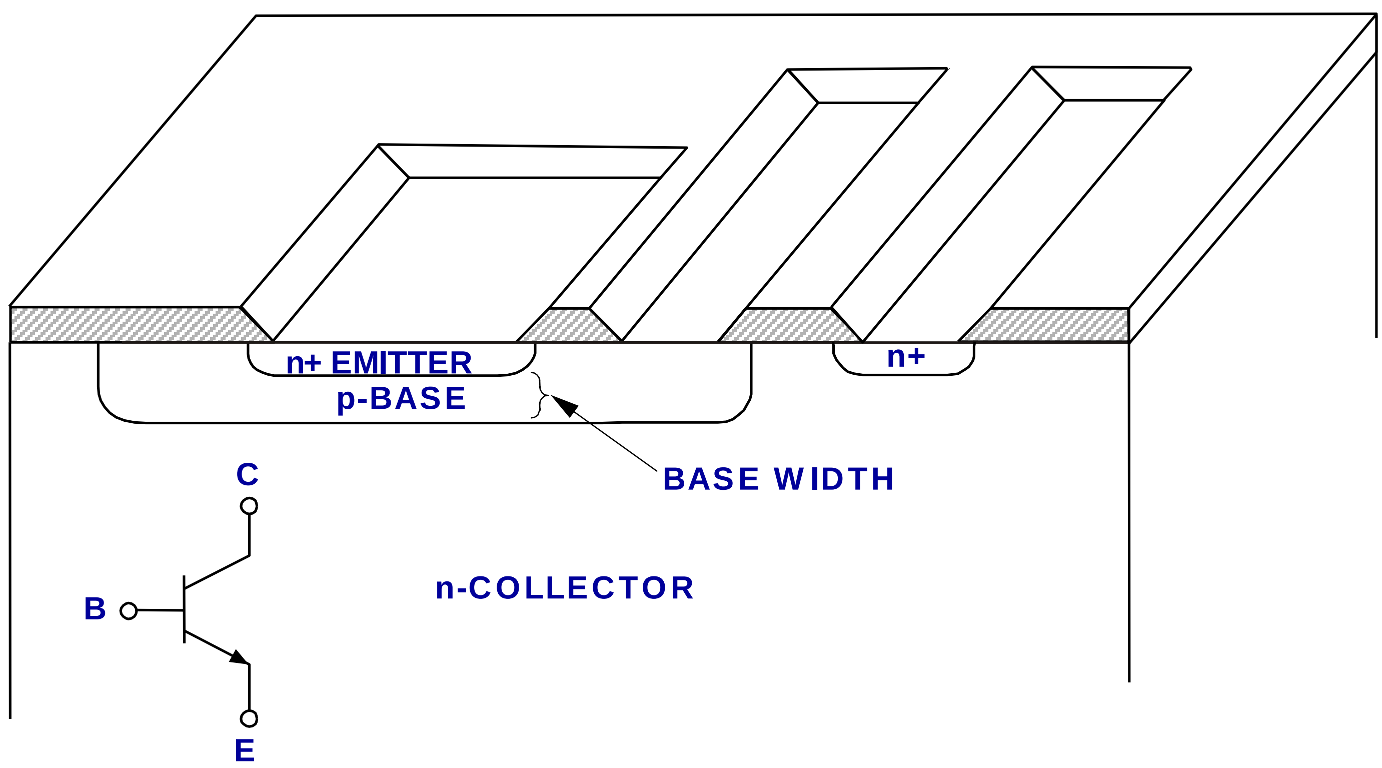


Bulk and Epitaxial Substrates



Bipolar Technology

Structure of a bipolar transistor



Section III: Recoverable SEU Effects

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SEE Effects in Operational Spacecraft

“Safehold” Condition in DS-1 Shortly after Launch

Multiple-Bit Errors in Cassini Solid-State Recorder

- Occurred even though extensive testing was done during design phase
- Attributed to system architectural flaw

Inadvertent Switching of Cassini Power Modules to Standby Mode

- Caused by transients from PM139 comparator
- Low probability because of high input voltage used in design

Single-Event Upset

First Observed in Bipolar Flip-Flops in 1979

- Original work treated with skepticism
- SEU has emerged as one of the major issues for application of microelectronics in space

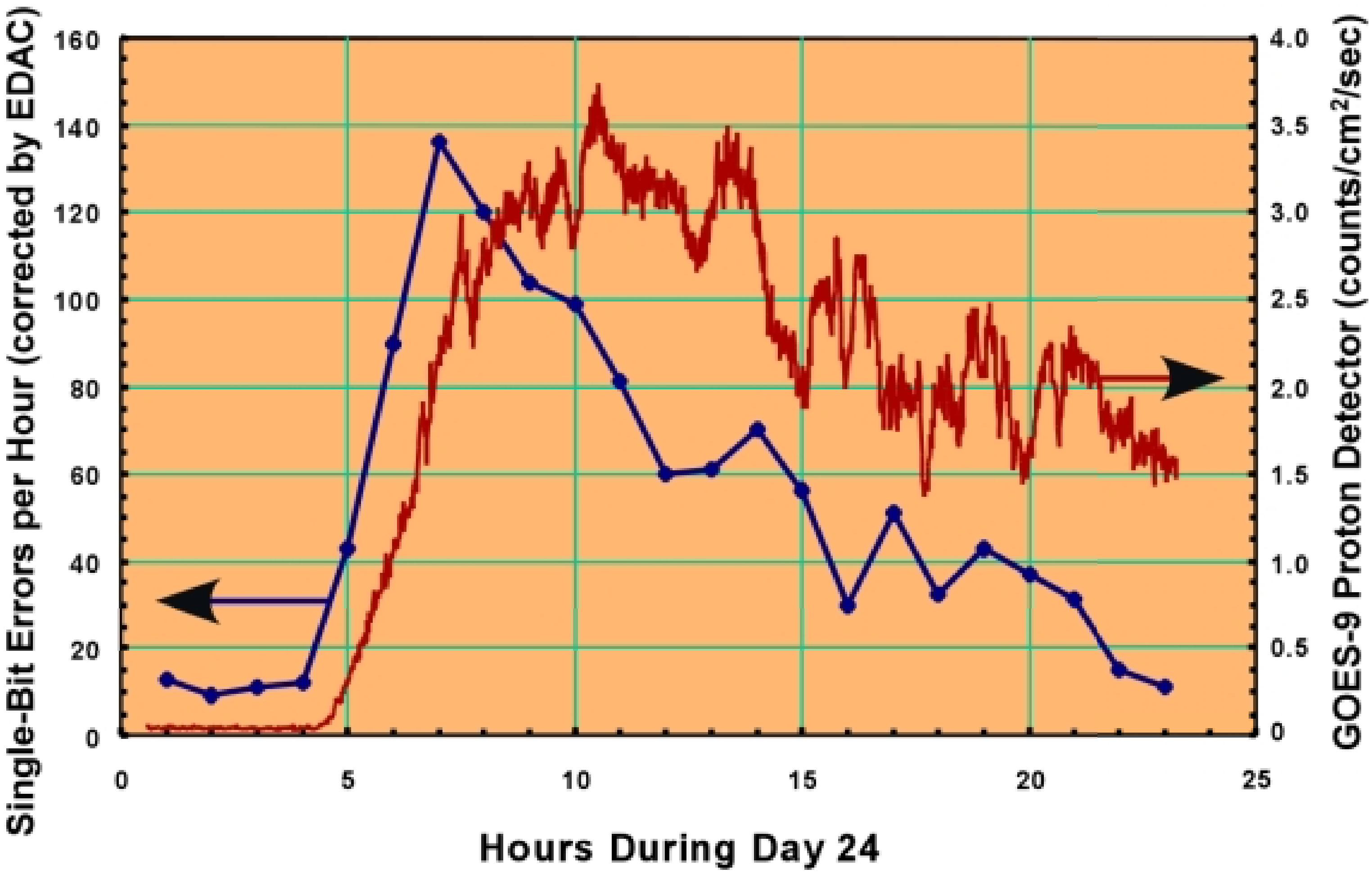
Previous JPL Missions Have Struggled with SEU Problems

- Galileo used a 2901 bit-slice microprocessor (bipolar technology)
- Initial testing showed SEU susceptibility, at moderate rate
- Subsequent die design changes increased the SEU rate beyond the point where the device was useable
- Sandia National Laboratory designed a special rad-hard CMOS version that was used on the spacecraft

SEU Effects Have Become Worse as Devices Have Evolved

- Lower “critical charge” because of small device dimensions
- Large numbers of transistors per chip and overall complexity

Cassini SSR Errors During Solar Flare



Overview

How storage elements are upset
- SRAM
- DRAM

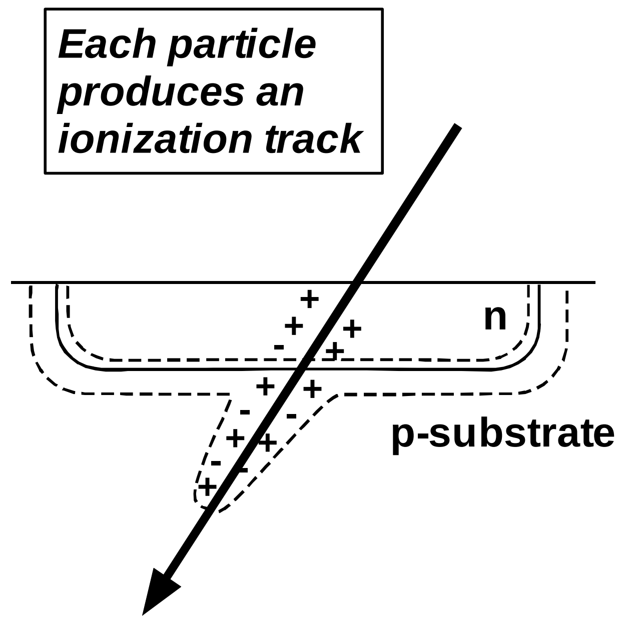
What are “cross-section” and “L.E.T.”

How space upset rates are calculated

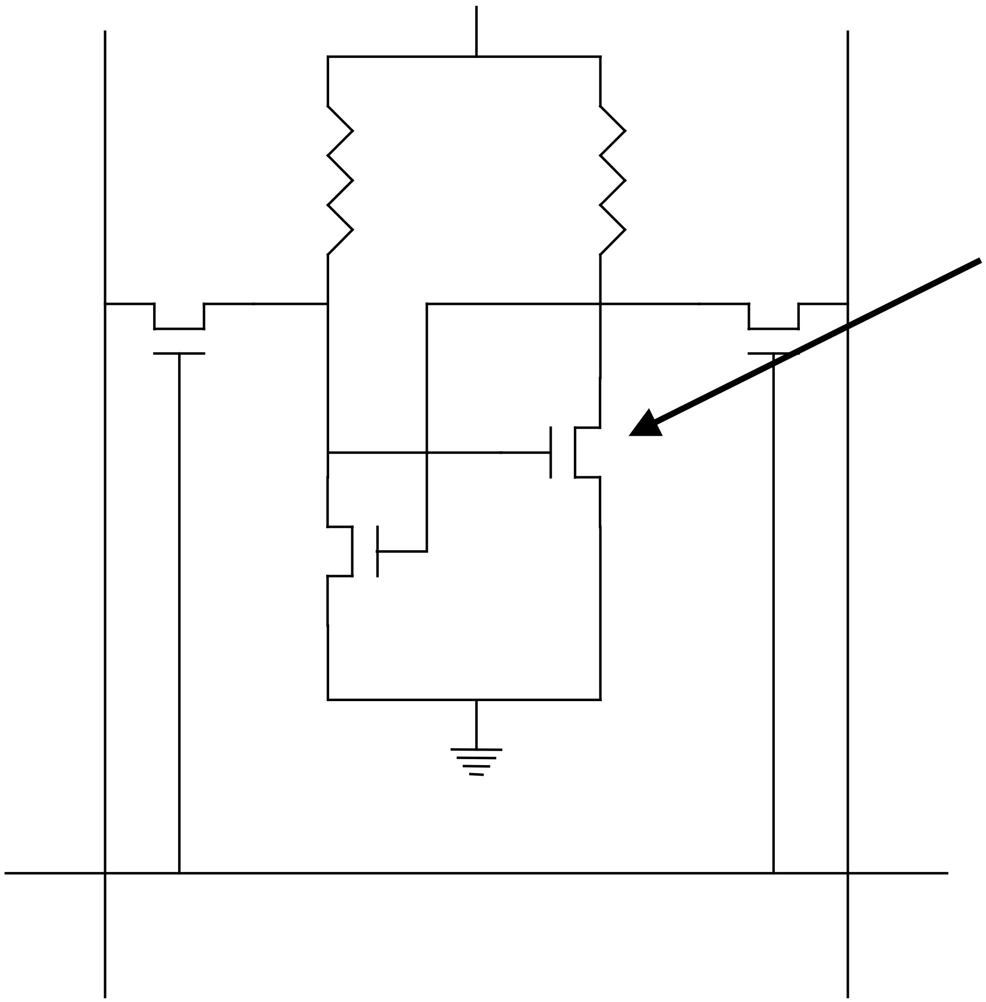
Upset mitigation techniques

Other effects
- SEFI
- Transients

Ion Strike on a p-n Junction



How an SRAM Cell Upsets



Ion strike on or near transistor will change bit state

What is LET?

Measure of energy deposition in a material

- for example: silicon

Linear Energy Transfer

Units are MeV per mg/cm^2 (energy per areal density)

Proportional to MeV/μ or pC/μ

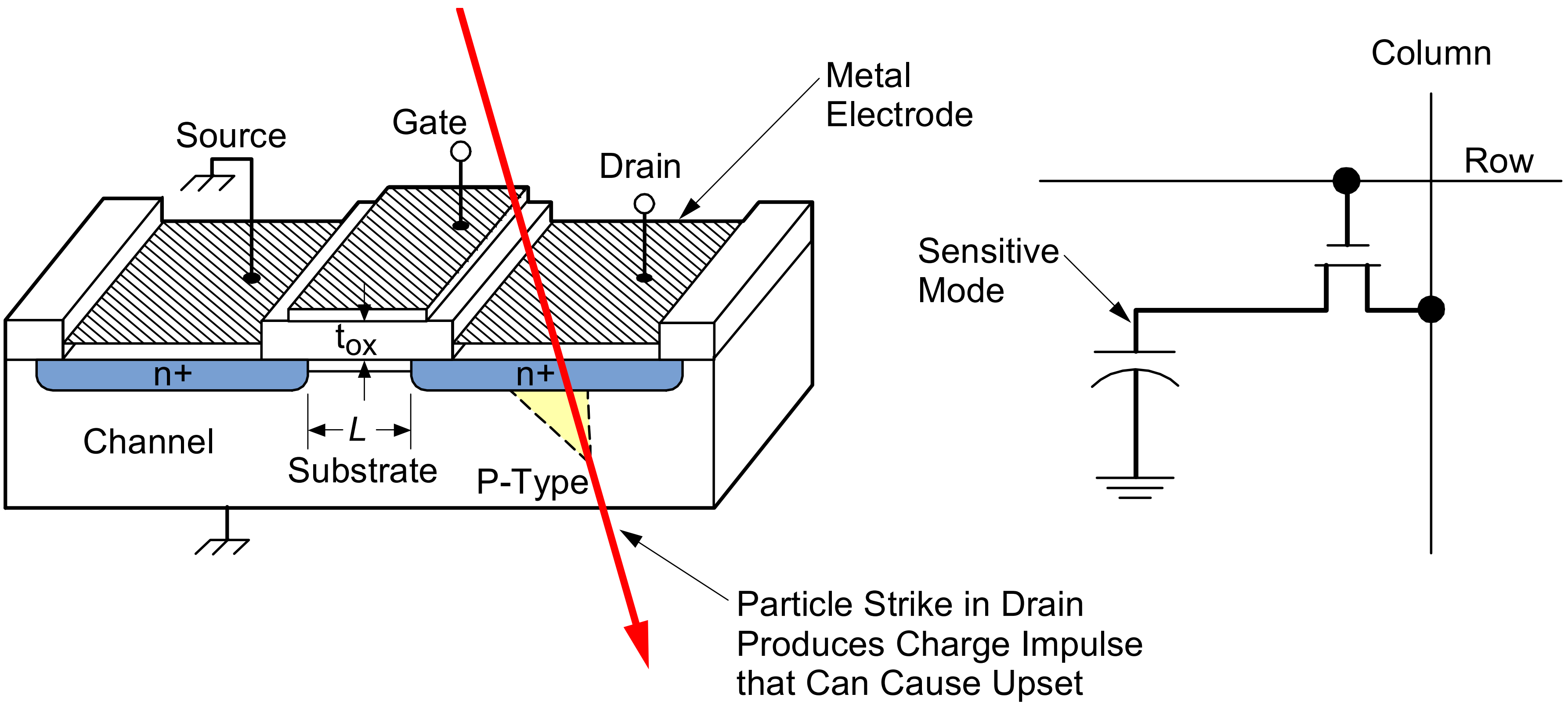
What is Cross Section?

Measure Of Susceptibility

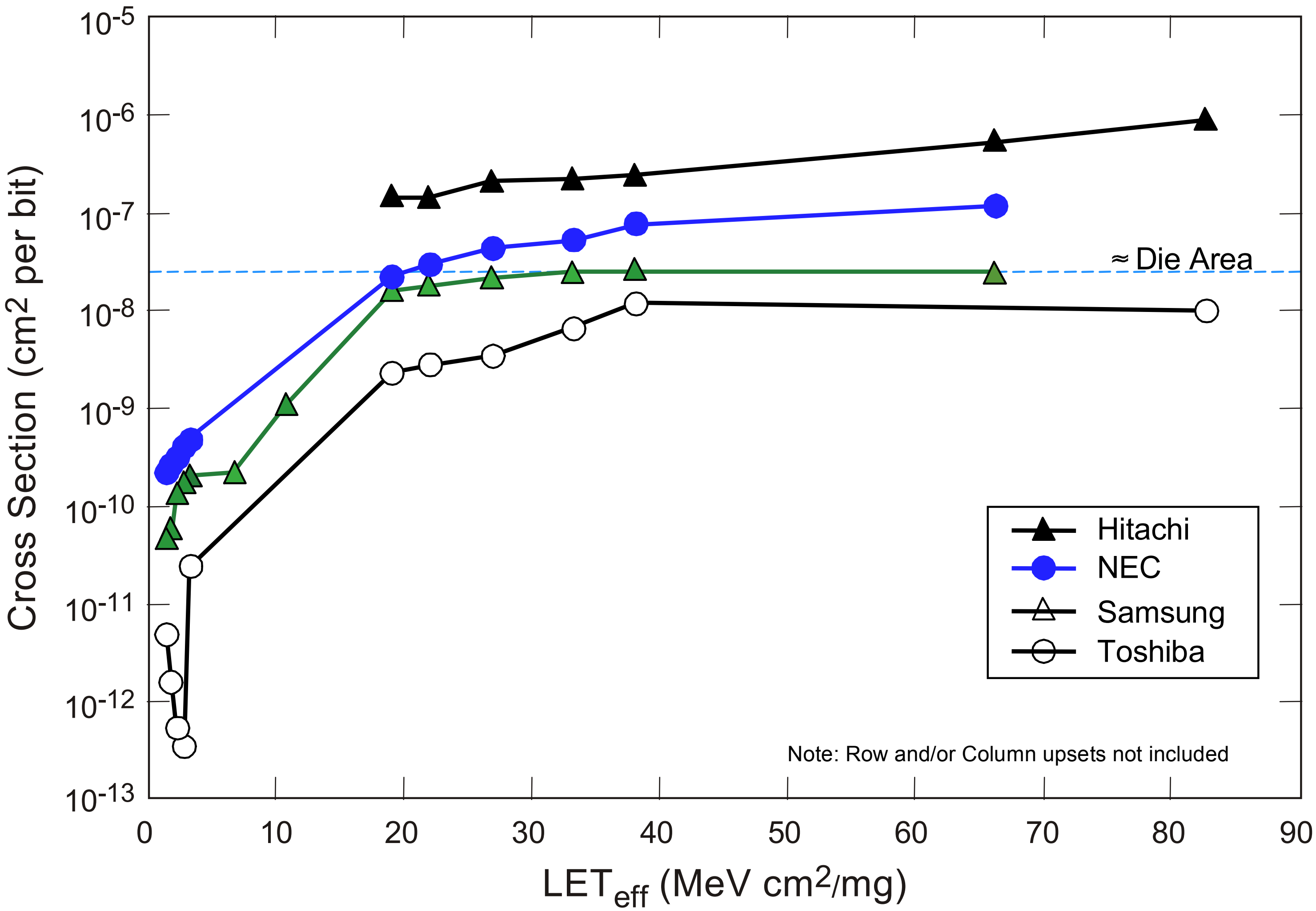
Units = area (cm^2 or μ^2)

Dart Board Analogy

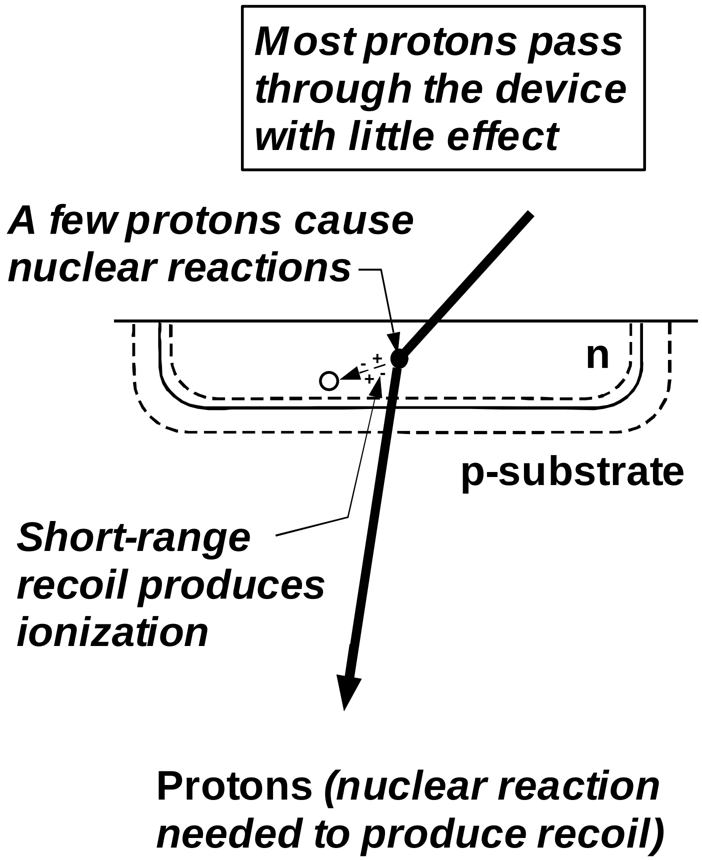
Upset Mechanism for DRAMs



Single-Event Upset in 64-Mb DRAMs



Proton Reaction in a p-n Junction



Upset from Protons

Proton LET Is Extremely Low

- Proton upset is usually dominated by nuclear reactions
- Secondary reaction products have much higher LET, but have short ranges compared to galactic cosmic rays

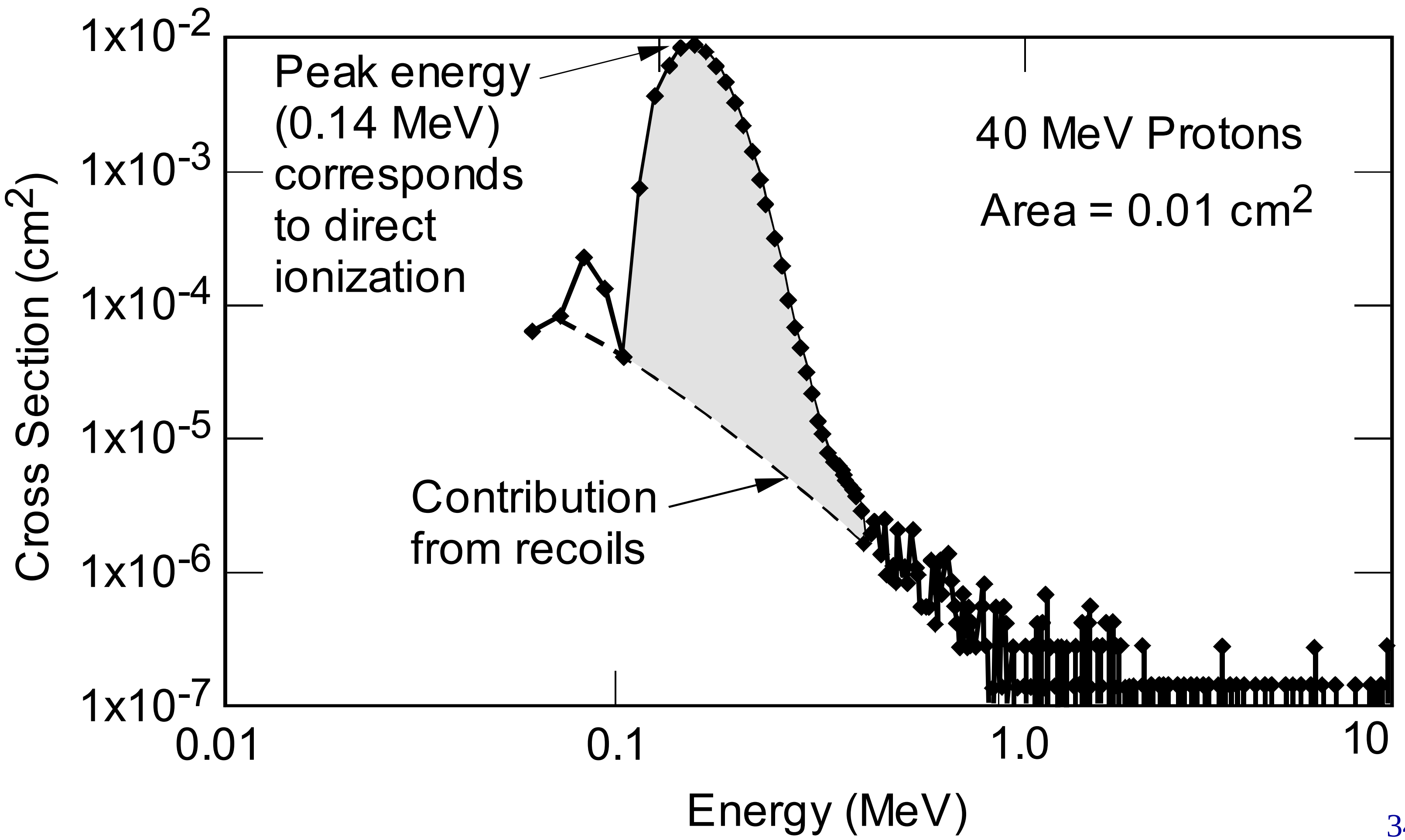
Proton Testing Provides only Limited Information about SEE Sensitivity

- "Effective" LET of protons is 3-12 MeV-cm^2/mg
- Depends on device construction

Significance of Proton Upset

- Important because protons can make a large contribution to the overall upset rate (particularly for low earth orbits)
- Proton testing is cheaper and easier than tests with heavy ions
- In many cases proton test data may be the only available information

Proton Recoil Distribution in a Surface Barrier Detector that Is 50 μm Thick



How Space Upset Rates Are Calculated

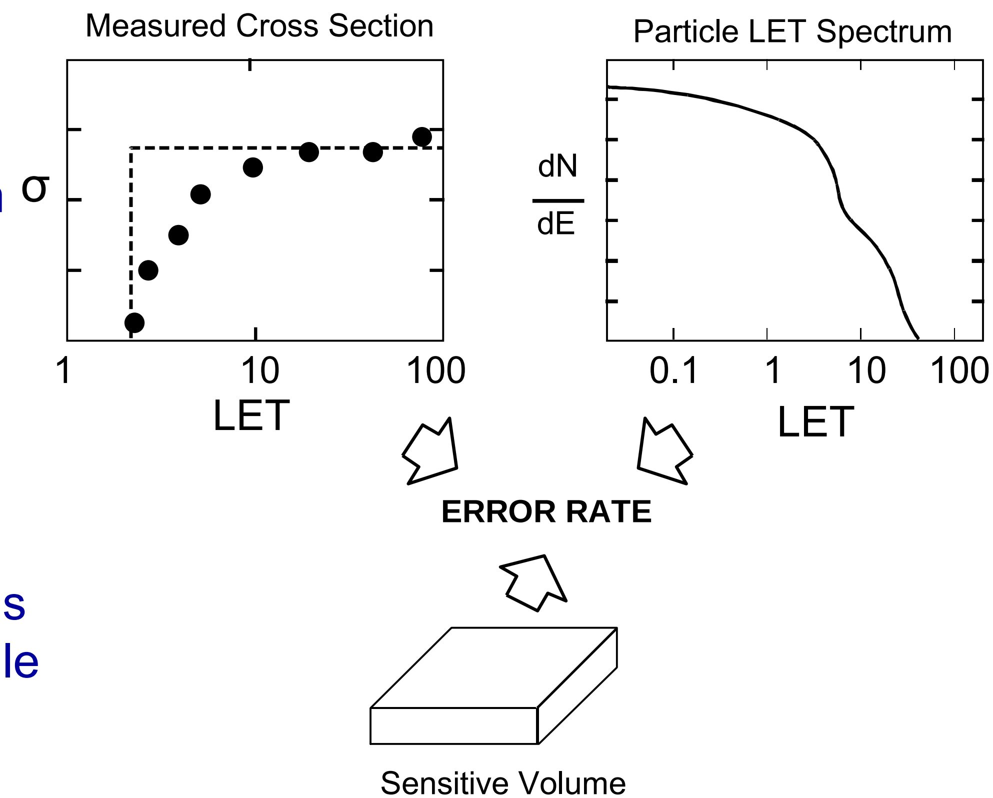
Measure σ vs. LET

- Testing done at high-energy accelerator
- Cross-section determined from circuit response

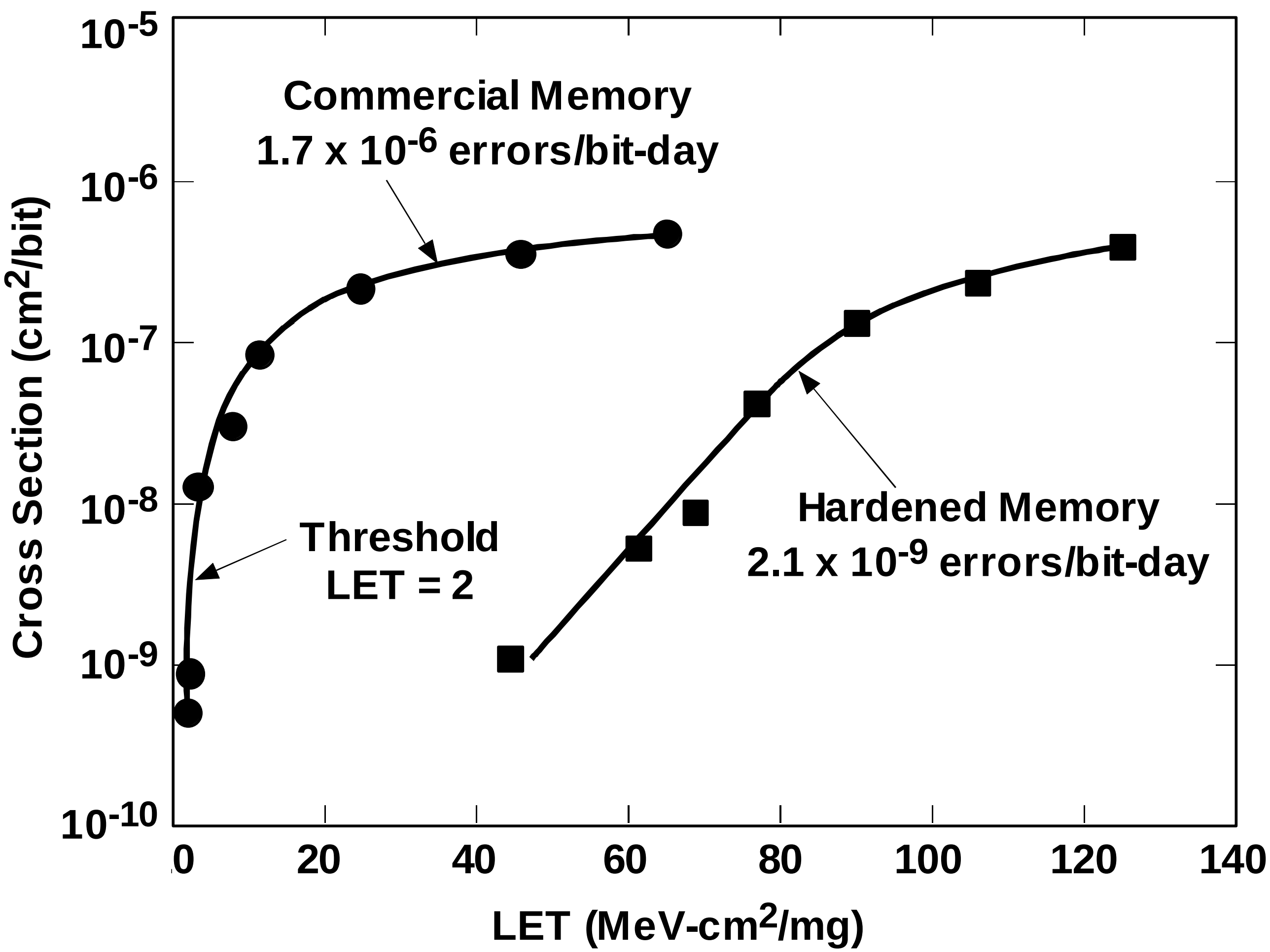
Determine Sensitive Volume

- Requires assumptions about device construction
- Used to determine effect of ions that strike the device at an angle

Integrate with LET Spectrum

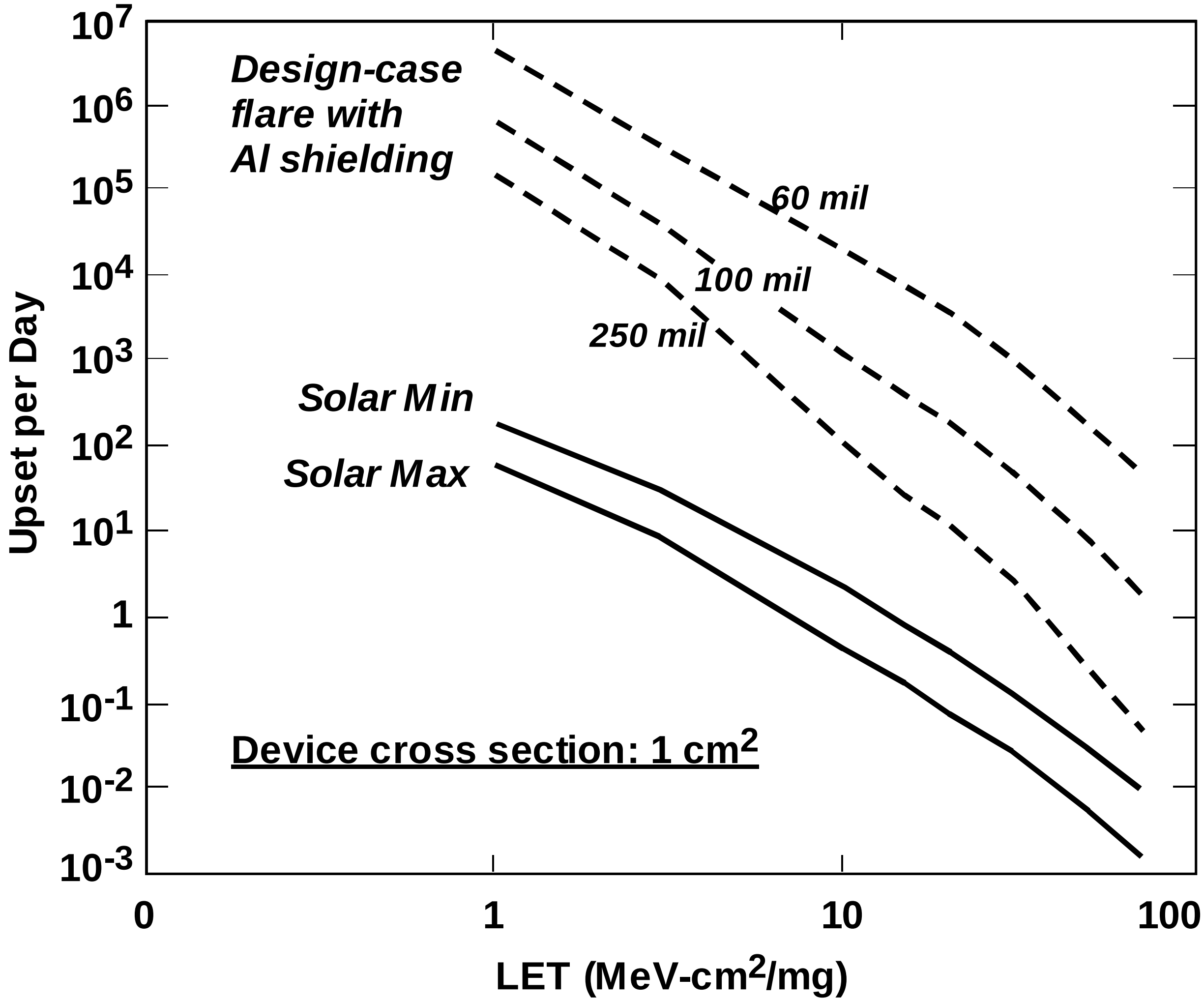


Dependence of Cross Section on Stopping Power

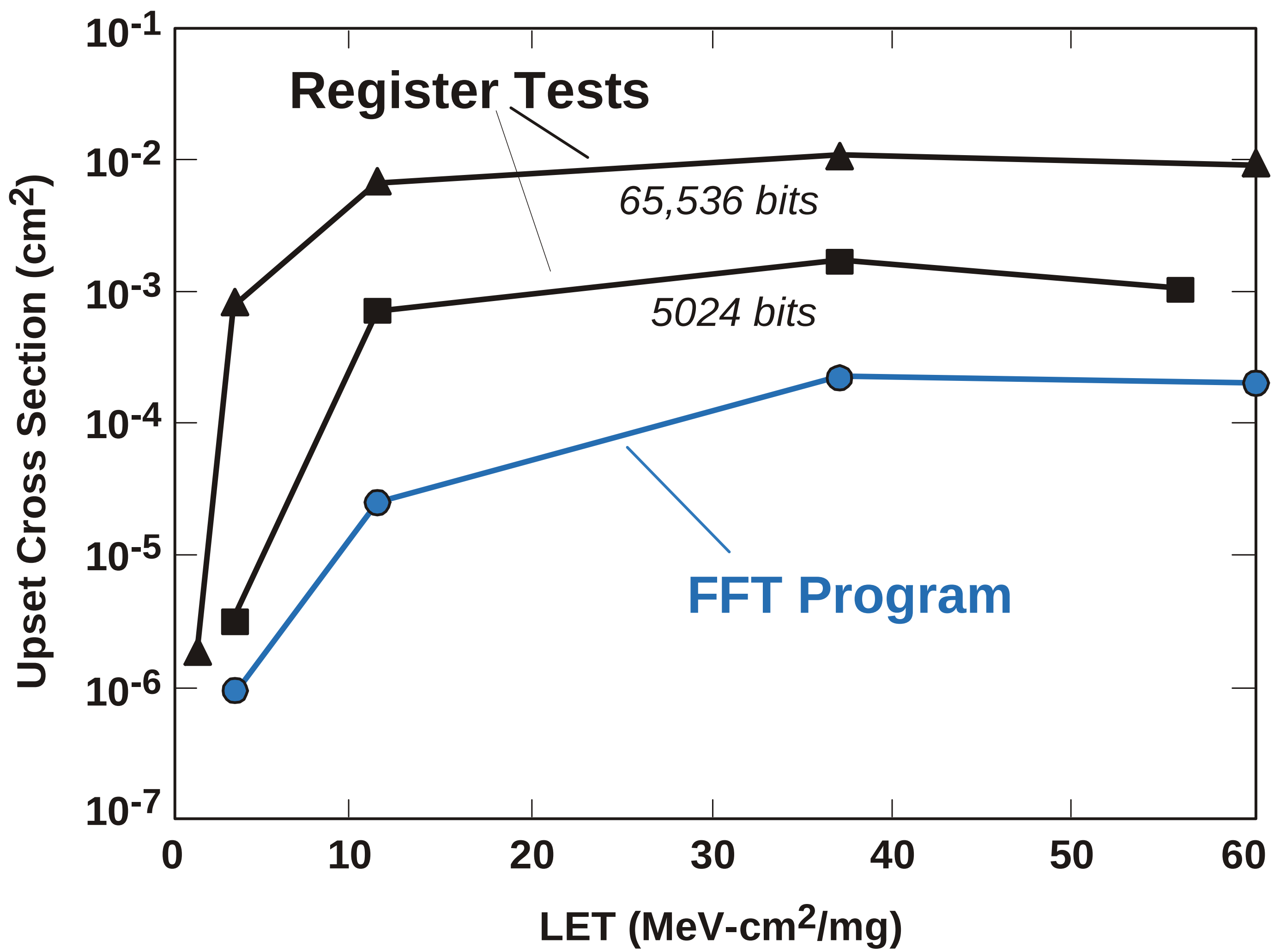


SEU Rates

(Interplanetary Space)



Dependence of PC603e Cross Section on Test Method



Hamming Codes

"SECDED" = Single Error Correction
Double error Detection
- example: (39, 32) = 32 data bits + 7 parity

"DECTED" = Double Error Correction
Triple Error Detection
- example: (79, 64) = 64 data bits + 15 parity

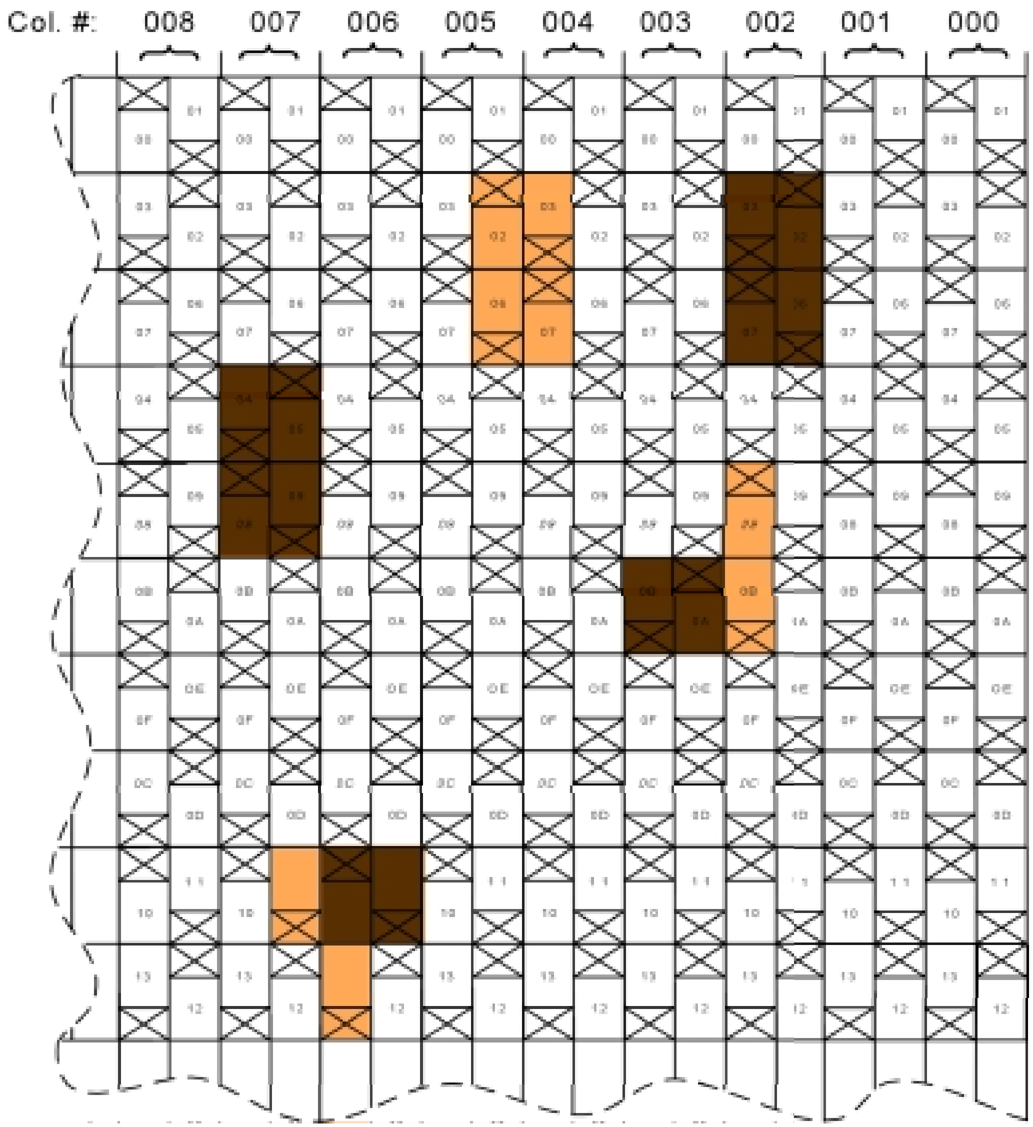
EDAC word error rate is approximately one half of:

$$\frac{T_{scrub}}{N_{EDAC}} \quad U^2$$

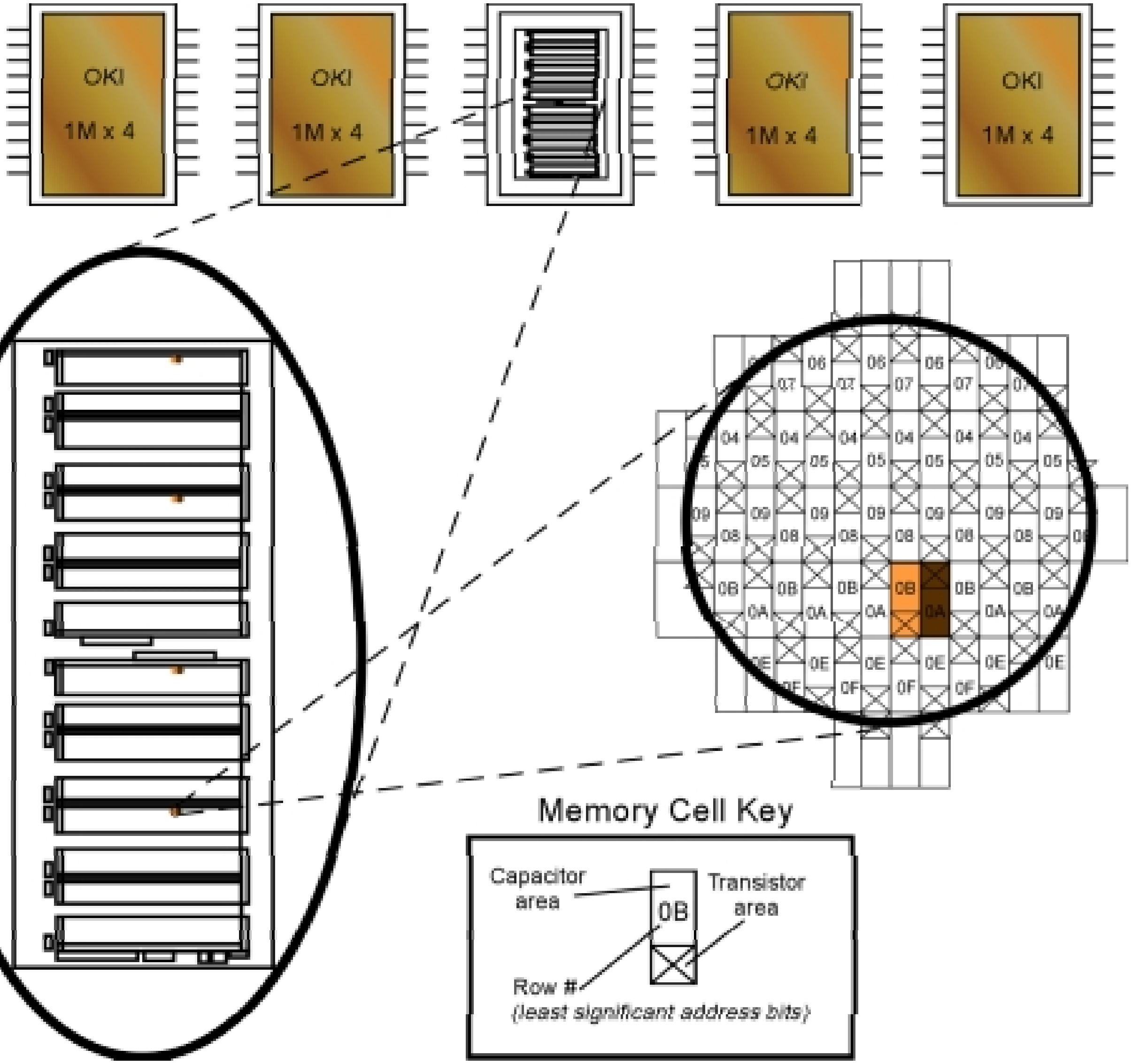
EDAC Issues

- Error-detection-and-correction
  - Used in solid-state recorders on many JPL spacecraft
  - Different levels of correction, depending on algorithm
    - Single and double bit detection, with single-bit correction
    - Double bit detection and correction (larger word size)
- EDAC algorithms can fail at high rates
  - Solar flares
  - Transitions through radiation belts

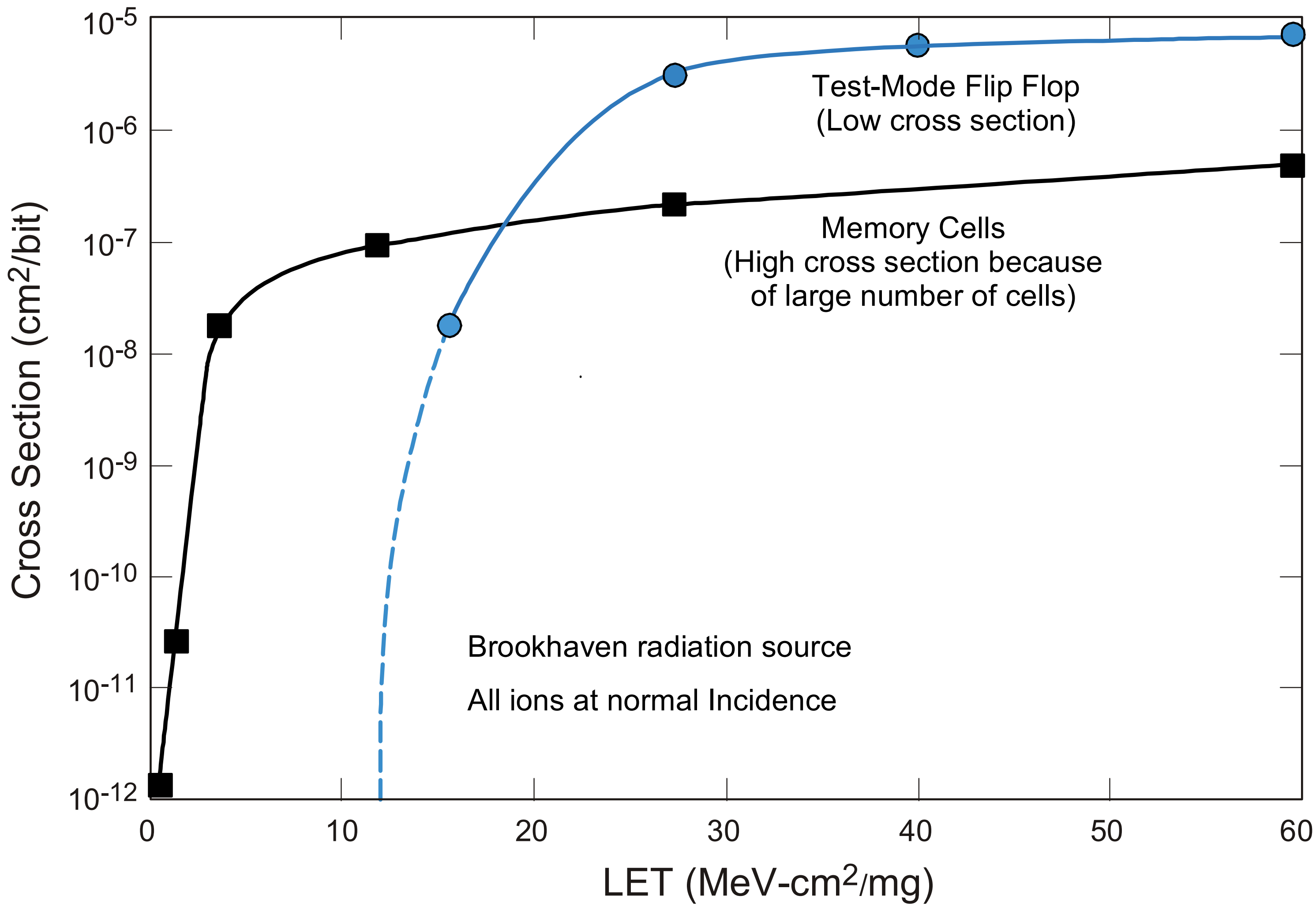
Multiple Bit Upsets in OKI DRAM



Cassini SSR Architectural Flaw



Functional Interrupt Effect ("SEFI")



Circuit Technologies where SEFI Is Important

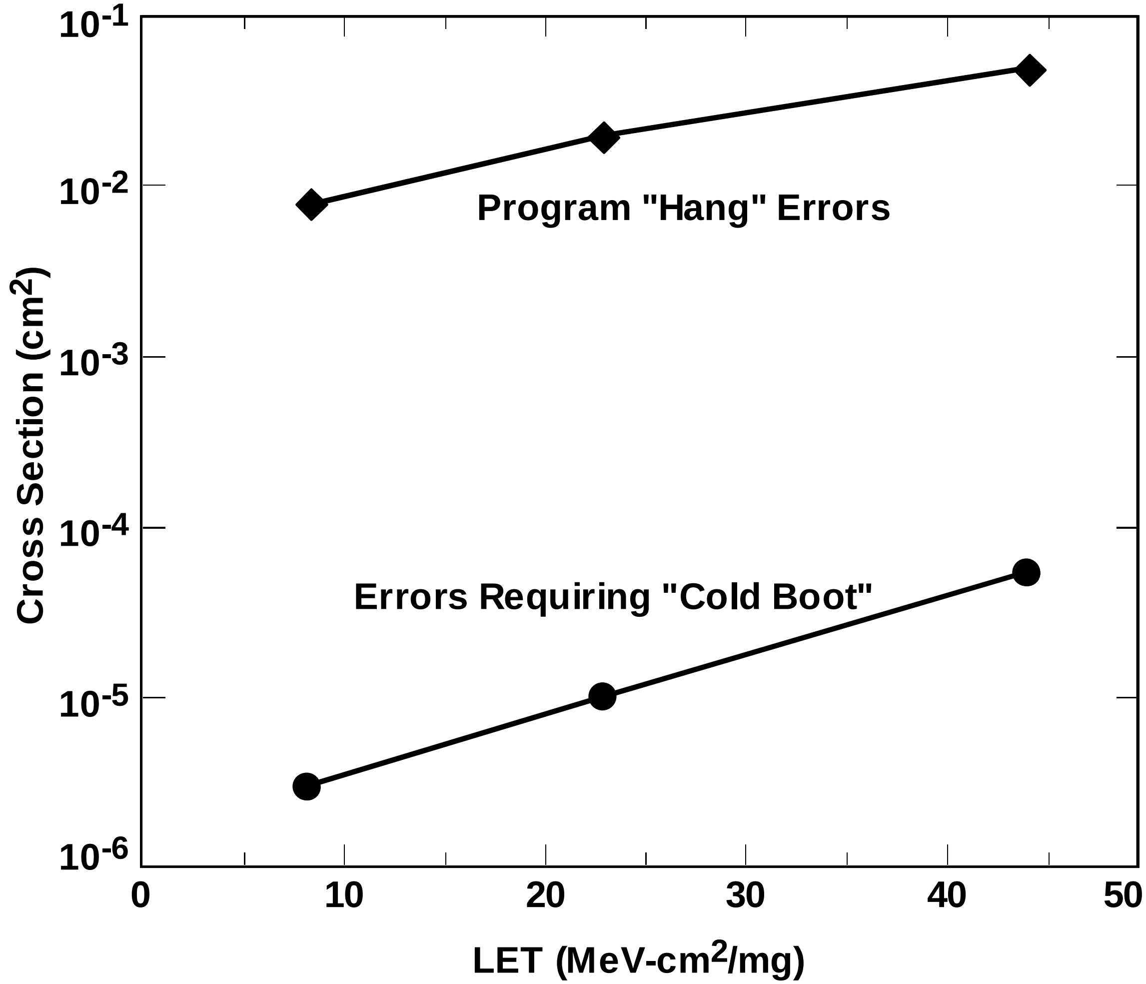
Advanced Memories
- Internal test modes
- Microprogrammed cell architecture

Flash Memories
- Dominant effect
- “Crashes” internal state controller and buffers

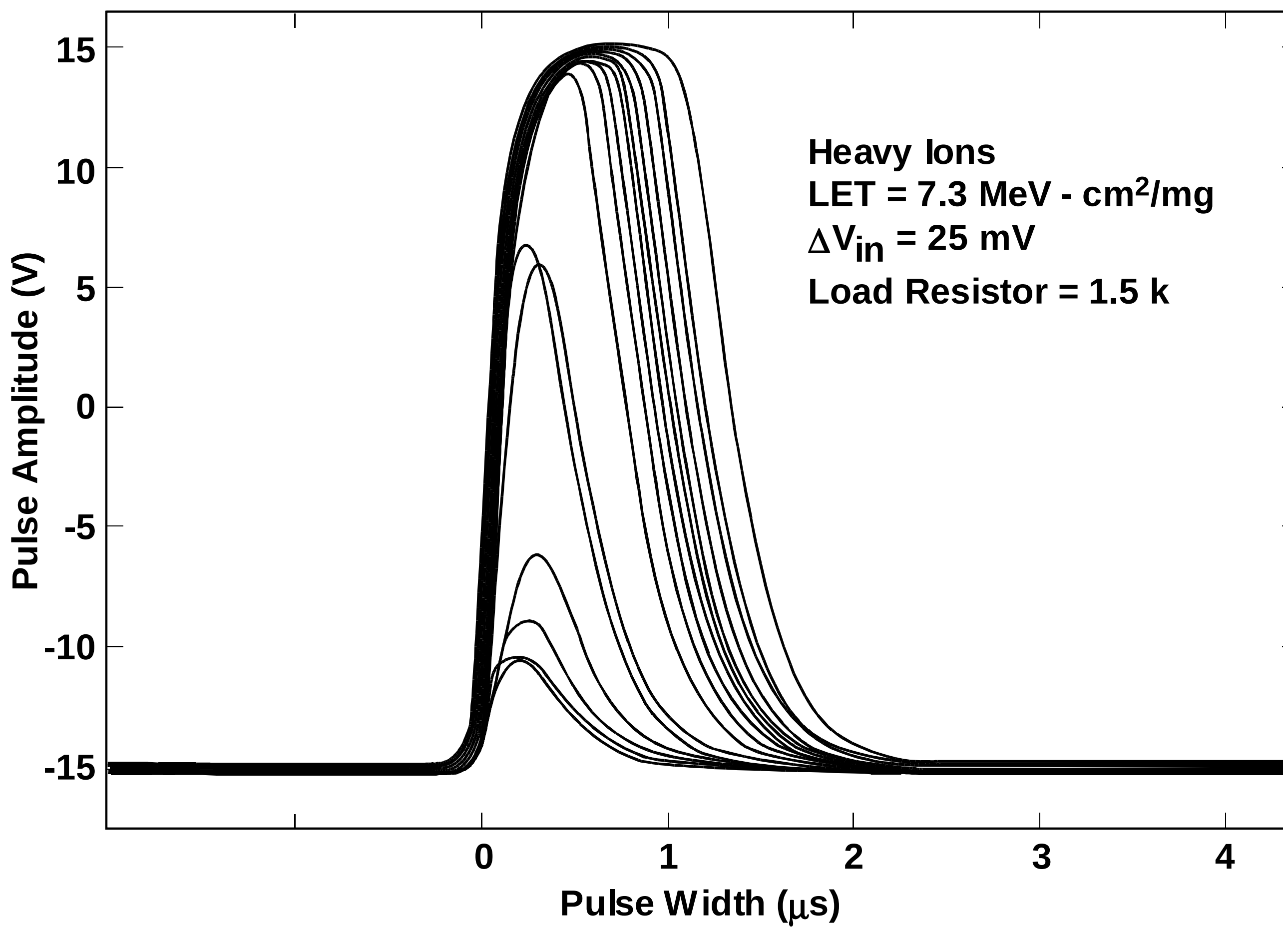
Xilinx Programmable Logic Arrays

Microprocessors
- Many categories of responses
- Detection and recovery are very difficult problems

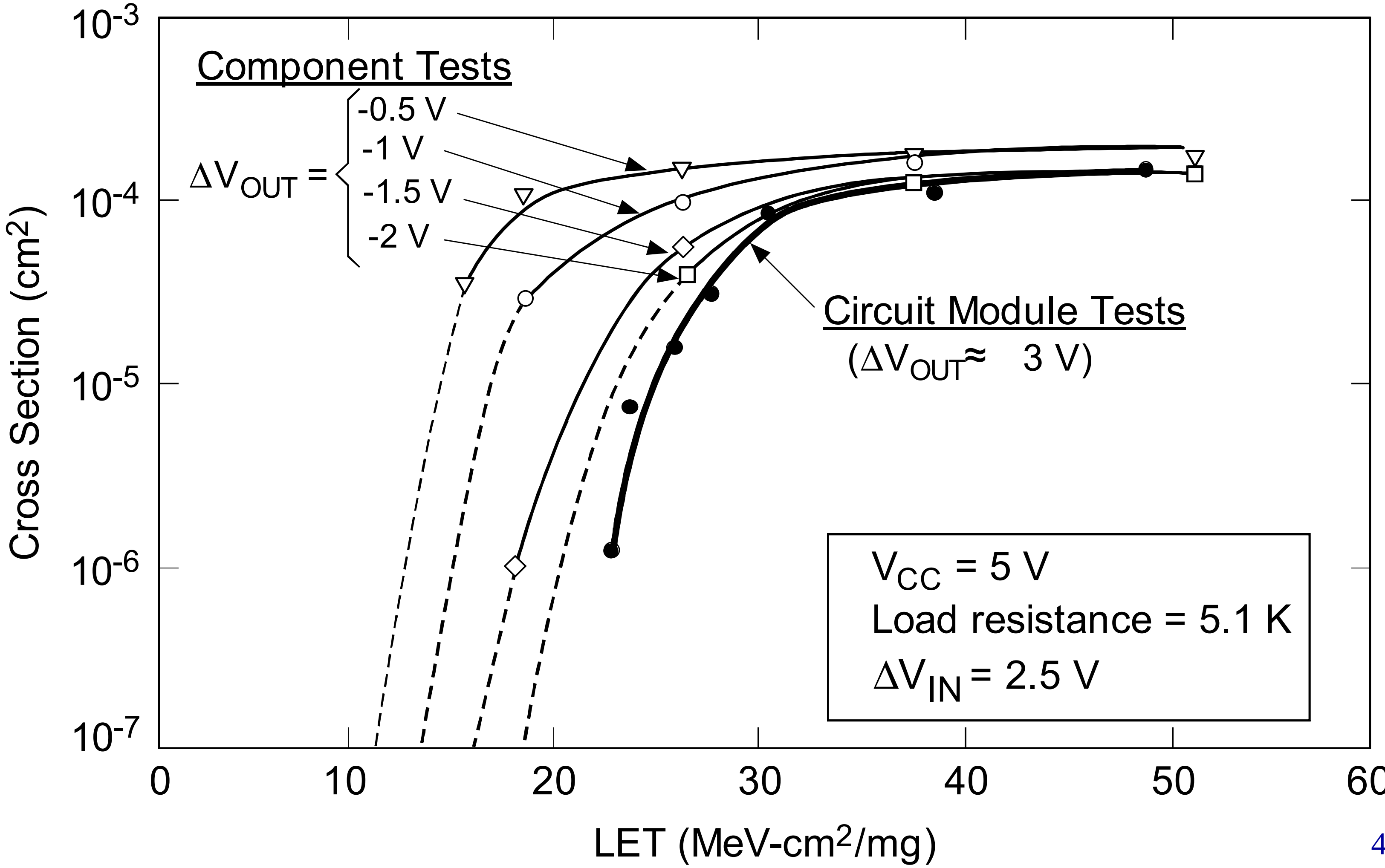
Non-Recoverable Errors in the 486 Processor



Output Pulses from Ion Strikes on a Comparator



Cross Section for Transients in the PM139 Comparator



Calculated Upset Rate for Cassini Power Modules

Assumed Environment	Aspect Ratio	Errors per Switch-Day
GCR, solar minimum	5:1	4.5×10^{-5}
GCR, solar maximum	5:1	8.2×10^{-6}
Design-case solar flare	5:1	1.6×10^{-2}

SEE Testing

Why so expensive?

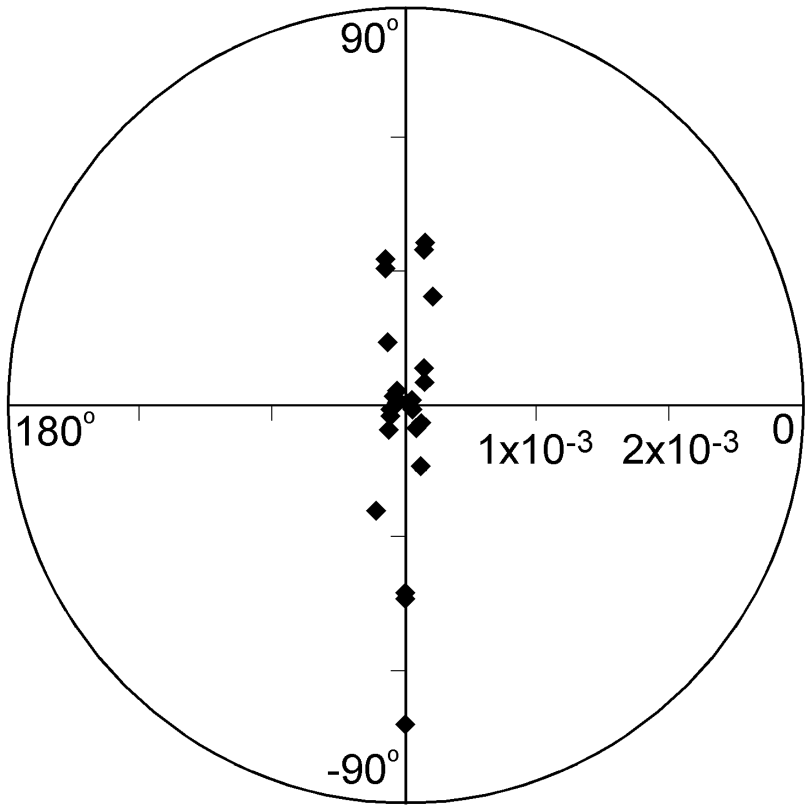
Remote, Expensive Facilities (Accelerators)

Test Development

Special Problems
- Part De-lidding
- In Vacuum Operation

Toshiba Angle Plot

Cross Section vs. Azimuthal Angle for a Toshiba 64Mb DRAM Using F at 48° (polar plot)



Summary

SEE Effects Are an Important Issue for All Spacecraft

Testing and Evaluation of the Impact of SEE Is a Complex Problem

- Few problems with older spacecraft because of thorough testing
- Likely to become more severe for newer technologies

Section 514 Continually Evaluates SEE Effects

- Direct Support to Many JPL Programs
- Testing of Advance Microprocessors for REE
- Evaluation of Advanced Devices under the NEPP Program

Section IV: Nonrecoverable SEU Effects

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Non-Recoverable SEE

Events which interrupt device function and do not recover without external interaction

These events may permanently damage the device

Three main types

- Latchup (SEL)
- Hard errors (SHE)
- Rupture/Burnout (SEGR/SEB)

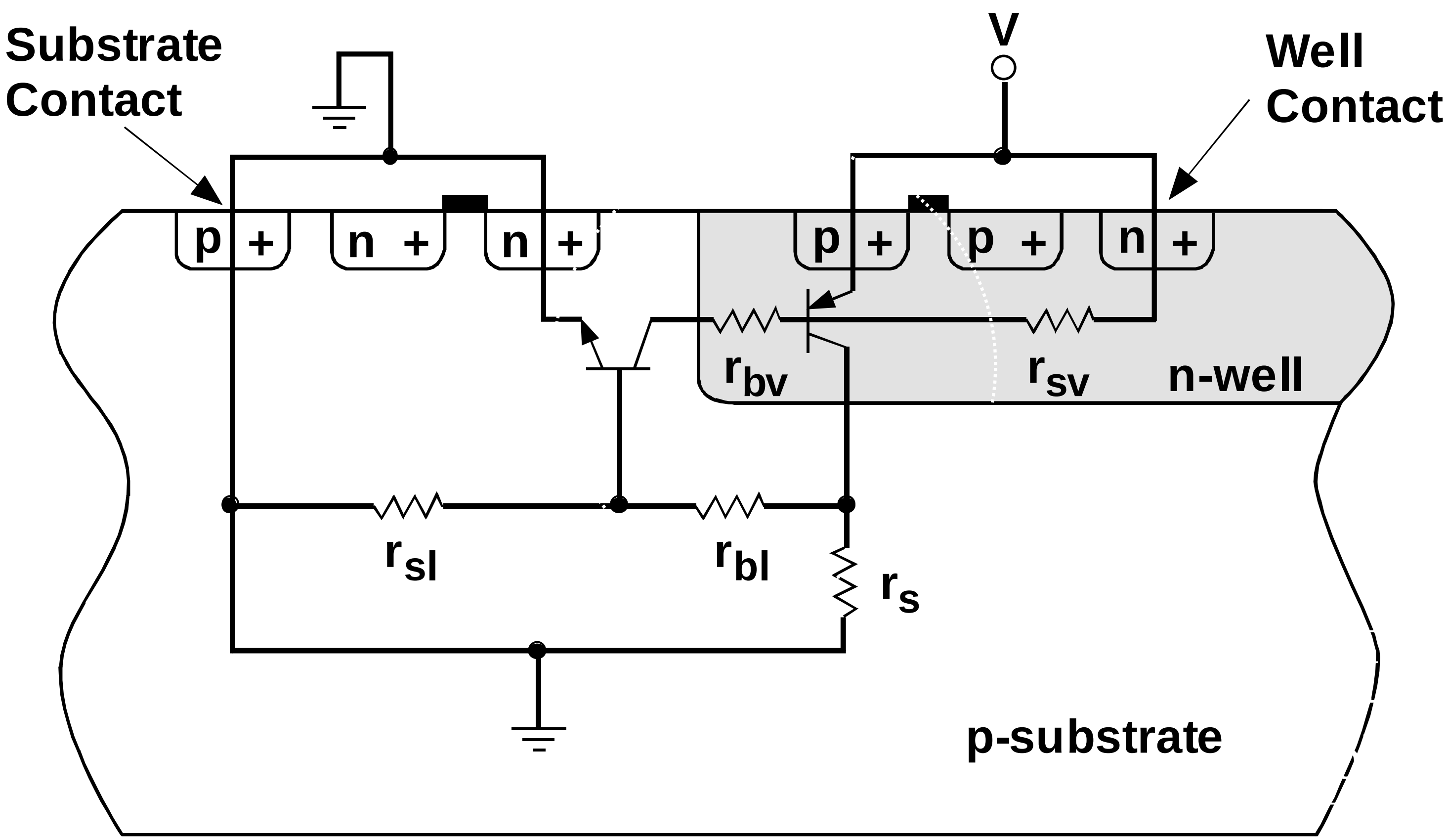
Latchup Is a Common Problem for CMOS Technology

Latchup paths are inherent in most CMOS circuits because of the fabrication technology

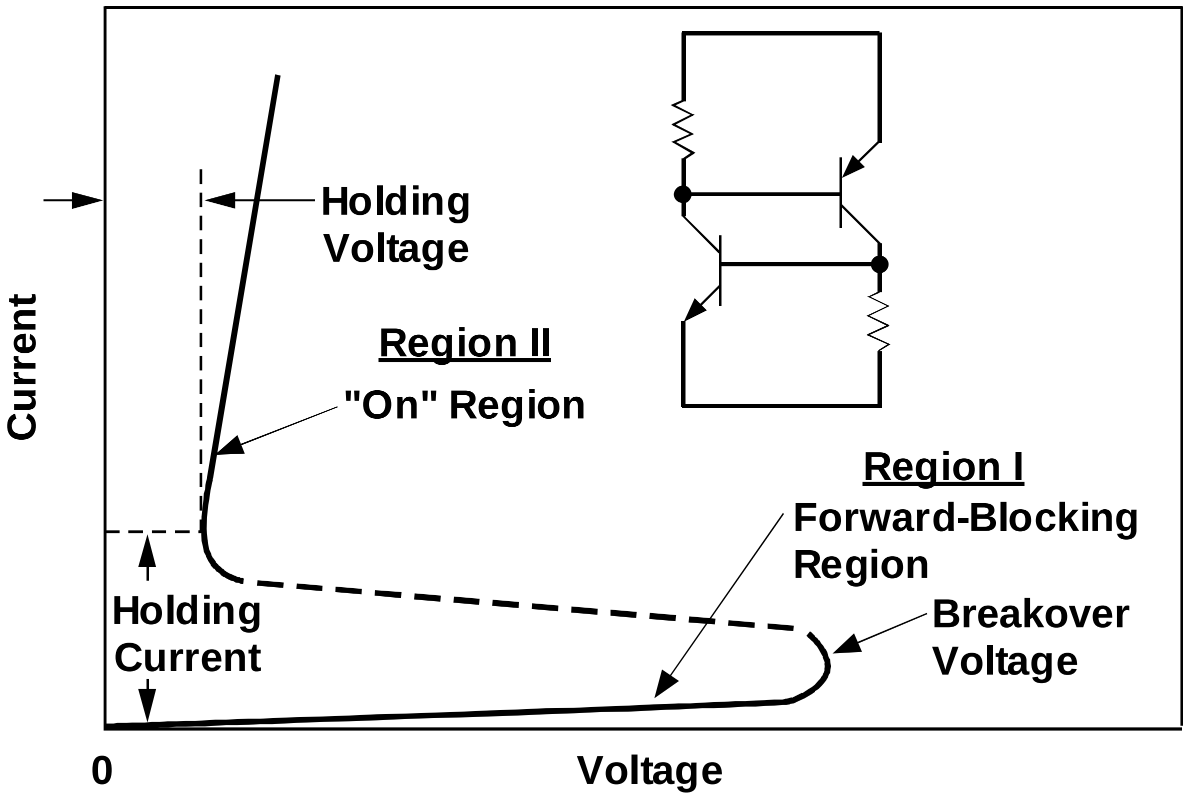
The commercial Modem on Pathfinder’s Rover was susceptible to latchup

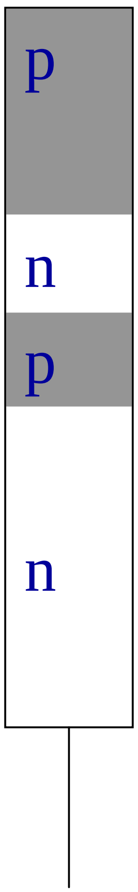
- Laboratory tests showed that the latchup was not destructive
  - This allowed the device to remain latched for periods of several minutes
  - A simple power cycle counter measure was used in the application
- The latchup probability was low for this application
  - Short mission life (nominally two weeks)
  - Risk deemed acceptable by mission planners

SEL Latchup Path



SEL I-V Characteristics





SEL Facts

Triggered by heavy ions, protons, neutrons

May be catastrophic

Only recovered by power cycle

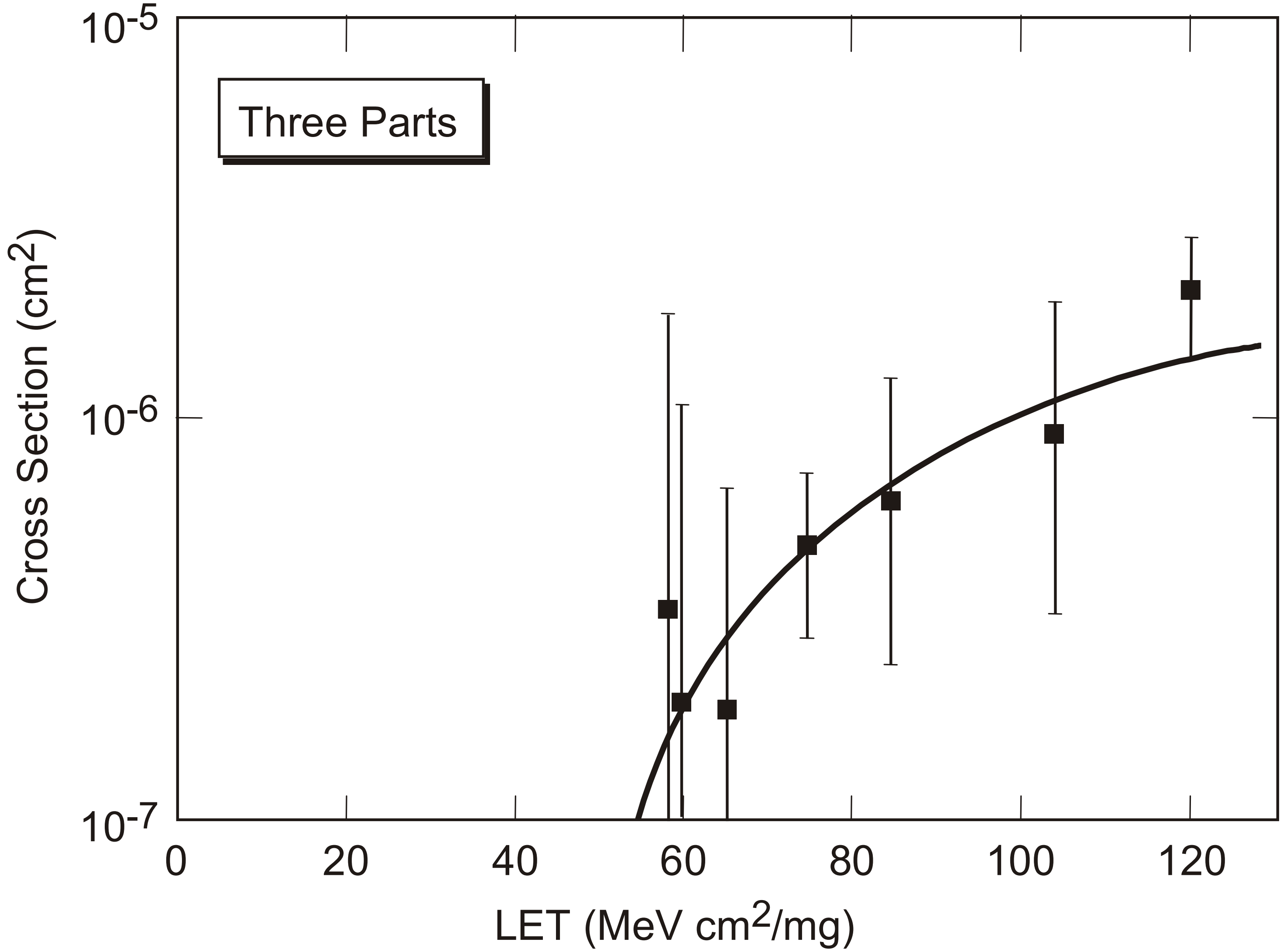
SEL is strongly temperature dependent

- Threshold for latchup decreases at high temperature
- Cross section increases as well

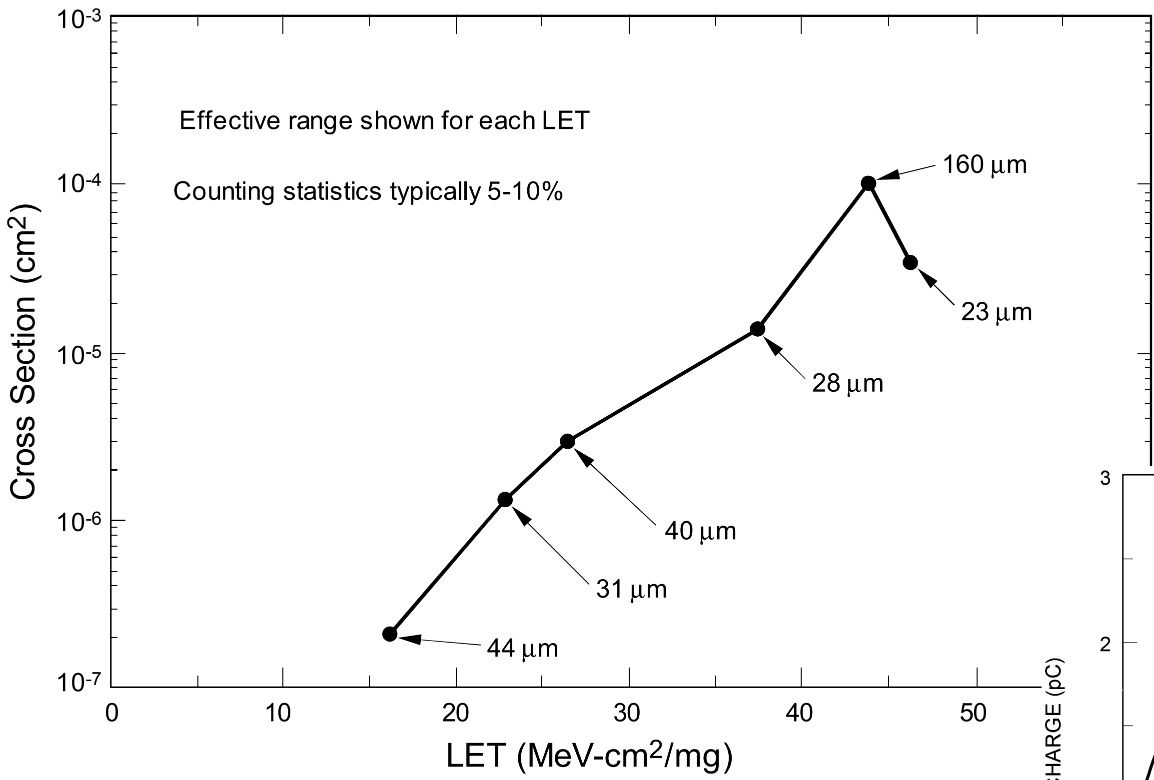
Modern devices may have many different latchup paths

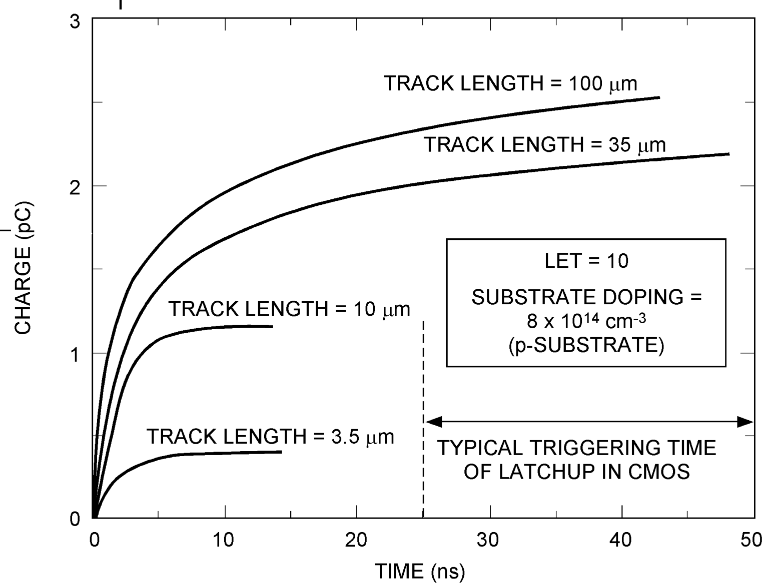
- Both high current and low current SELs can occur
- Characterization of latchup is a difficult problem for complex circuits

SEL LET Dependence

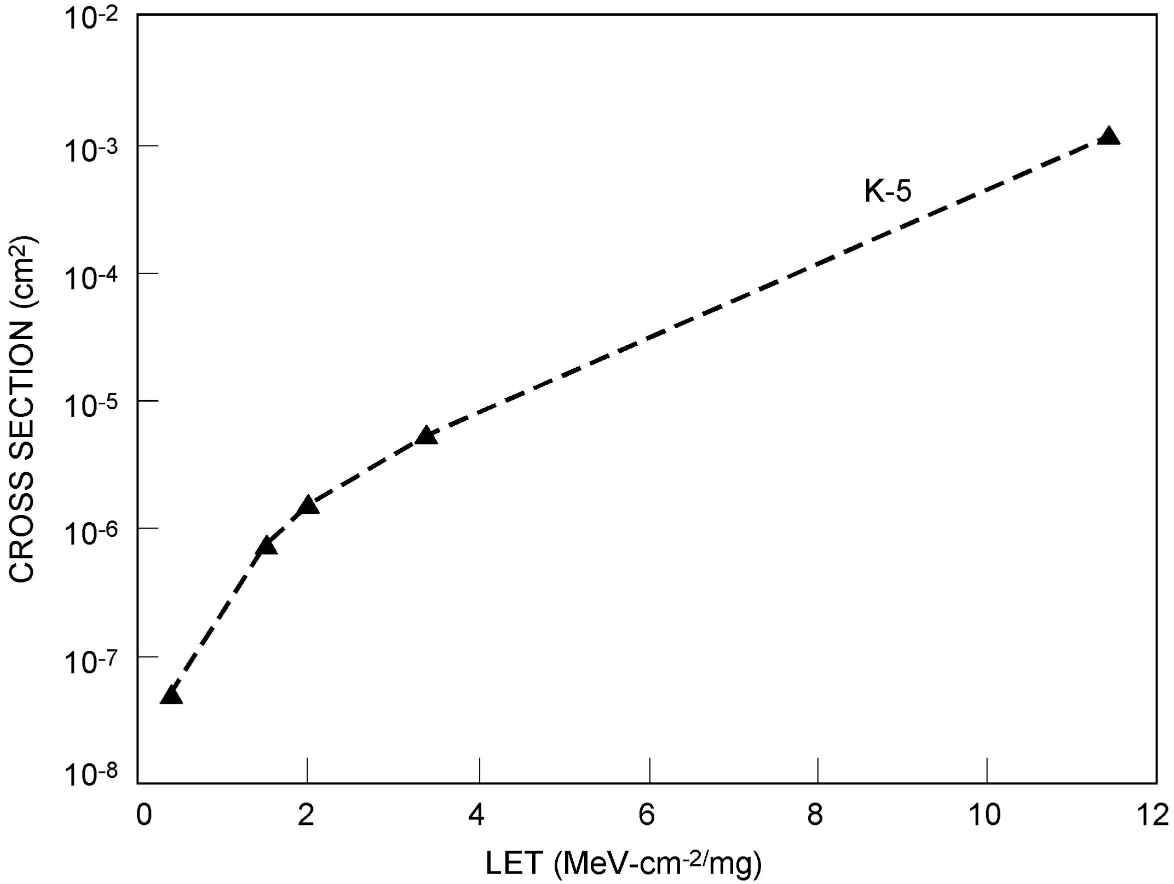


SEL Ion Range Dependence





SEL Example: Induced by Protons in K-5

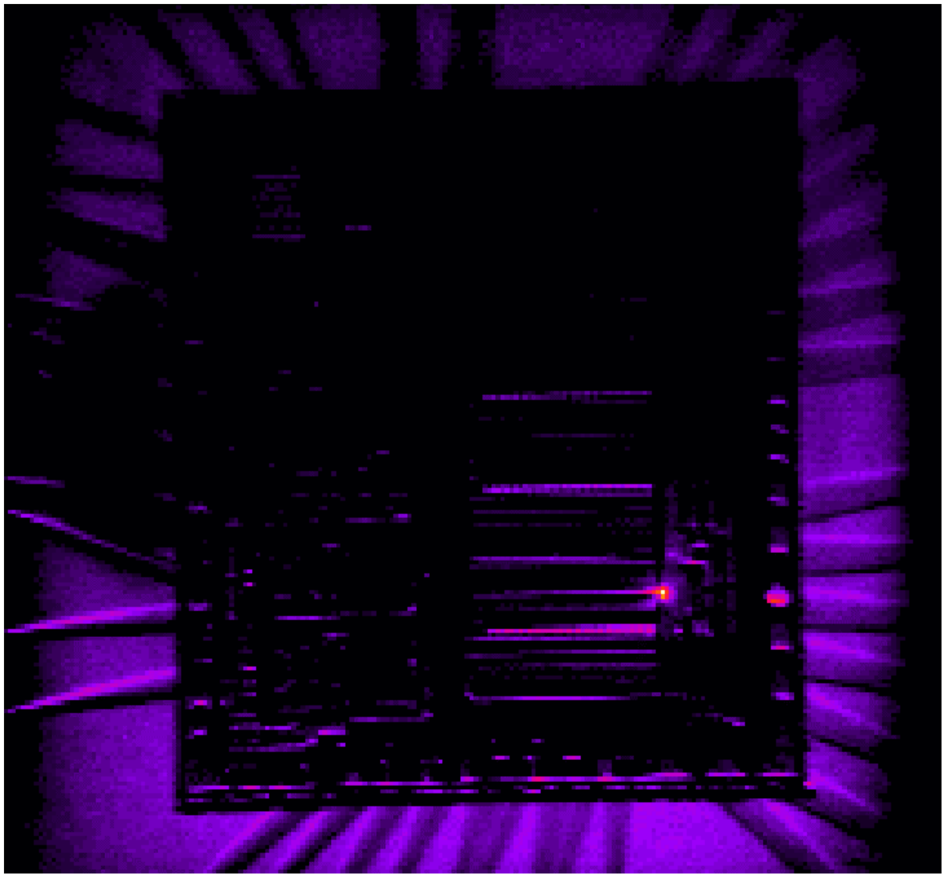


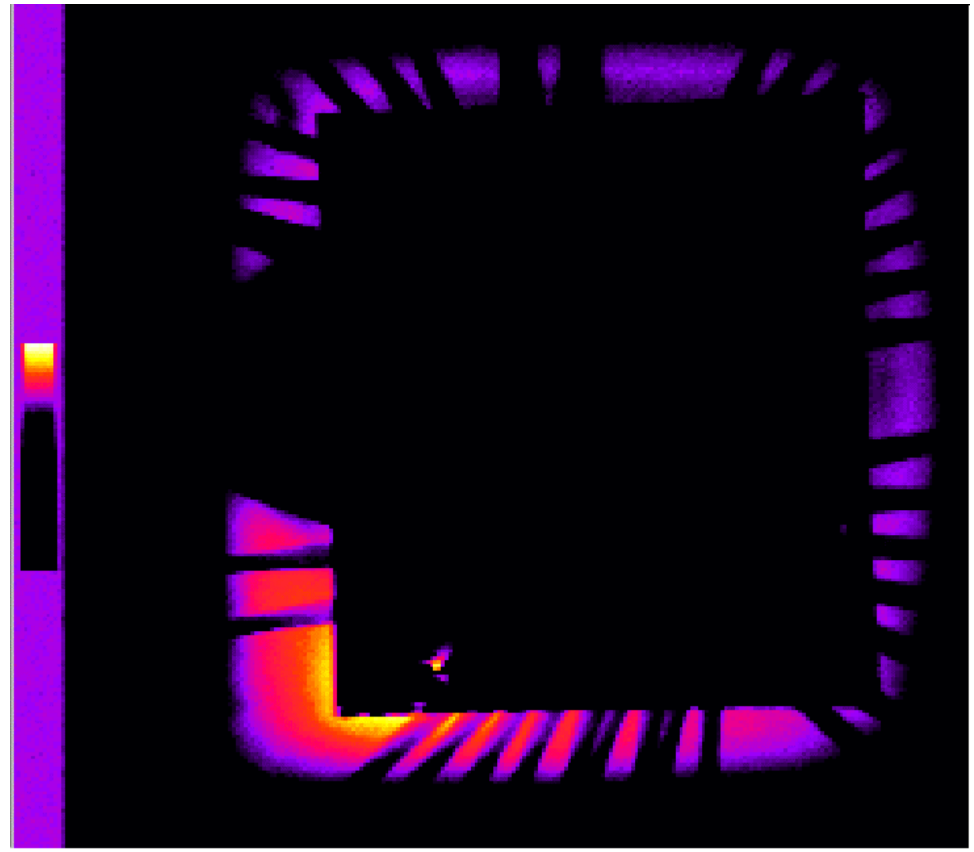
SEL occurred at 0.4 MeV cm^2/mg

- **Due to nuclear recoils**
- **Cross section of 6.7×10^{-8} cm^2**

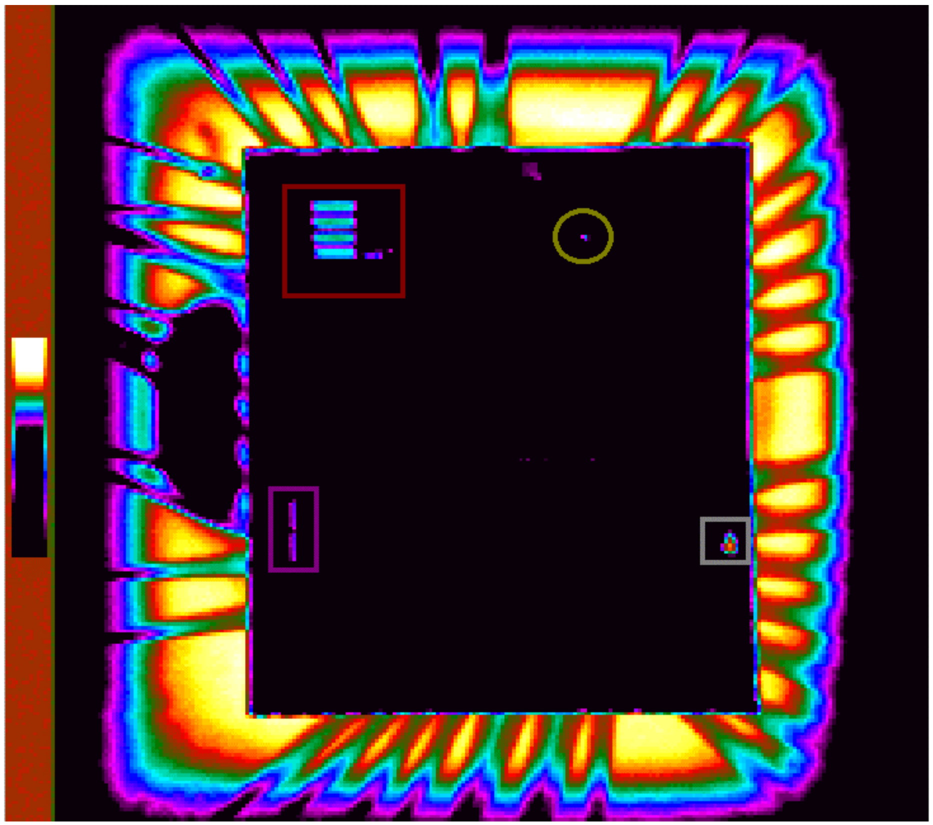
Many of the latchup events were destructive

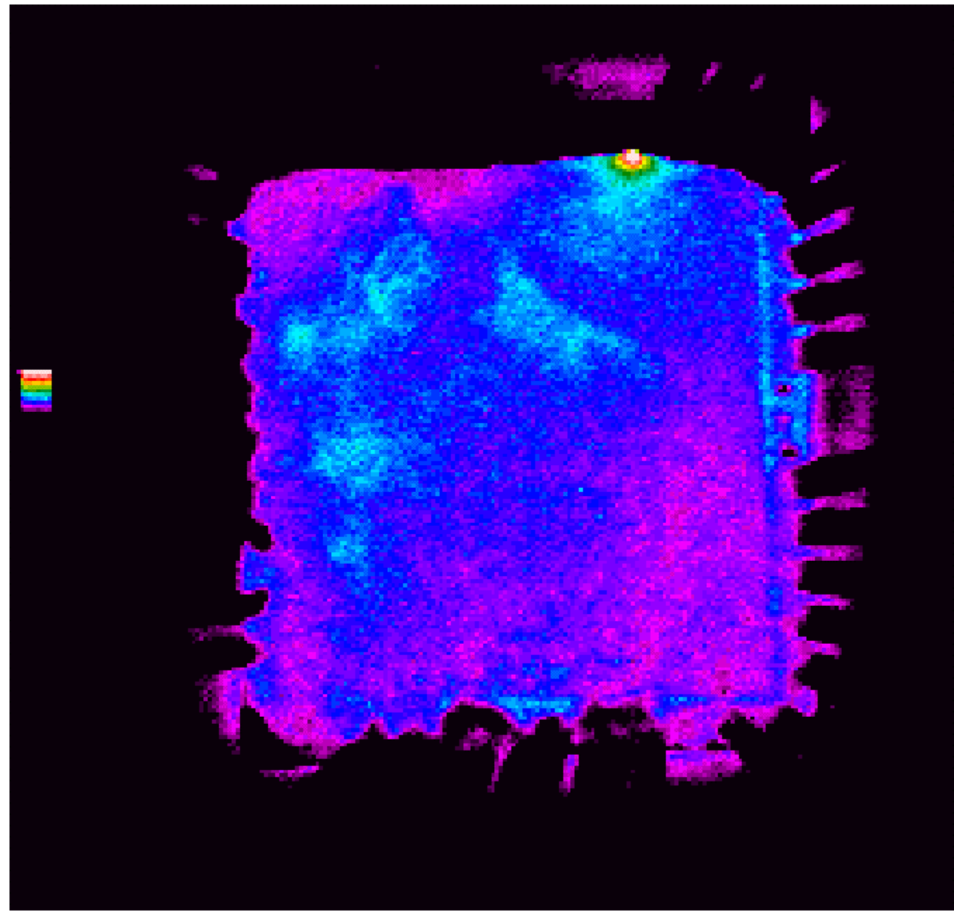
SEL Heating



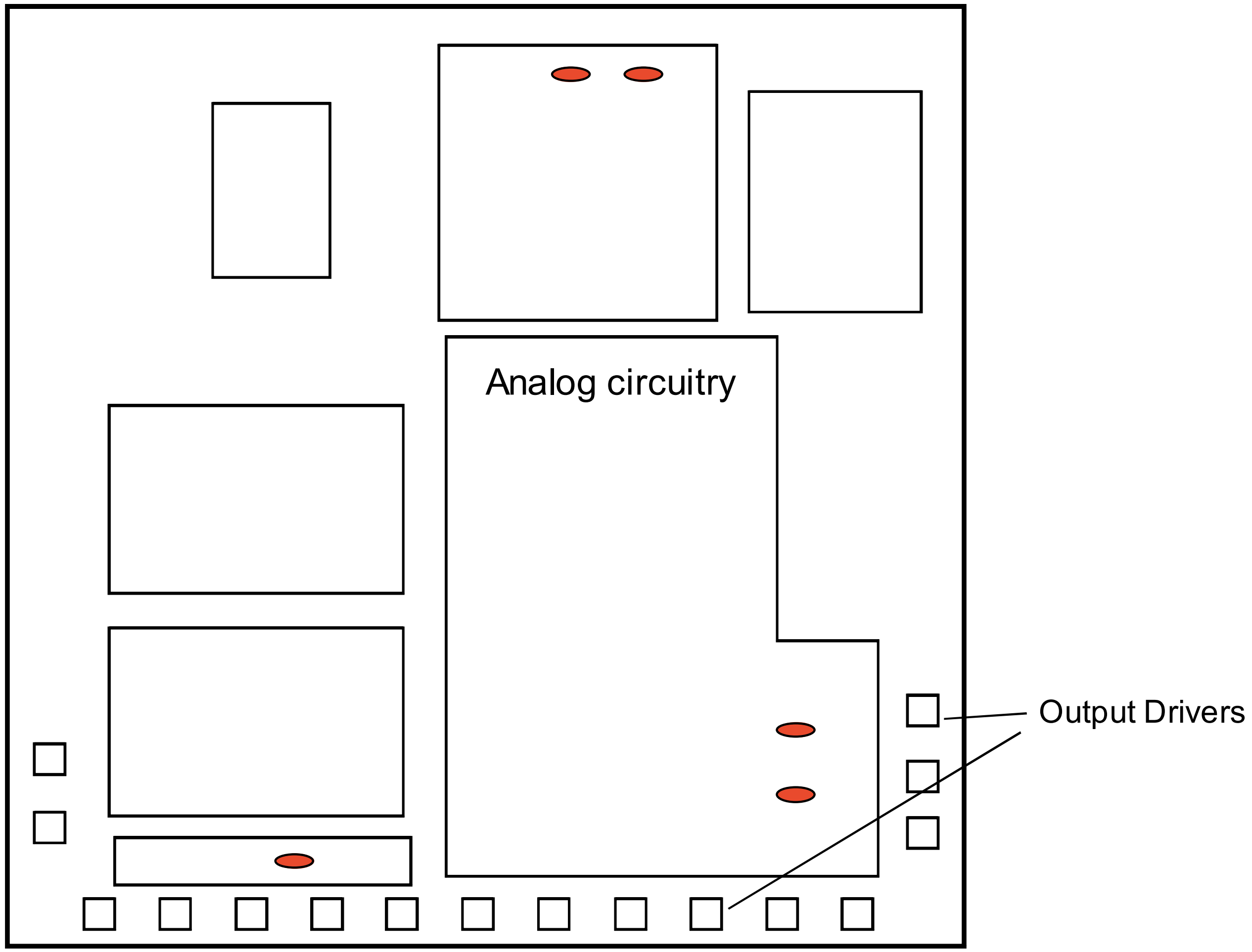


SEL Heating*

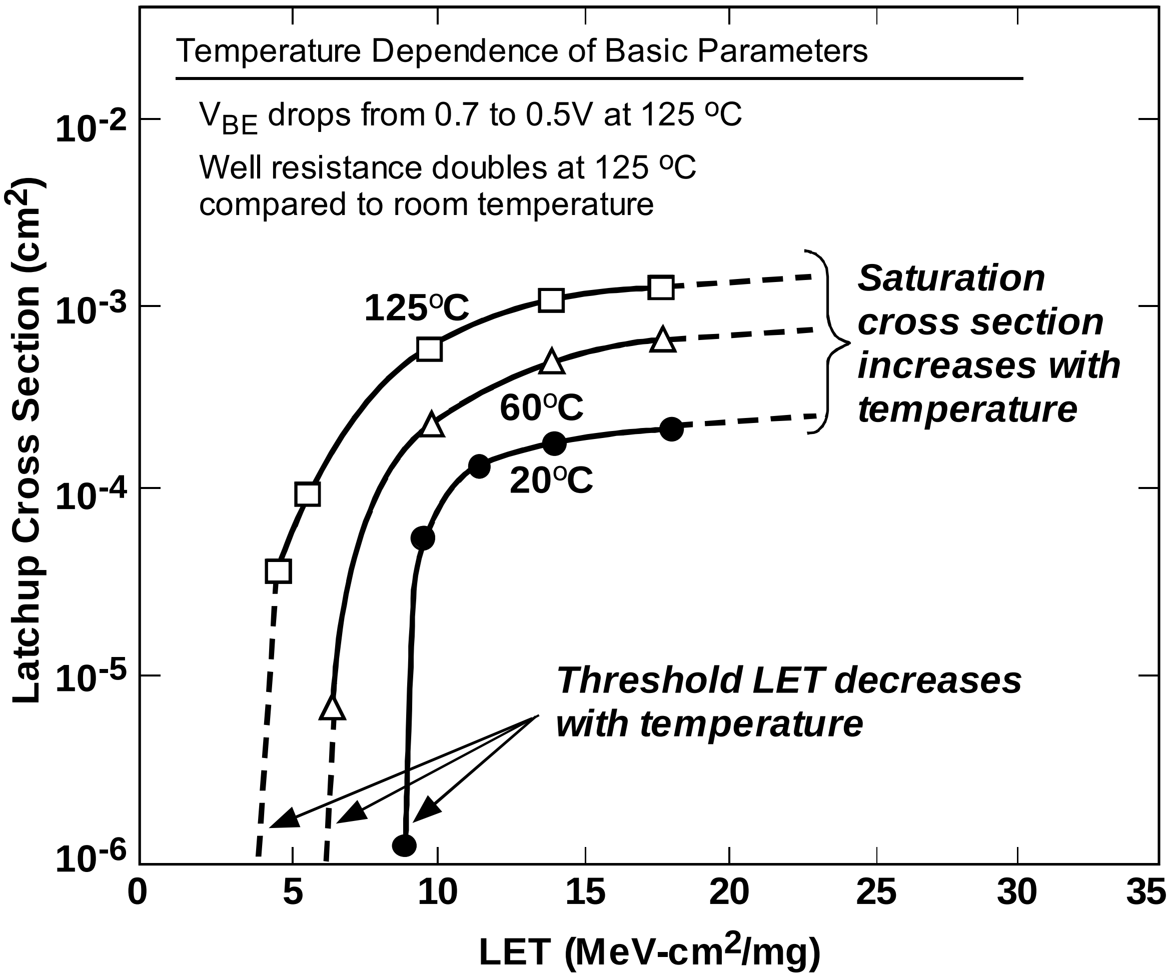




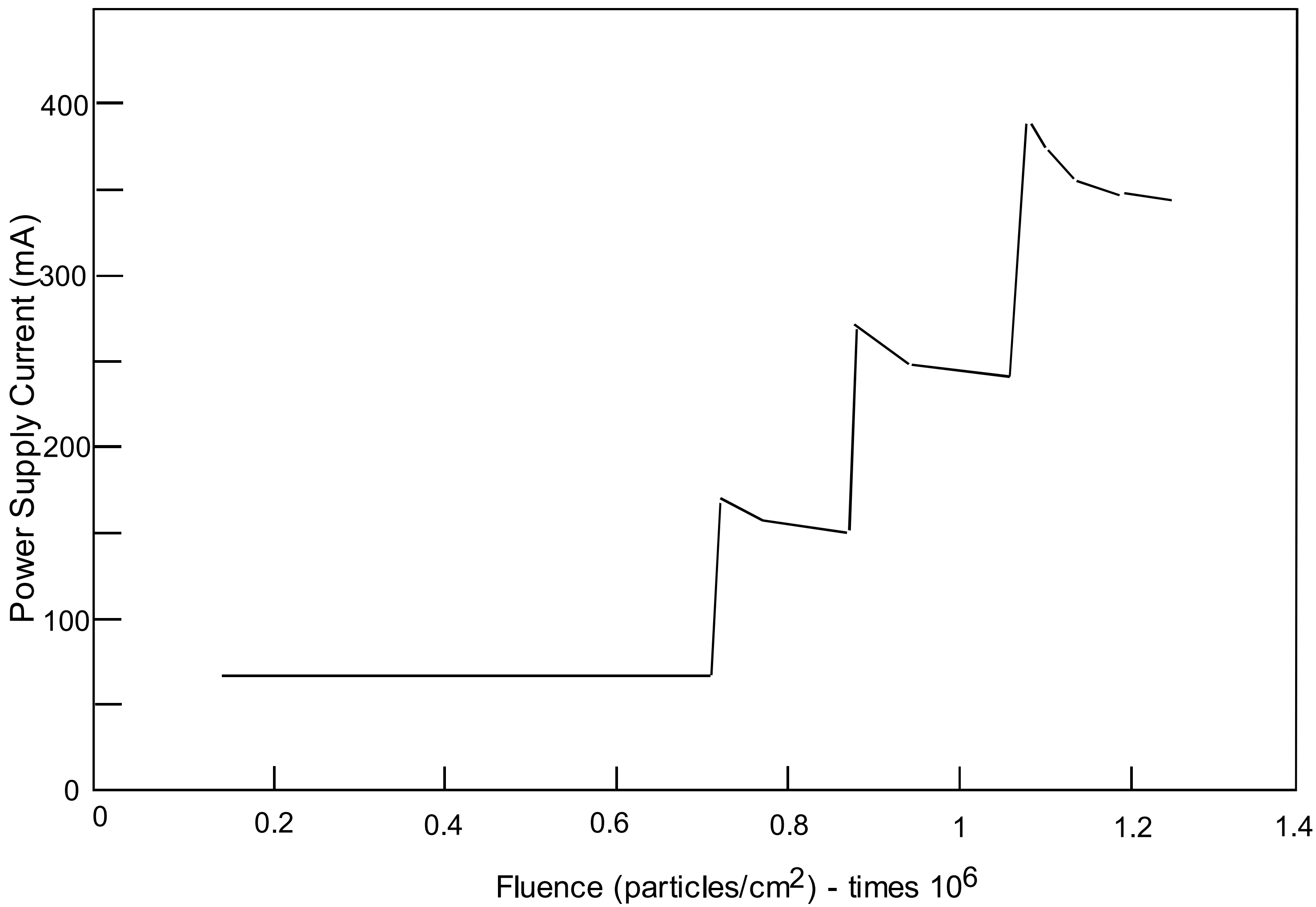
SEL Heating



SEL Temperature Dependence



SEL Temperature Dependence*



SEL Counter Measures

SEL Detection and Mitigation

- Current limiting devices can’t stop latchups or low current latchups
- Detection circuits can’t stop all latchups
  - Some devices have latchup modes which are always destructive
- Mitigation may not be fast enough
- Thorough testing required to ensure that all latchup events are detected

SEL Technology Options

Device type

- Bulk CMOS latches worst
  - **COTS**
- CMOS deposited on epitaxial layer may improve SEL immunity
  - **Some COTS - More Expensive**
  - **Not always effective (e.g., K-5 processor)**
- SOI and isolated oxides are mostly immune
  - **Very expensive**
  - **Limited availability**

Single Hard Errors

Large rare energy depositions can cause individual cells to be unable to change state

- Referred to as a “stuck bit” in memory
  - This is a microdose effect
- Microlatchups can cause a fraction of bits to be unable to change state
  - Power cycling is required

Destructive SEEs

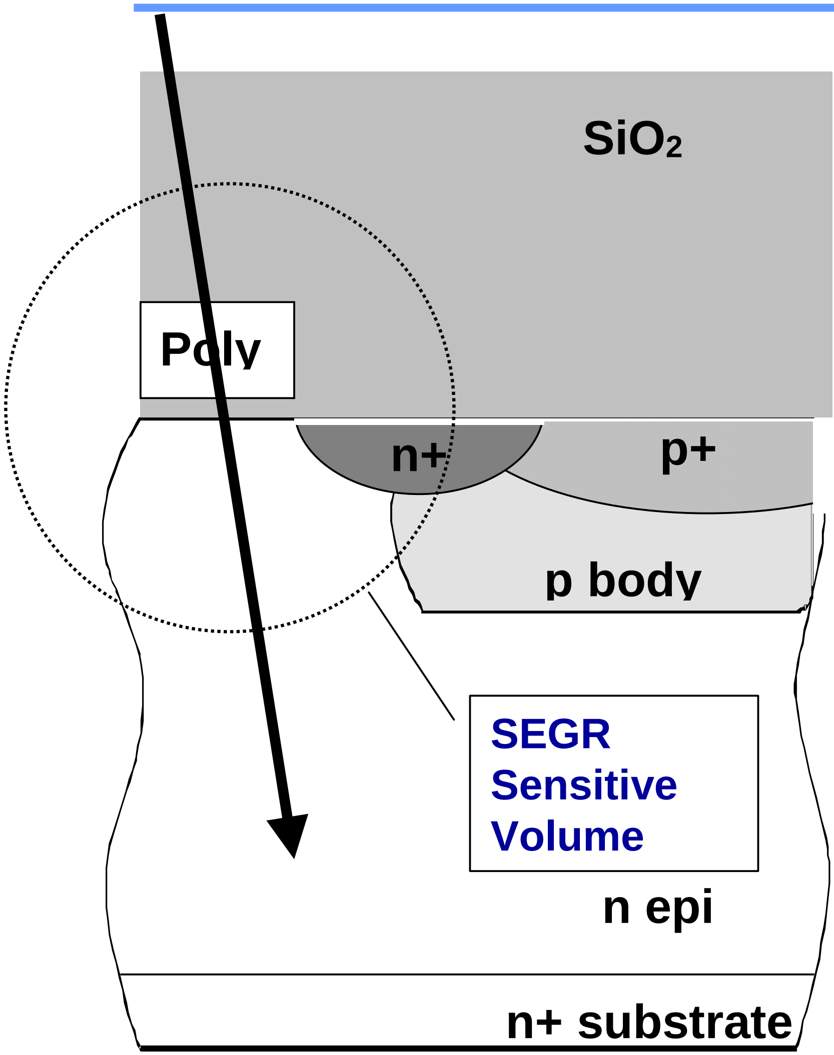
Gate Rupture (permanent failure of oxide)

- Power devices are most susceptible
- Programmable devices also susceptible
- Very thin oxides in VLSI devices

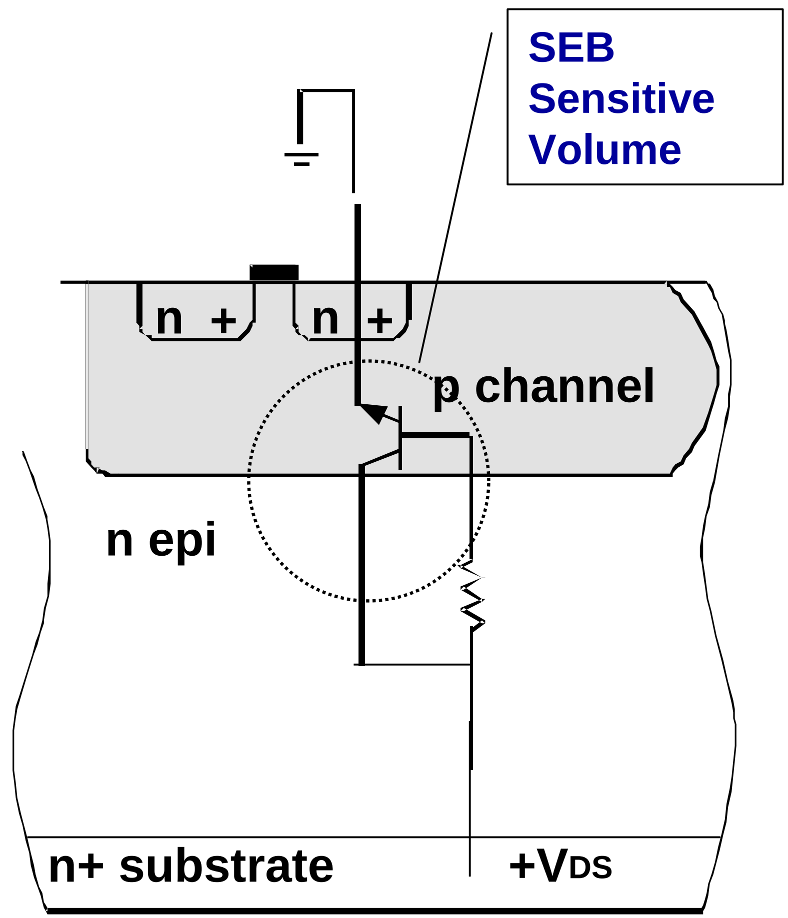
Burnout

- Caused by excessive localized current within the structure
- Power transistors
- Some types of linear integrated circuits

Destructive SEEs



Single Event Gate Rupture Power MOSFET



Single Event Burnout HEXFET

SEB Facts

Triggered by heavy ions, and possibly by protons and neutrons

Always destructive

CMOS, power BJTs and MOSFETs are susceptible

Mechanism:

- Localized current in body of device
- Roughly analogous to second breakdown in power transistors
- Devices with low doping concentrations are most susceptible

SEGR Facts

- Triggered by heavy ions
- Always destructive to device
- Dependent on angle of incidence
- Dependent on electric field in gate oxide
  - **May also occur with zero electric field**
  - **Interplay between pulsed current in drain region and oxide field**
- Synergy between TID and SEE
- Power MOSFETs most susceptible
  - **Some modern programmable devices are also susceptible**

SEGR/SEB Examples

SEGR

EEPROM
- During writing/erasing

LAMBDA ASIC

Power MOSFET
- LET threshold of 25 MeV-cm^2/mg with drain biased at 1/2 rated maximum, and zero voltage on gate

SEB

CRUX/APEX
- 2N6796 had a LET threshold of 15 MeV-cm^2/mg

Dealing with SEGR and SEB

Test all device types that are potentially susceptible

Derate devices well below maximum rated values

- Possible for discrete power devices
- Not appropriate for SEGR or SEB in integrated circuits

Minimize duty cycle for application of high voltage to susceptible parts

Program high voltage device in low radiation environments

Summary

Latchup

- Temperature dependent
- Epi devices are generally better
- Prevention circuits not necessarily effective
- Best approach is to avoid using latchup-prone devices

Gate Rupture and Burnout

- High voltage devices are generally more susceptible
- Derate devices well below maximum operating conditions
- Ensure that all sensitive technologies undergo testing

Section V: Total Dose Effects

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Section 514

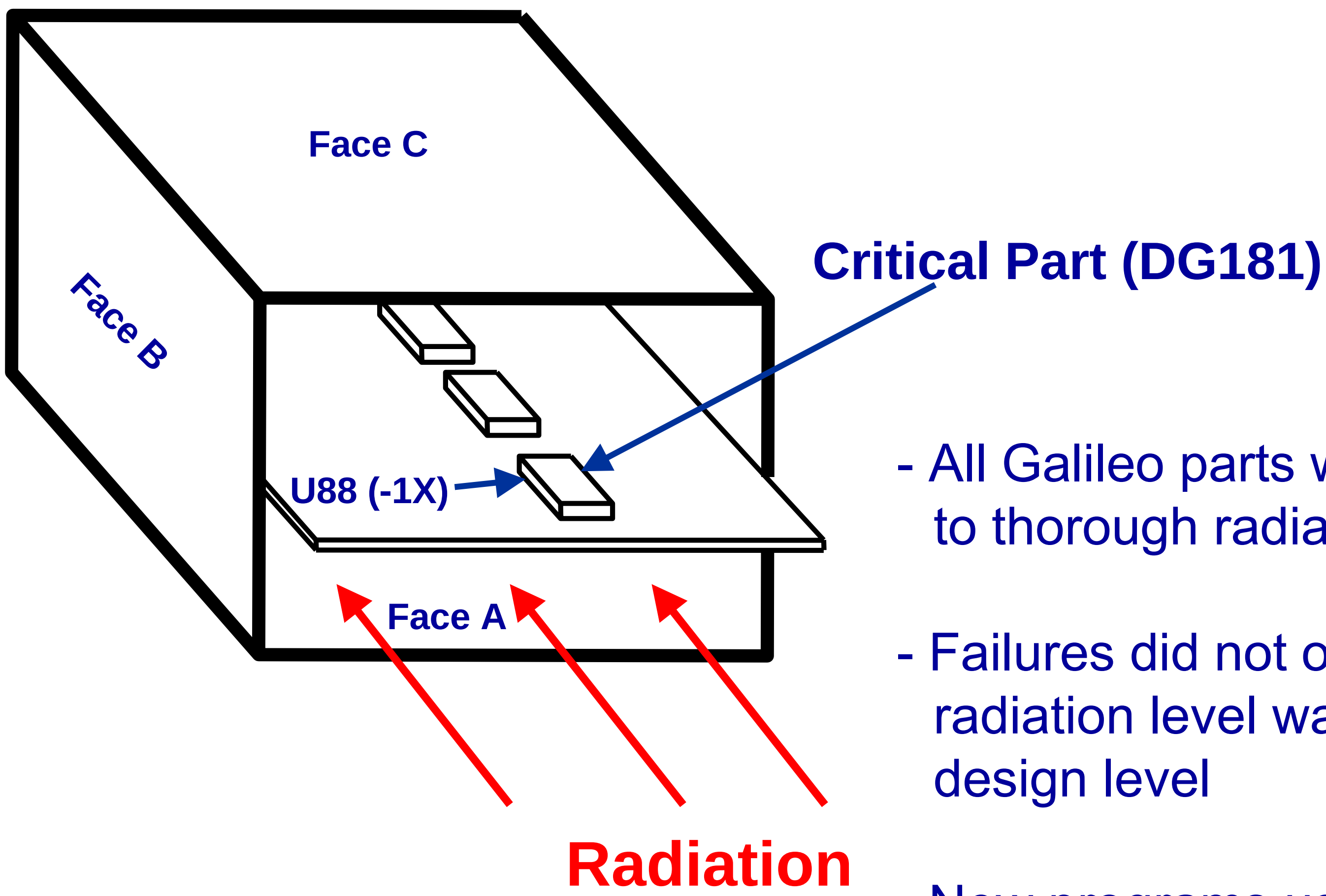
Space Radiation Effects

1) Single Event Effects (SEE)
   - Hard / Permanent
   - Soft / Recoverable

2) Total Ionizing Dose (TID)
   - Usually dominated by protons
   - Electrons are important for some planetary missions

3) Displacement Damage (DD)

Galileo Total Dose Problem



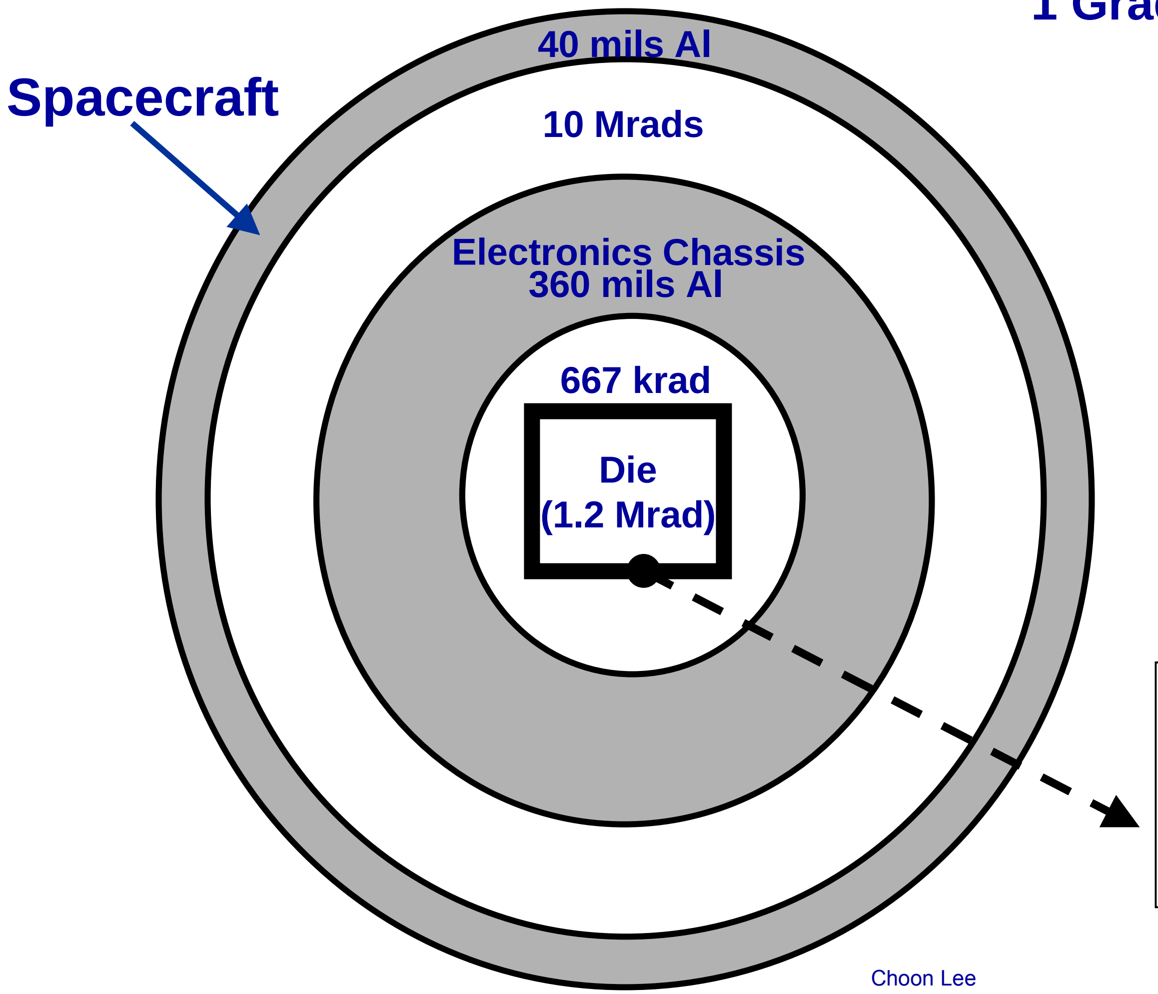
- All Galileo parts were subjected to thorough radiation testing

- Failures did not occur until radiation level was close to design level

- New programs use less stringent design methods

X2000/Europa Shielding Analysis

1 Grad outside Spacecraft!



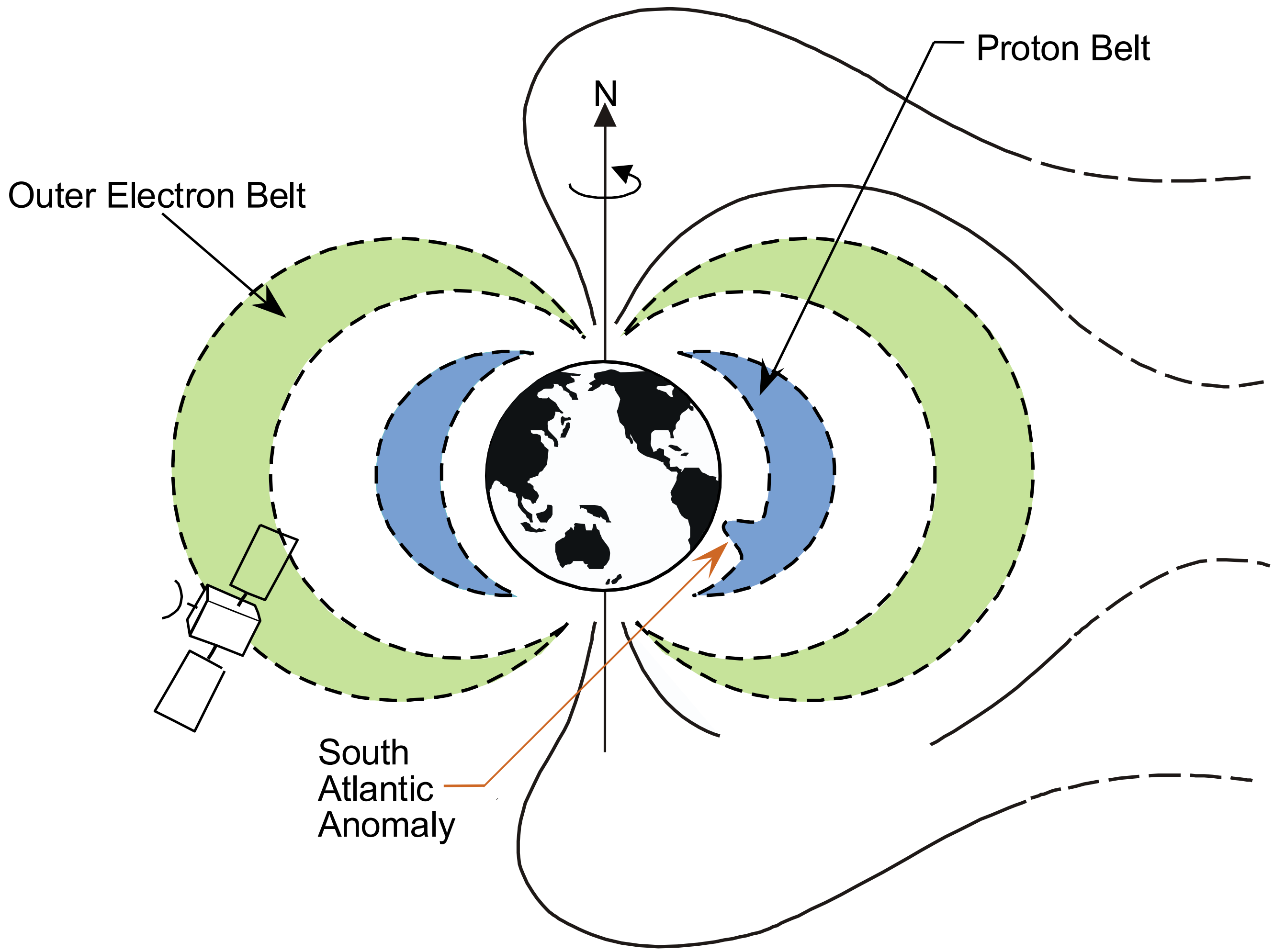
Additional 1.7 inches of Al shielding around the die provide 30 krad dose which allows use of 60 krad die with RDM of 2.0

Choon Lee

Outline

- Radiation Environment Shielding
- Basic Mechanisms
- MOS
- Bipolar
- COTS
- Testing
- Warnings and Misconceptions
- Recommendations

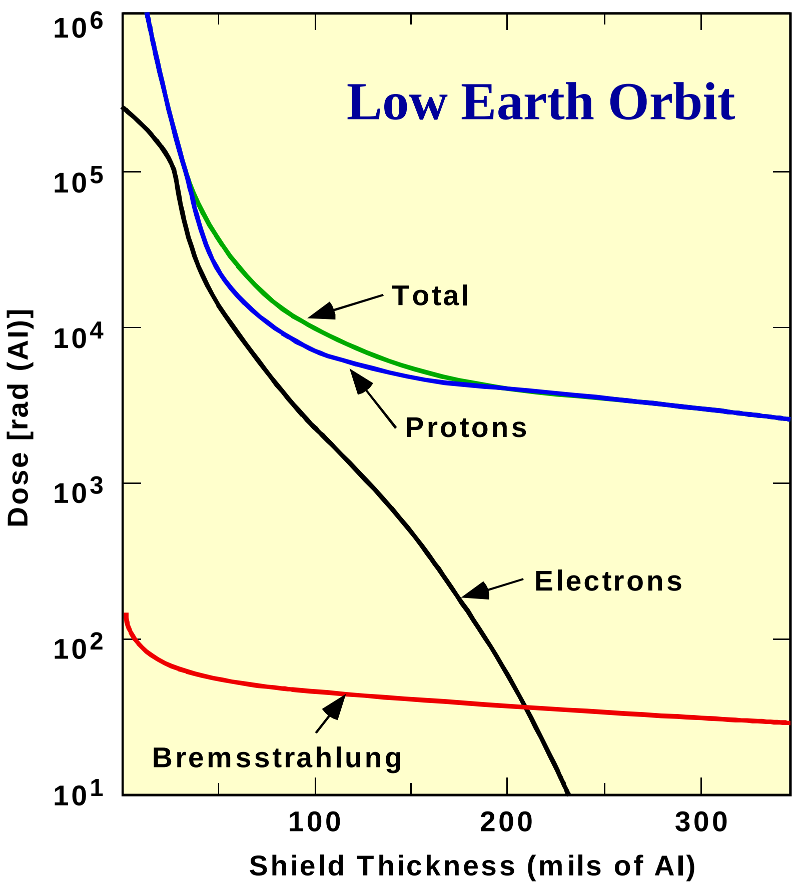
Near Earth TID Environment

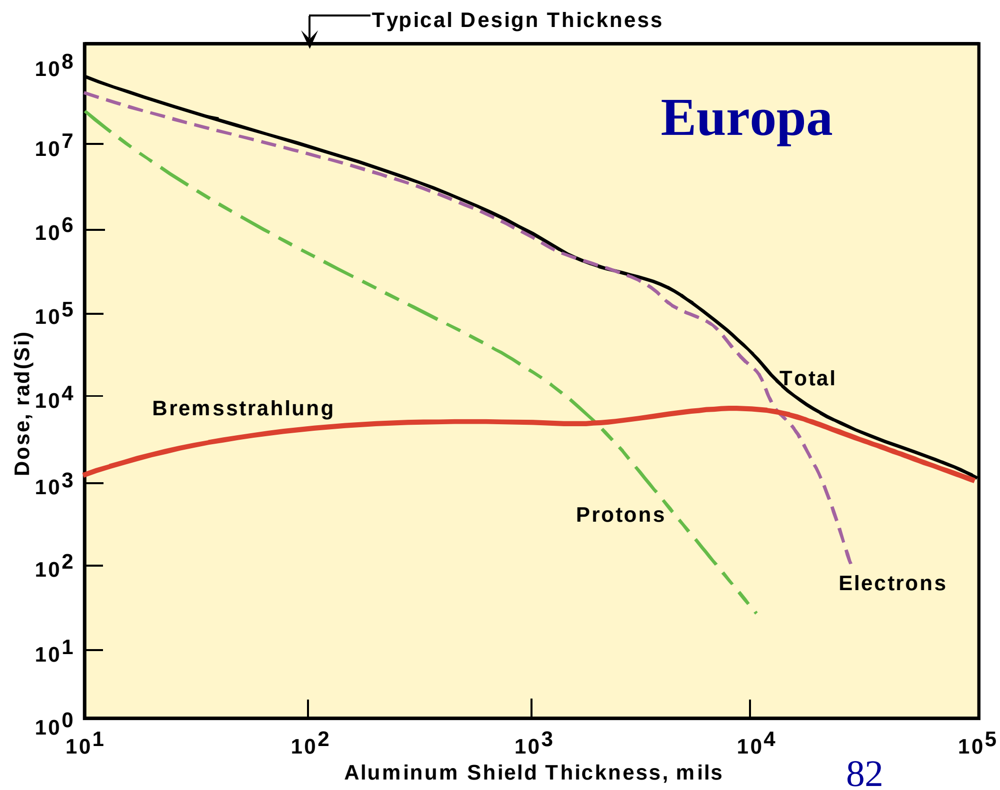


- Total accumulated dose depends on orbit altitude, orientation, and time.

TID Shielding

- Electrons more effectively shielded than protons
- Incremental shielding gives diminished returns



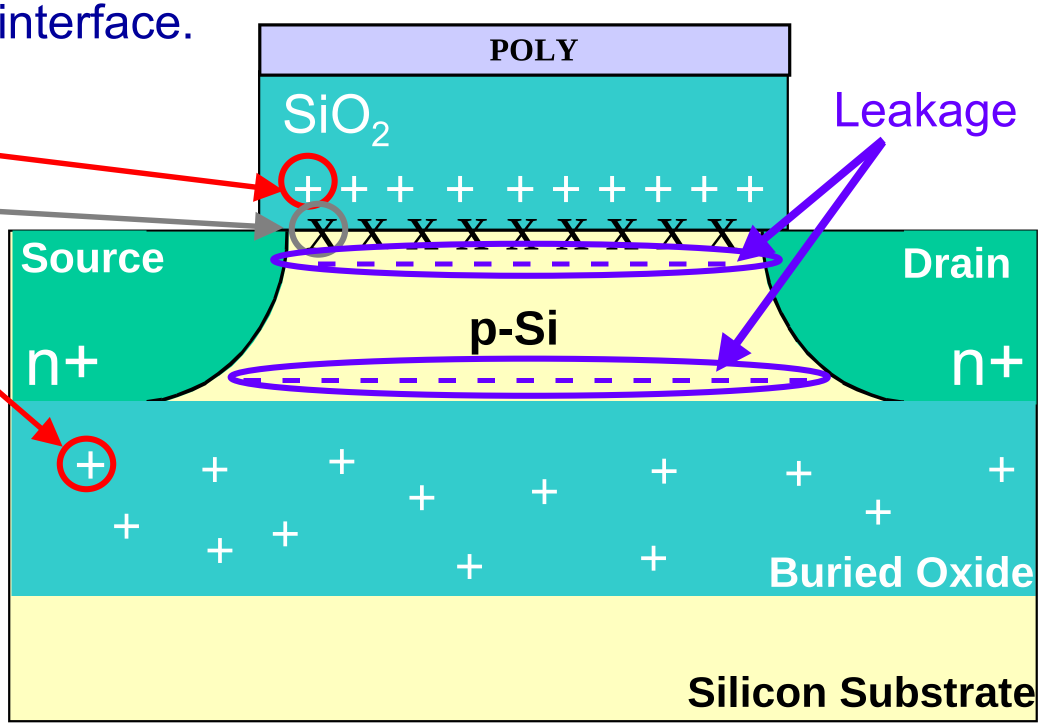


Total Dose Effects in MOS Devices

Charge trapping in SiO_2 and at Si/SiO_2 interface.

1. Oxide Trapping (N_{ot})
2. Interface Trapping (N_{it})

- Dominated by point defects



Metal/Semi Work Function; Fixed Charge; Mobile Ions; Interface Traps; Oxide Traps

$$V_{th} = V_{th}' + \phi_{MS} - \frac{Q_F}{C_O} - \frac{Q_M \gamma_M}{C_O} - \frac{N_{it} \bullet e \bullet (2\phi_f)}{C_{ox}} - \frac{N_{ot} \bullet e}{C_{ox}}$$

$$V_{th}' = 2\phi_F \pm (K_S / K_O) \chi_O \sqrt{\frac{4qN_B}{K_S \varepsilon_O}} \pm \phi_F$$

Basic Mechanisms

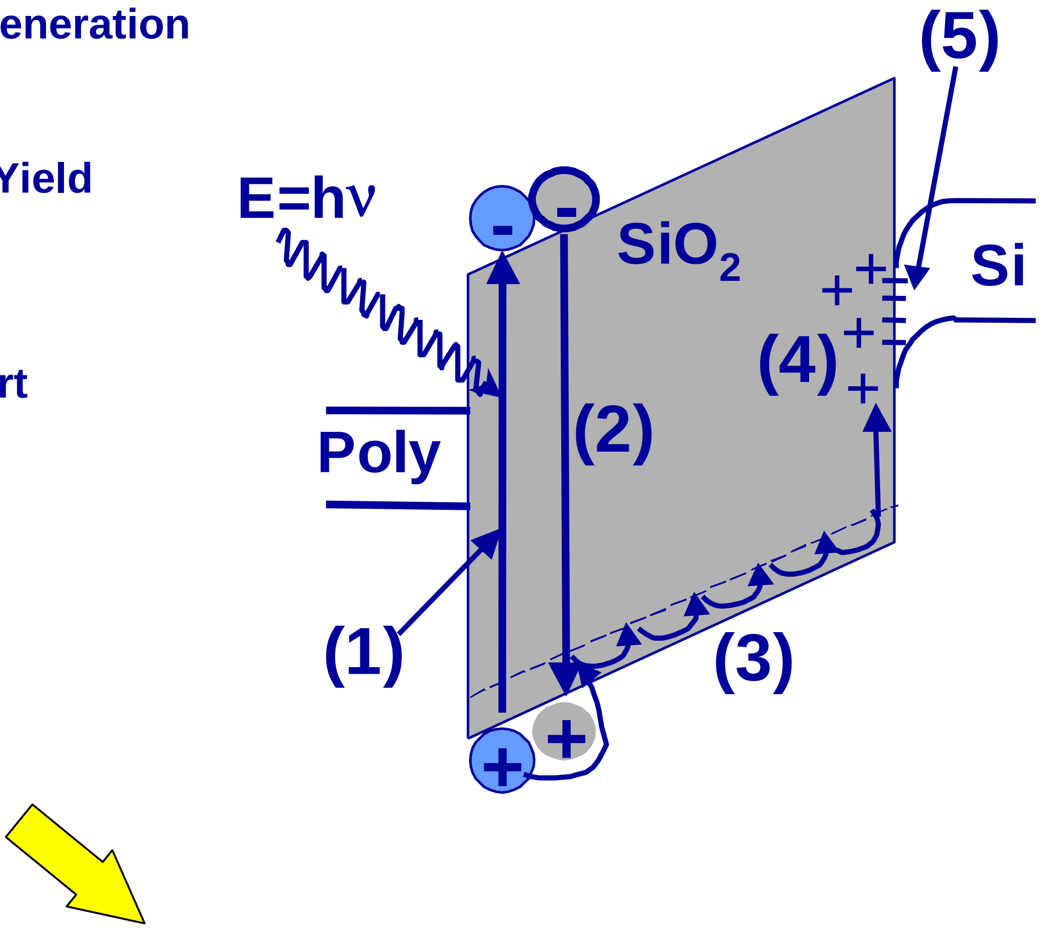
(1) Electron-Hole (e^-/h^+) Pair Generation
- **~17 eV / pair for SiO_2**

(2) e^-/h^+ Pair Recombination / Yield
- **Source**
- **Field**

(3) Electron and Hole Transport
- **e^- ~ psec**
- **h^+ ~ msec - sec**

(4) Hole Trapping
- **Precursor Density**
- **Cross section**

(5) Interface Trap Formation
- **Delayed buildup**



DEVICE PARAMETER SHIFT

What Is a rad?

1 rad = 100 erg / gram

 # electron-hole pairs (SiO_2) ~ 8.1×10^{12} /cm^3 / rad

Energy Unit Conversion of rad

ρ_{SiO_2}

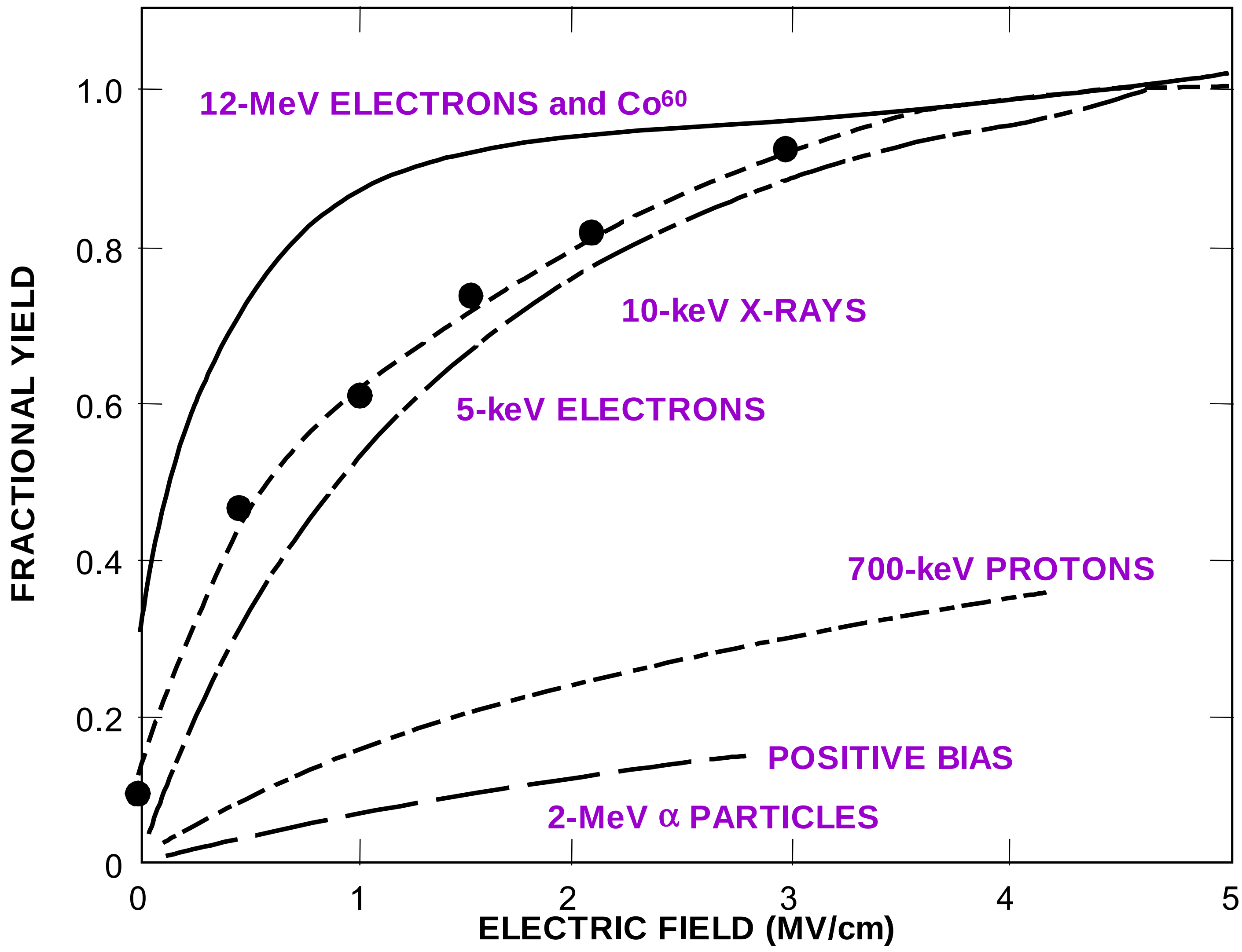
$$\frac{\#\ \text{pairs}}{\text{rad}\cdot\text{cm}^3} = \frac{\left[\left(\frac{100\ \text{ergs}}{\text{gram}}\right)\left(\frac{10^{-7}\ \text{J}}{\text{erg}}\right)\left(\frac{\text{eV}}{1.6\times10^{-19}\ \text{J}}\right)\right] \cdot (2.2\ \text{g} / \text{cm}^3)}{17 \pm 1\ \text{eV}}$$

17 +/- 1 eV

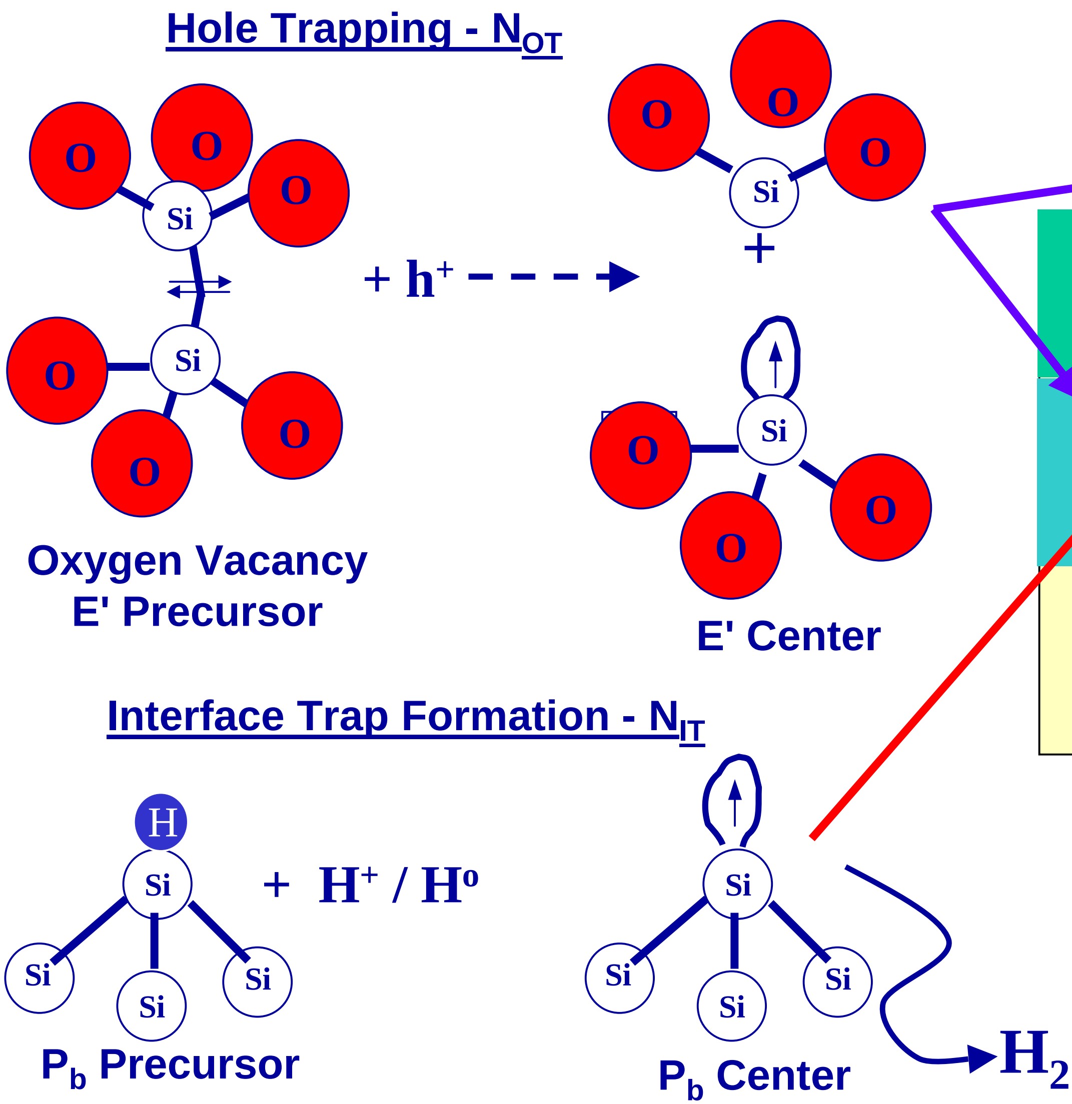
(electron-hole pair creation energy in SiO_2)

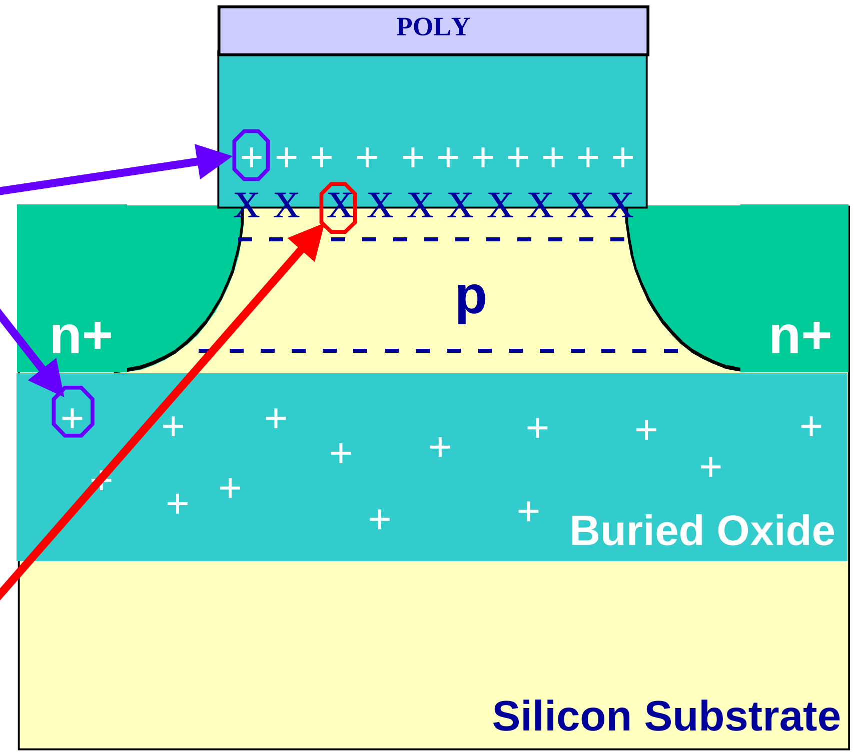
Recombination and Yield

- Radiation source and oxide field dependent



Total Dose Defects in MOS Devices



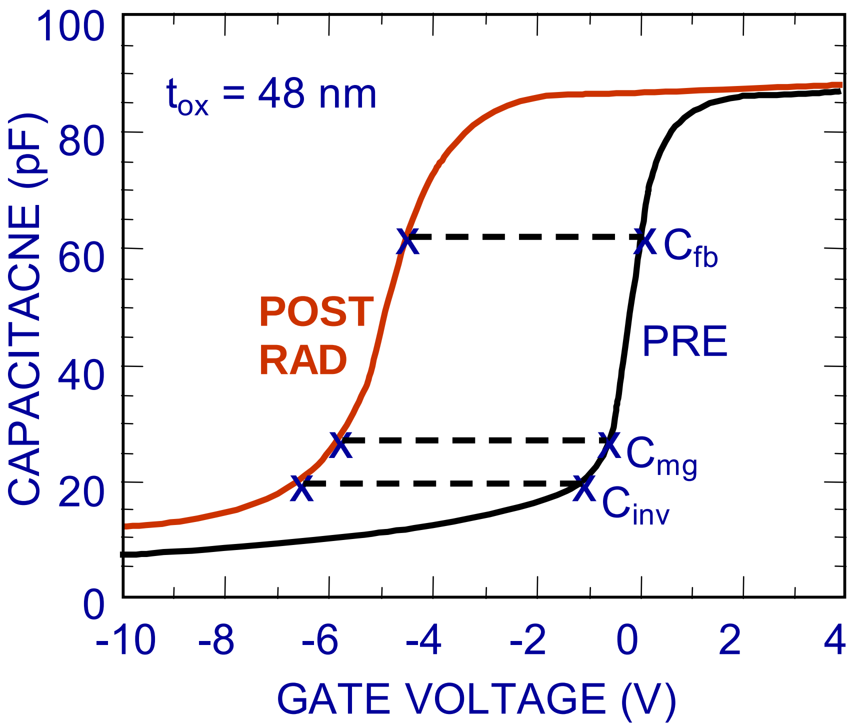


Radiation Damage Participants

E', P_b, P_b H, E'H, H^+, H^0, H_2, h^+

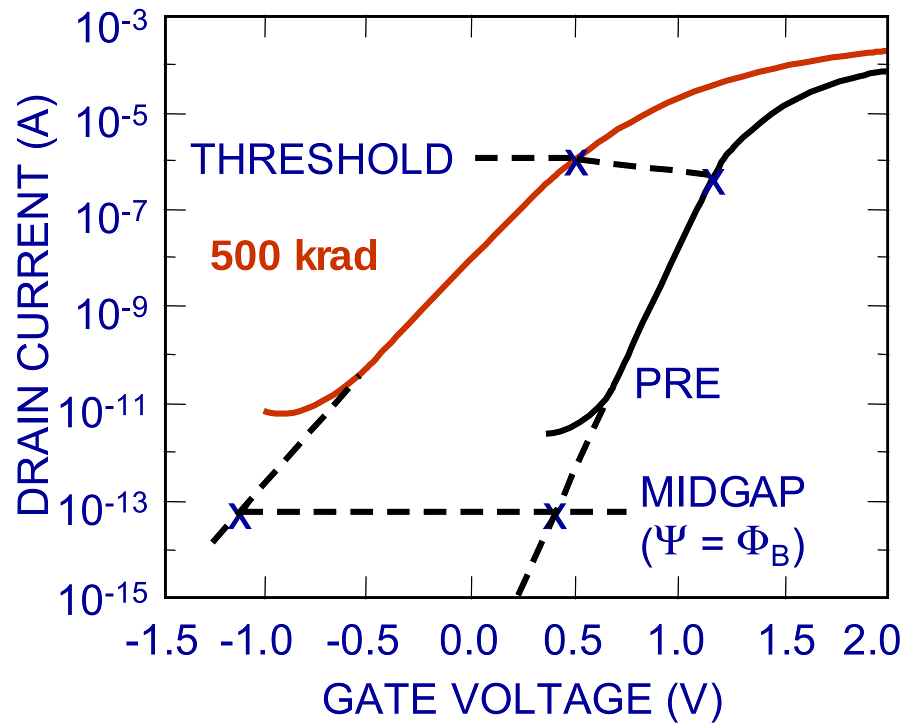
Influence of Hole Traps and Interface Traps on CV and IV Curves

CV



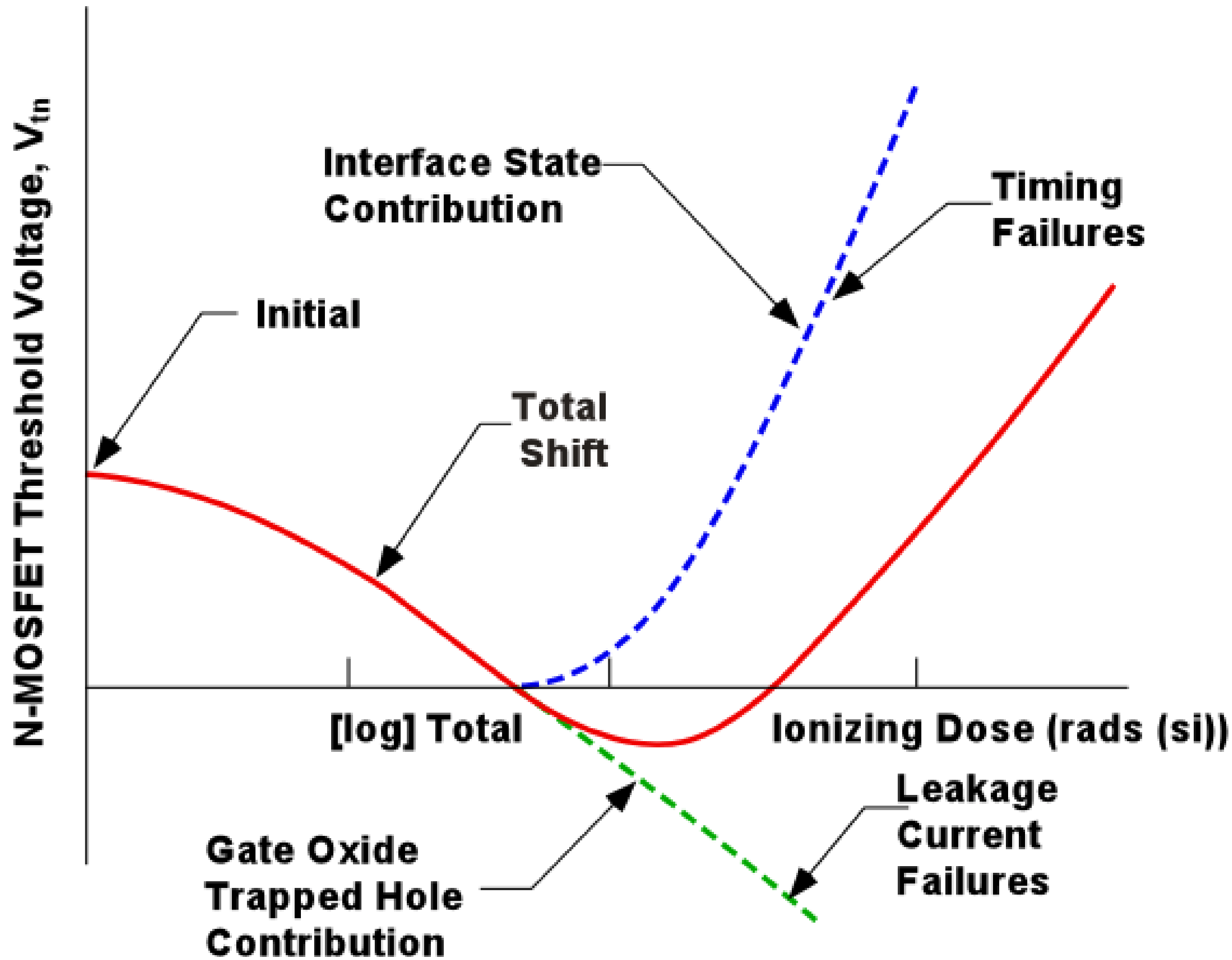
(a)

IV



(b)

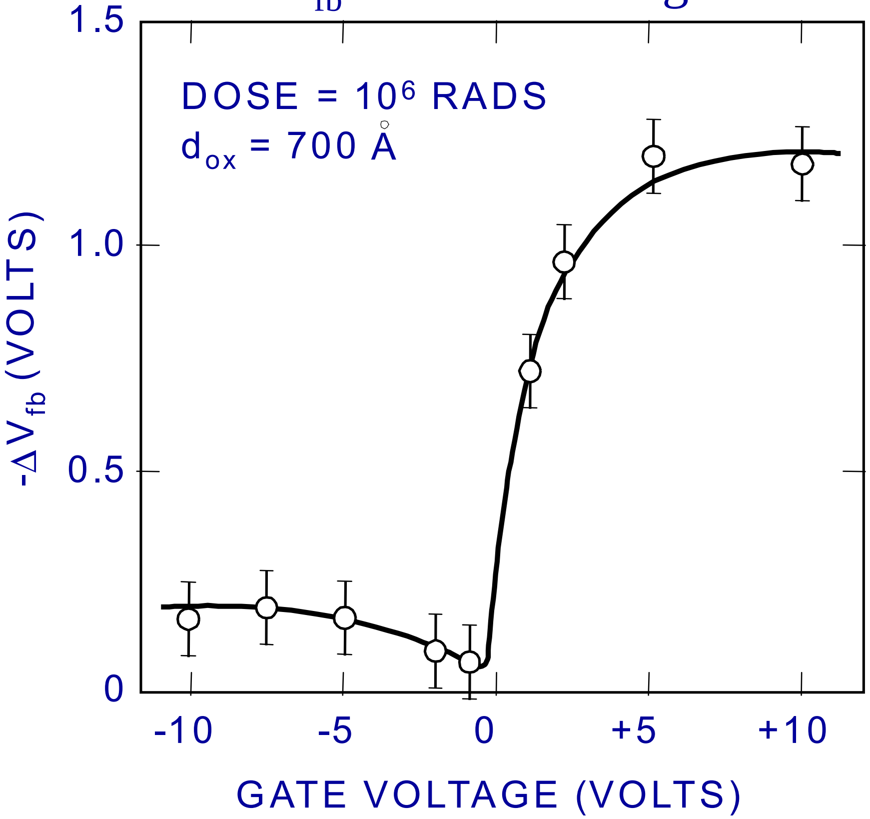
Influence of Interface and Oxide Trapped Charge



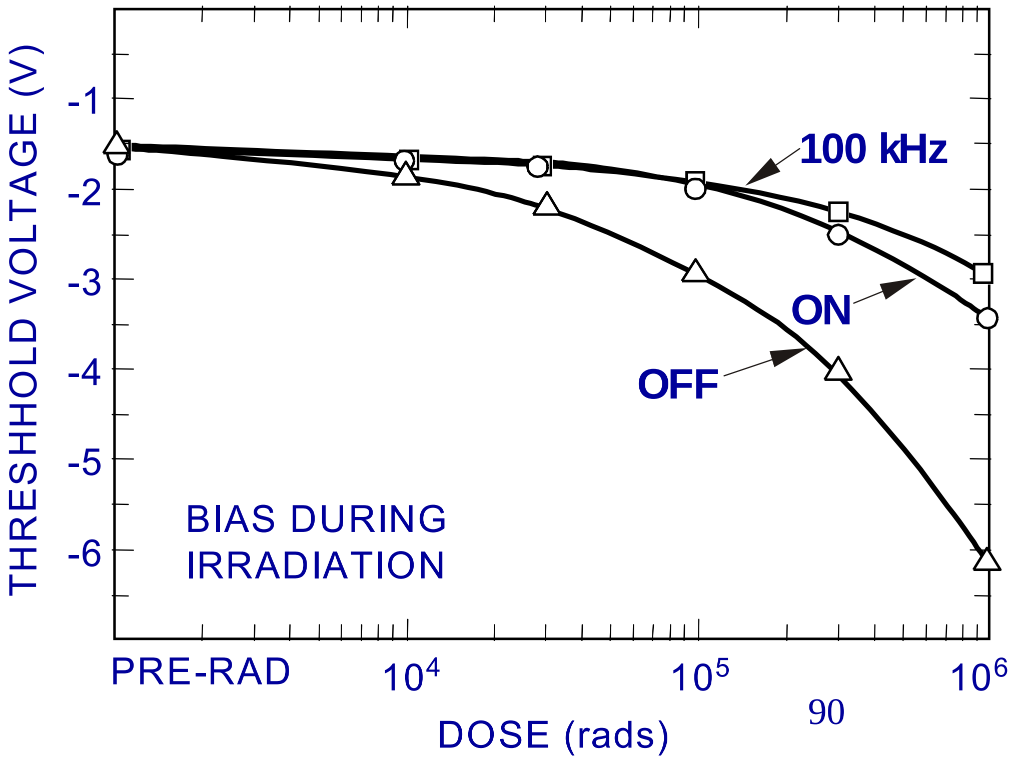
Effects of Bias

- Bias has a strong influence on the radiation response
- Powering down a device can sometimes improve radiation response
- A powered device is not always worst case

ΔV_{fb} vs. Gate Voltage



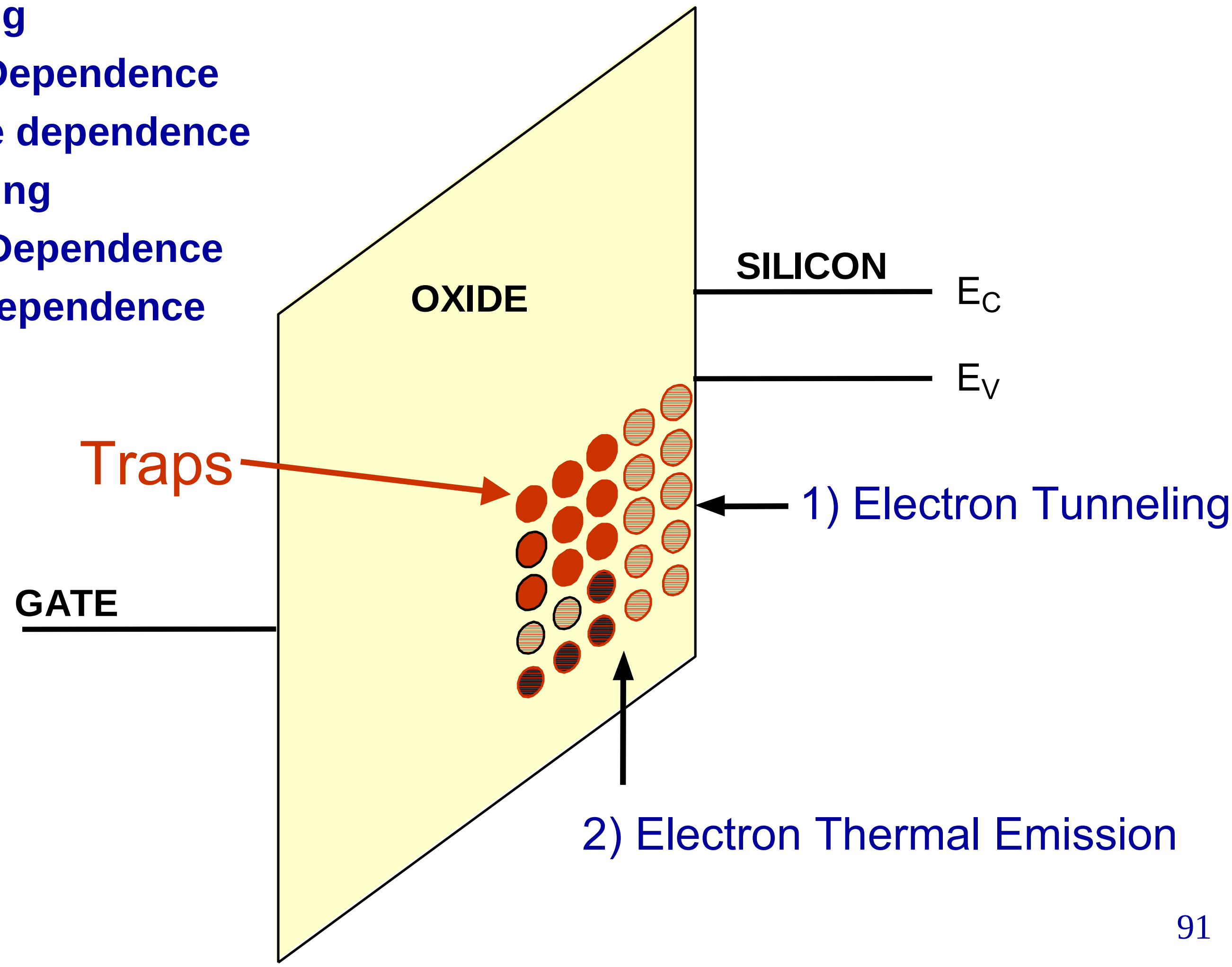
Dynamic vs. Static Bias



Annealing

1) Tunnel Annealing
- **Spatial Dependence**
- **Log time dependence**

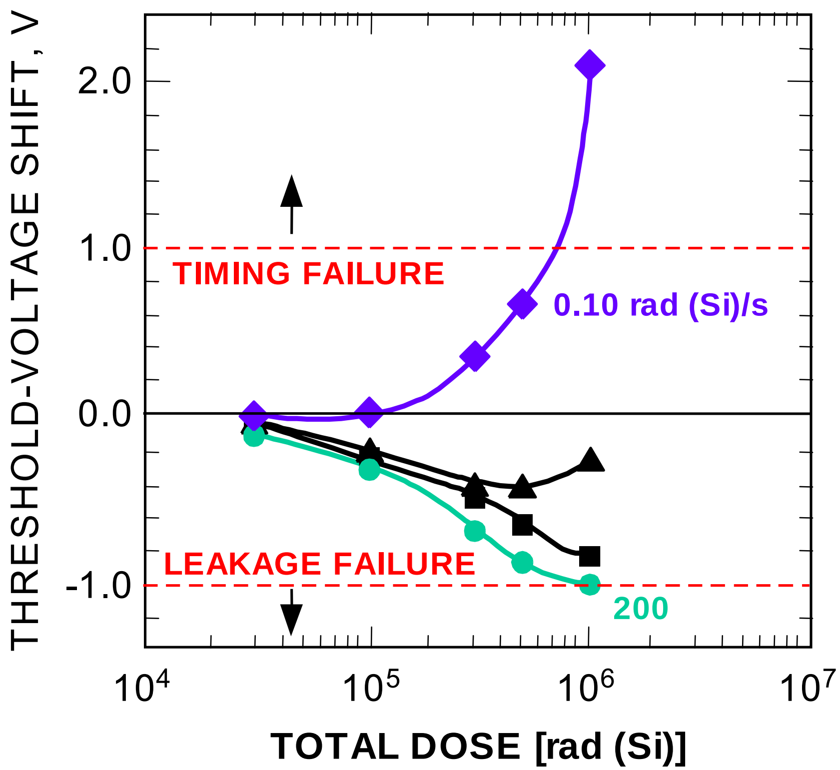
2) Thermal Annealing
- **Energy Dependence**
- **Temp. Dependence**



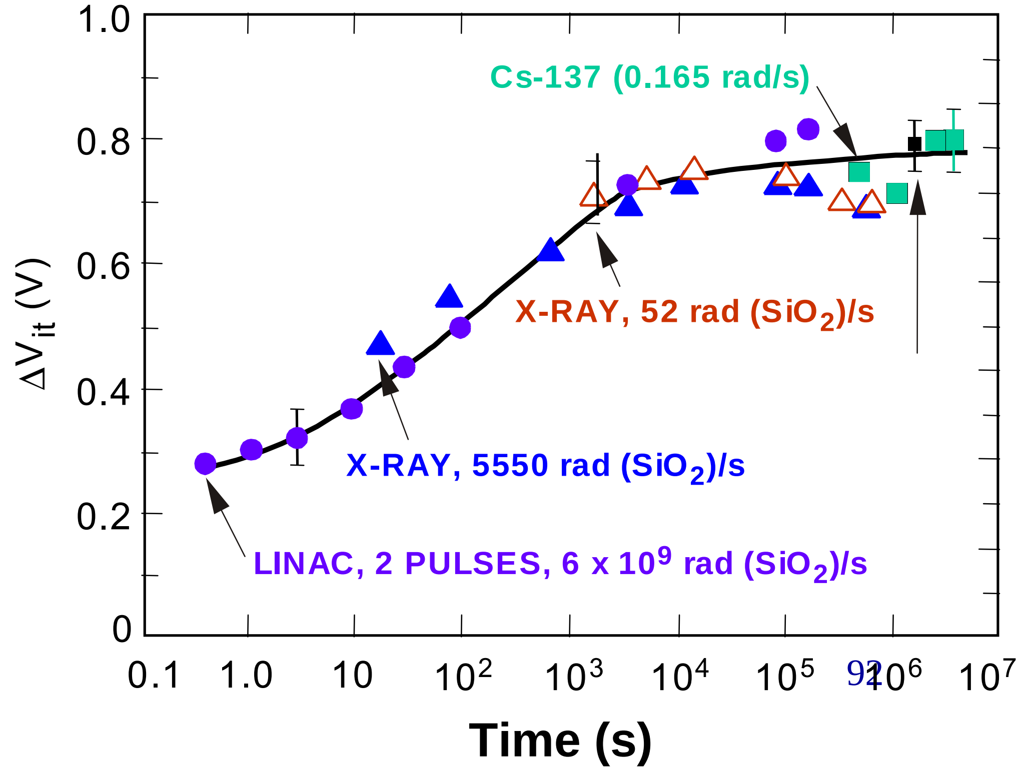
Dose Rate Effects

- Hole traps and interface traps build-up and anneal on different time scales.
- Irradiation at different dose rates can produce different failure mechanisms and total dose hardness.
- When time is considered, dose rate effects in CMOS disappear.

ΔV_{th} vs. Dose



ΔV_{it} vs. Time



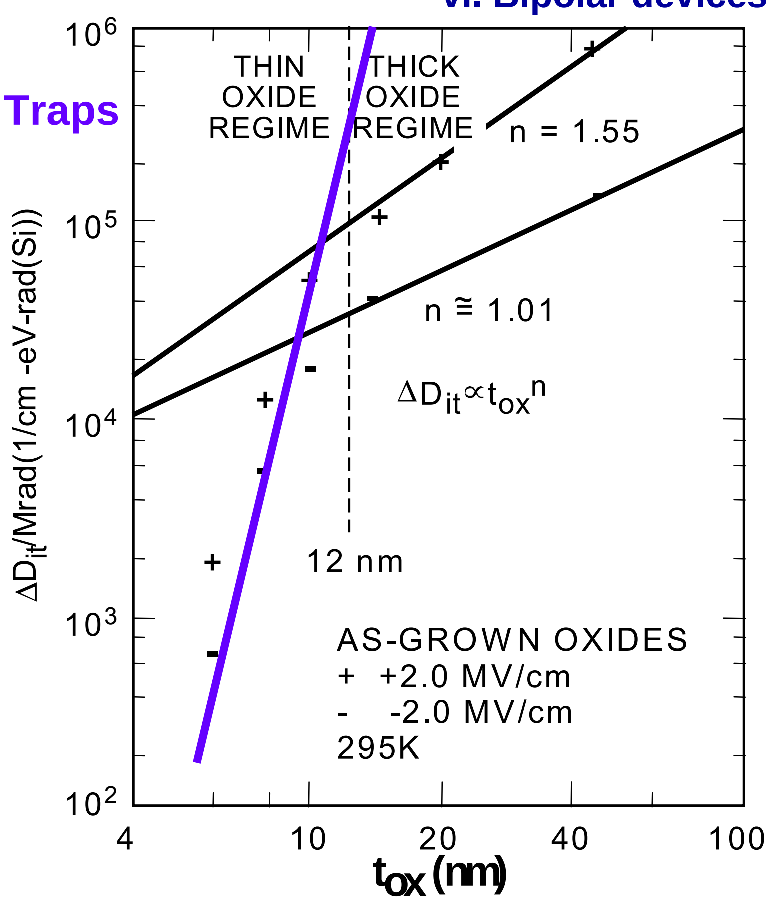
Oxide Thickness

Trapping drops off steeply in thin oxides but there are still problems:

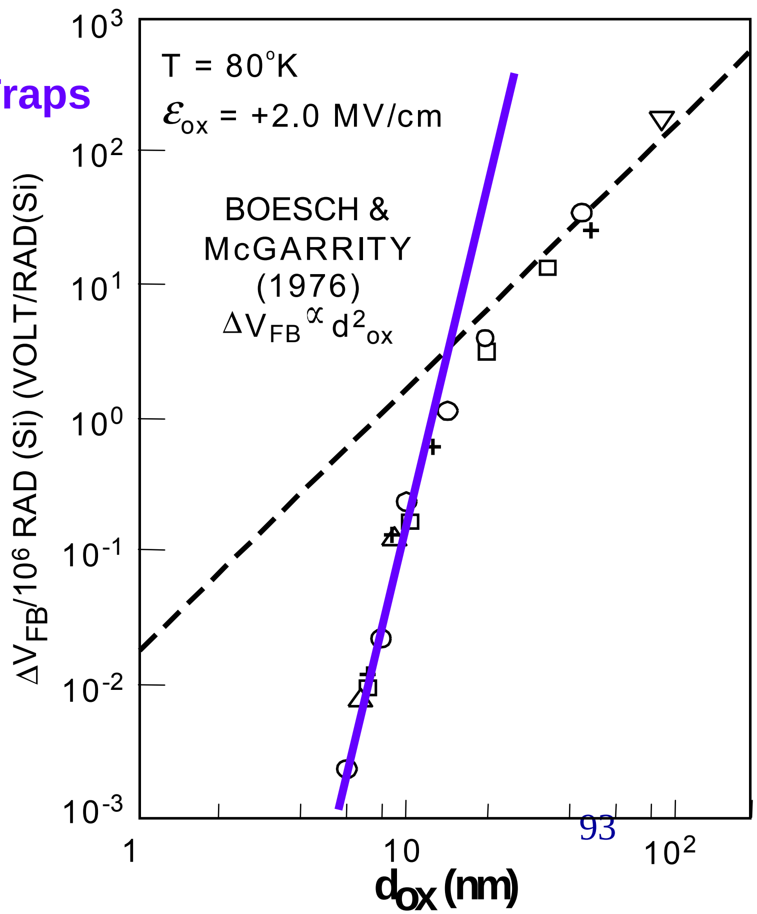
1) Radiation Induced Leakage Currents (RILC) in ultrathin oxides

2)Thick oxides:
- **i. Power MOSFETs**
- **ii. Field oxides**
- **iii. Silicon-on-insulator (SOI) buried oxides**
- **vi. Bipolar devices.**

Interface Traps

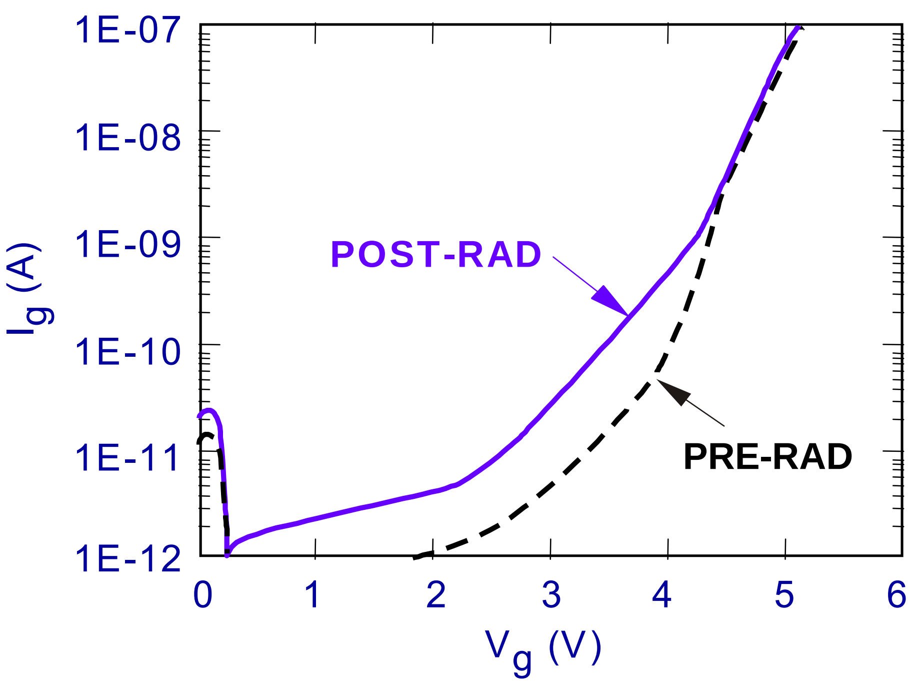


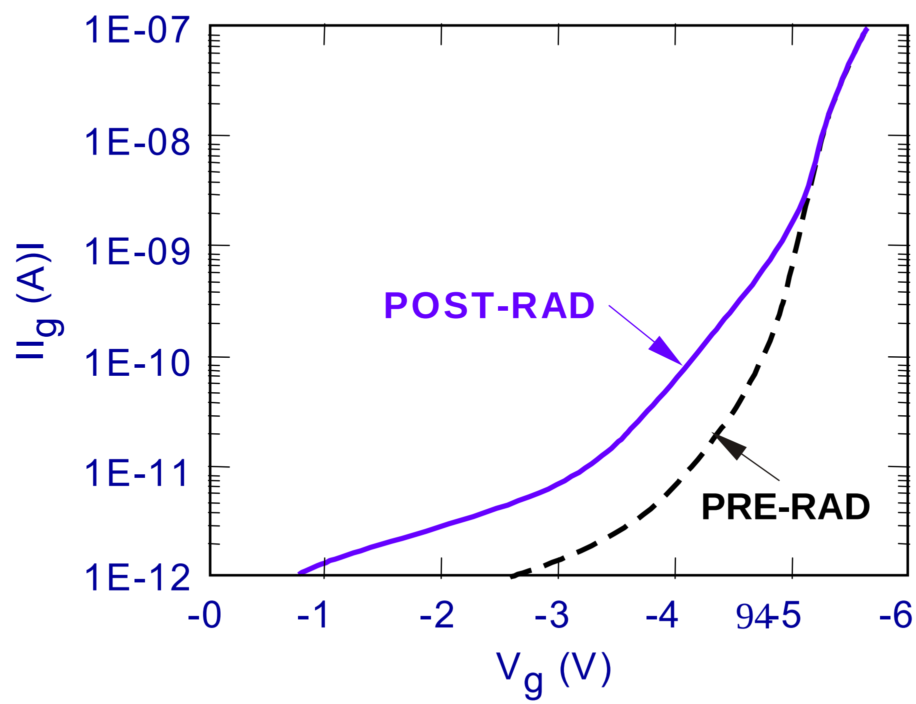
Hole Traps



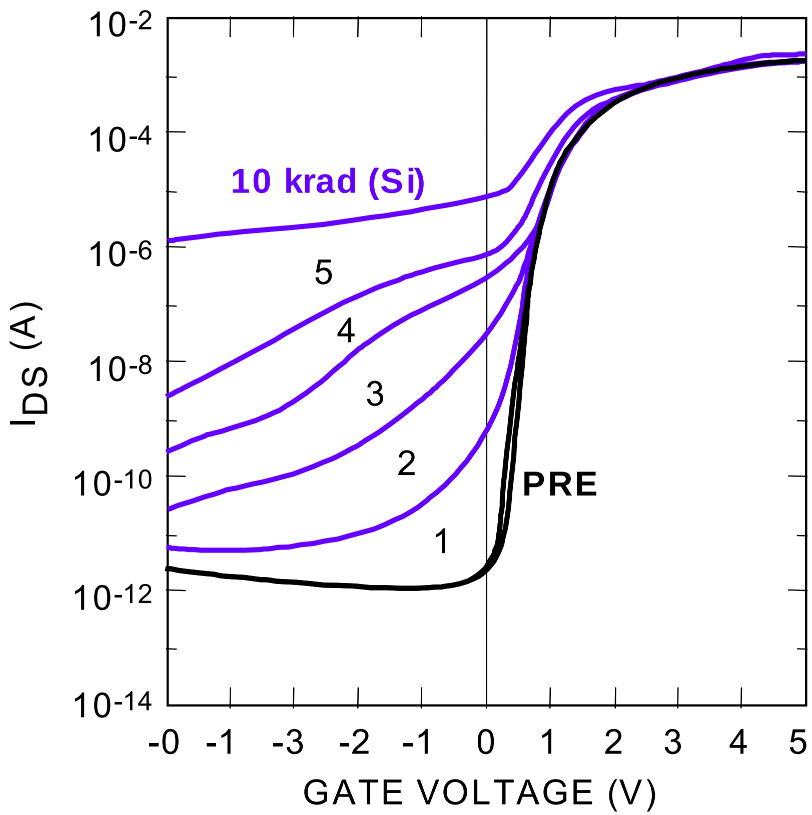
Radiation Induced Leakage Current (RILC)

- Reported in thin oxides (<10 nm) at high doses (>1Mrad).
- Similar to stress induced leakage current (SILC).
- Thought to be due to trap assisted tunneling.
- Possible failure mechanism for flash memories.

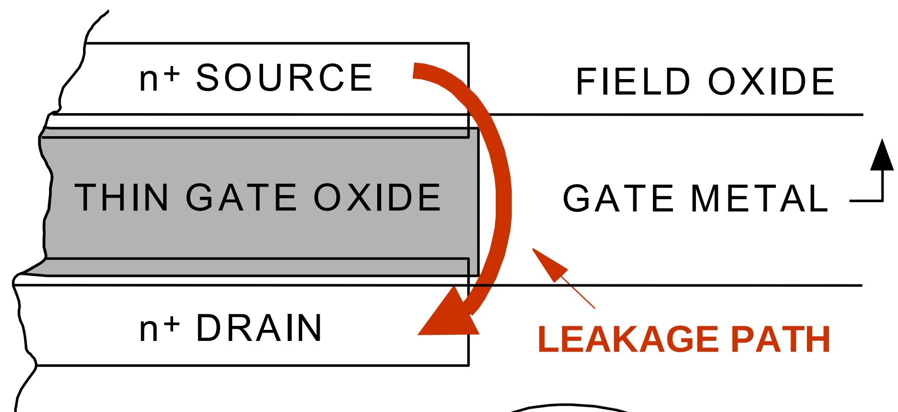


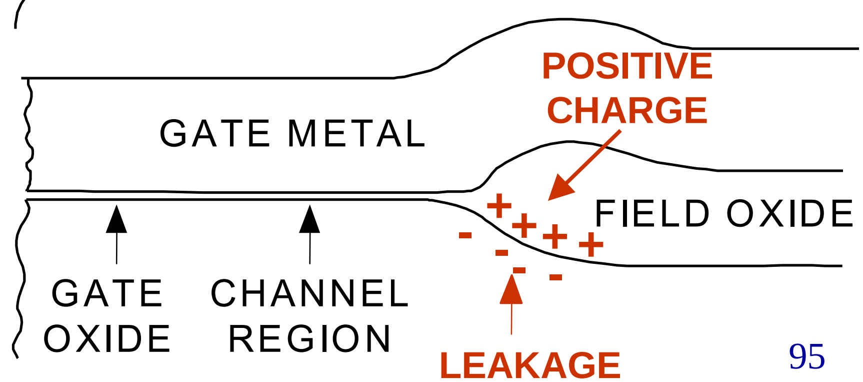


Field Oxide Leakage



- **Field oxides thick and poorly controlled.**
- **Dominant failure mechanism for commercial processes.**
- **Geometry is critical.**





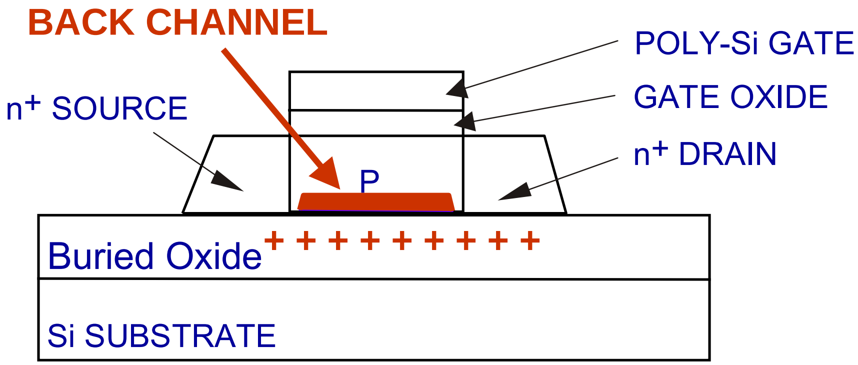
Silicon-on-Insulator (SOI)

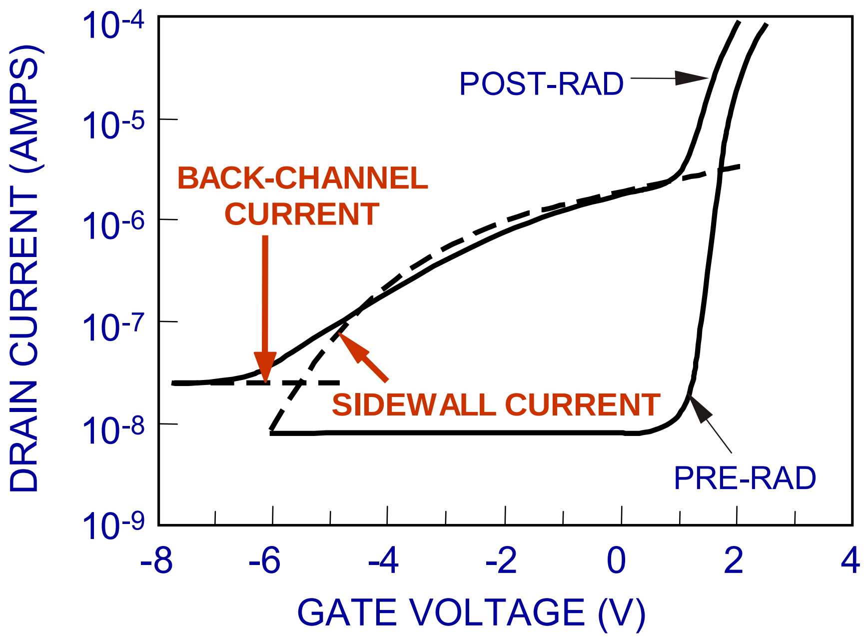
SOI Advantages:

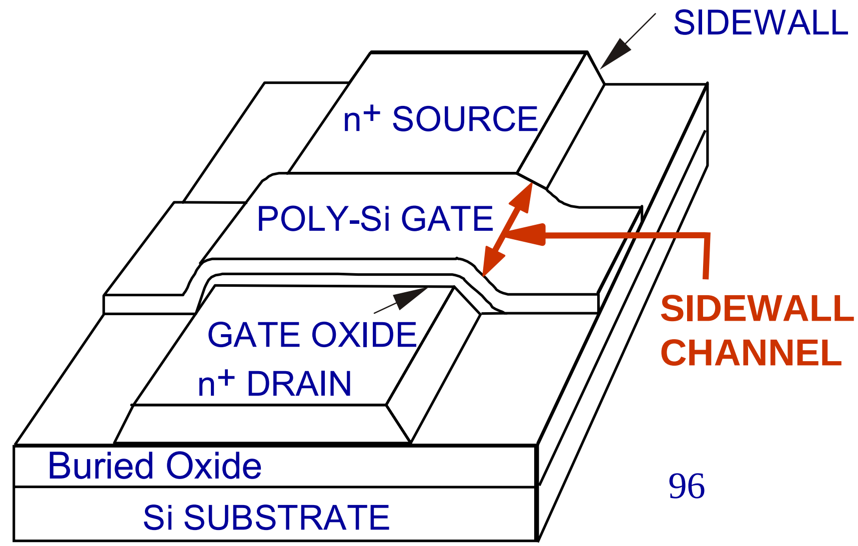
1. **Total Isolation**
2. **SEU Immune**
3. **High Speed**
4. **Low Power**
5. **Latchup Eliminated**

New SOI Total Dose Leakage Paths:

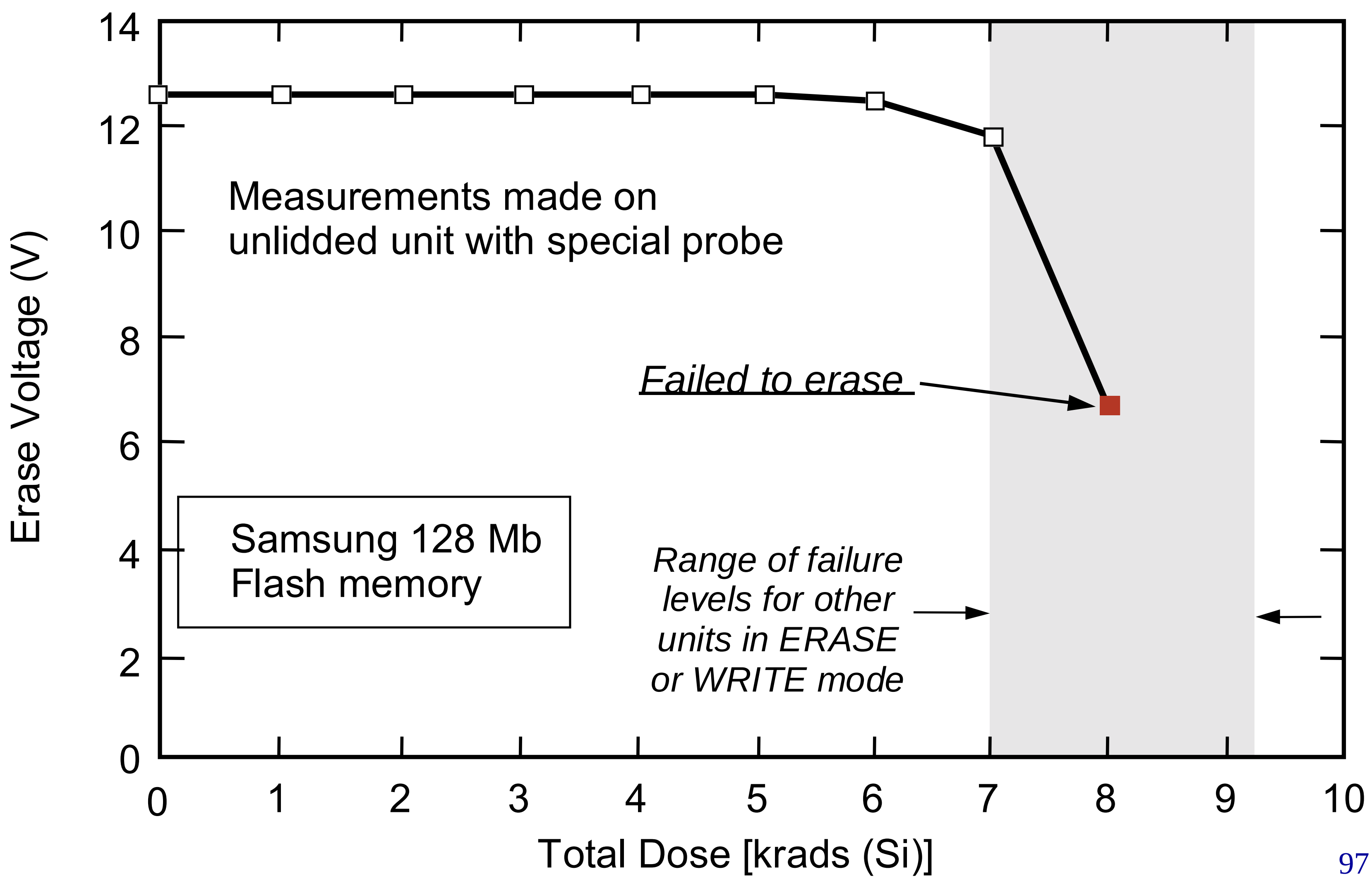
1. **Back Channel Leakage**
2. **Sidewall Leakage**





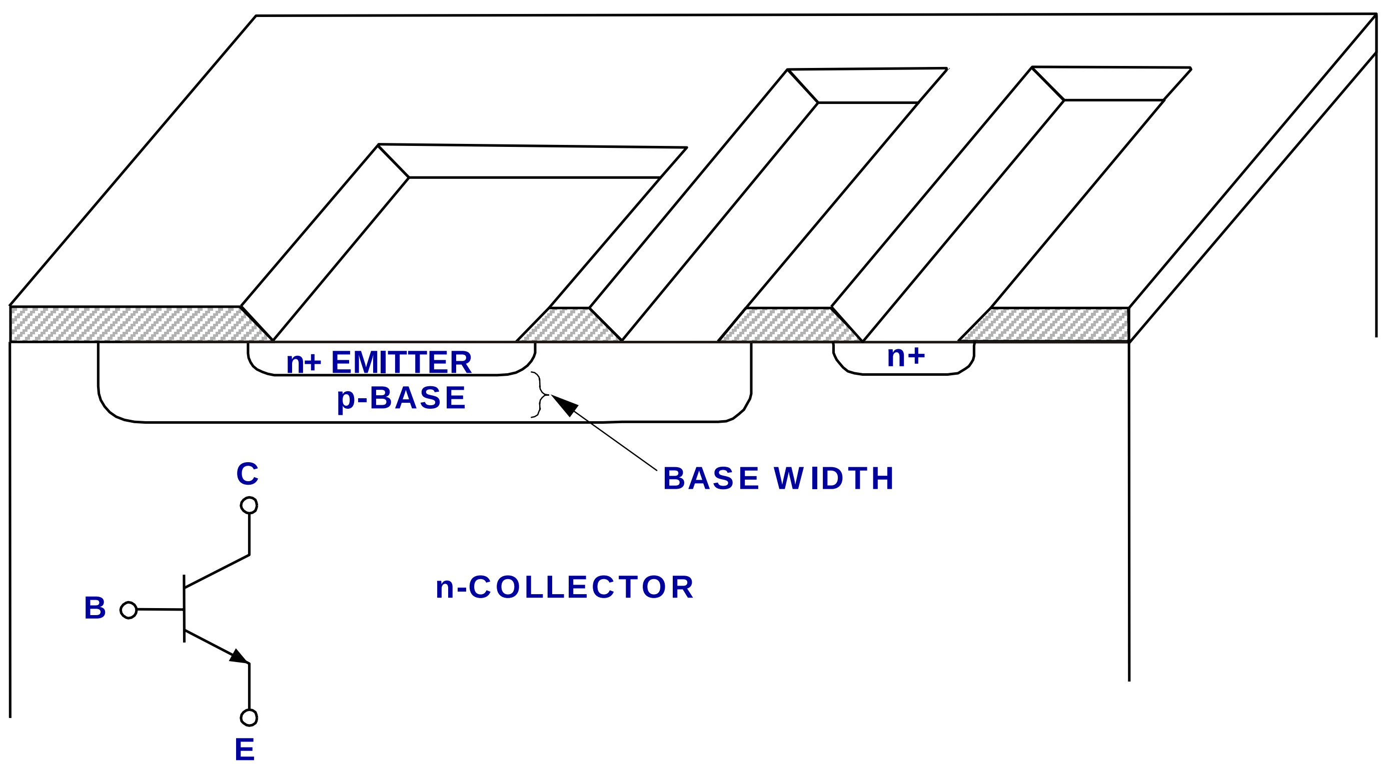


Flash Memories

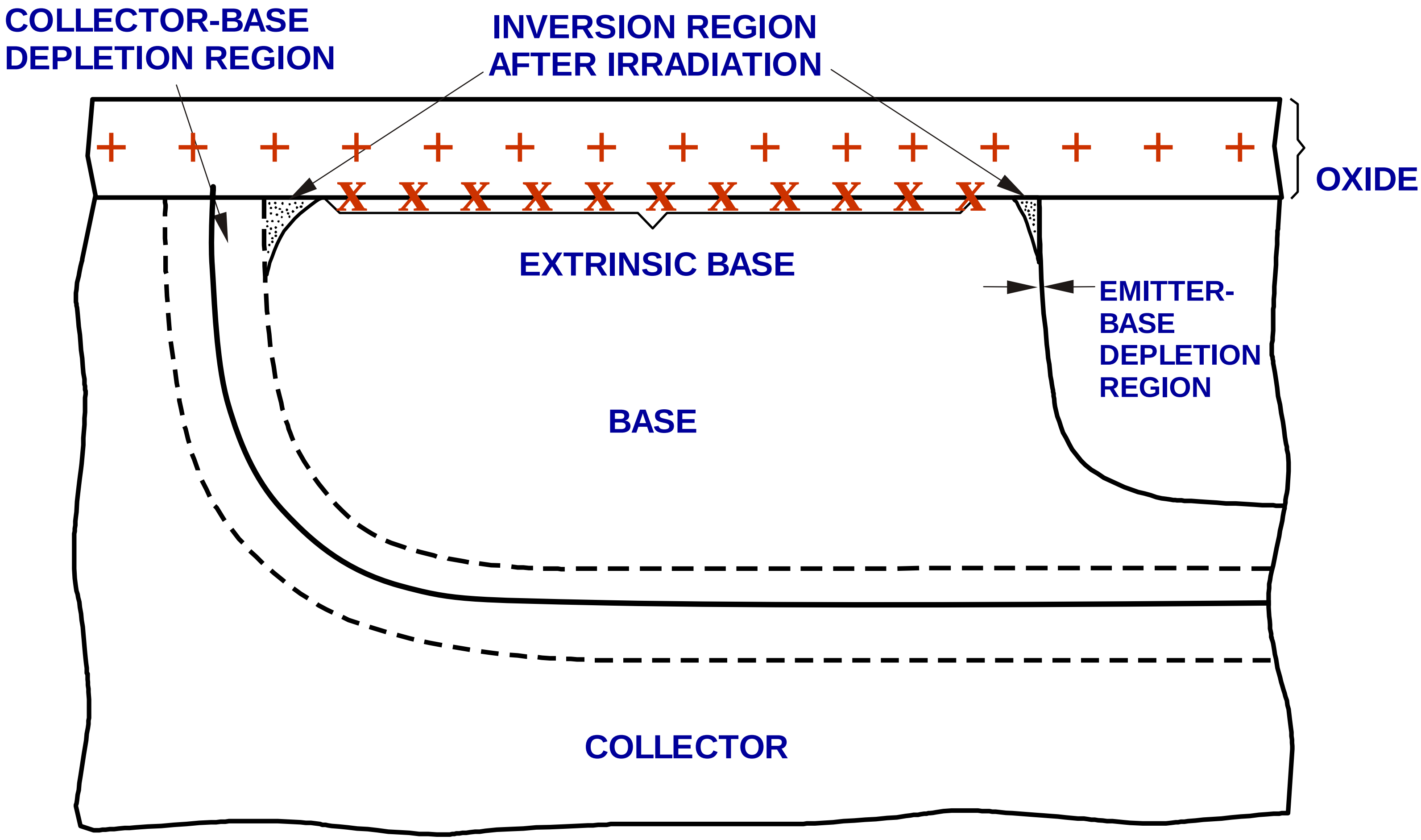


Linear BJT

Structure of a bipolar transistor

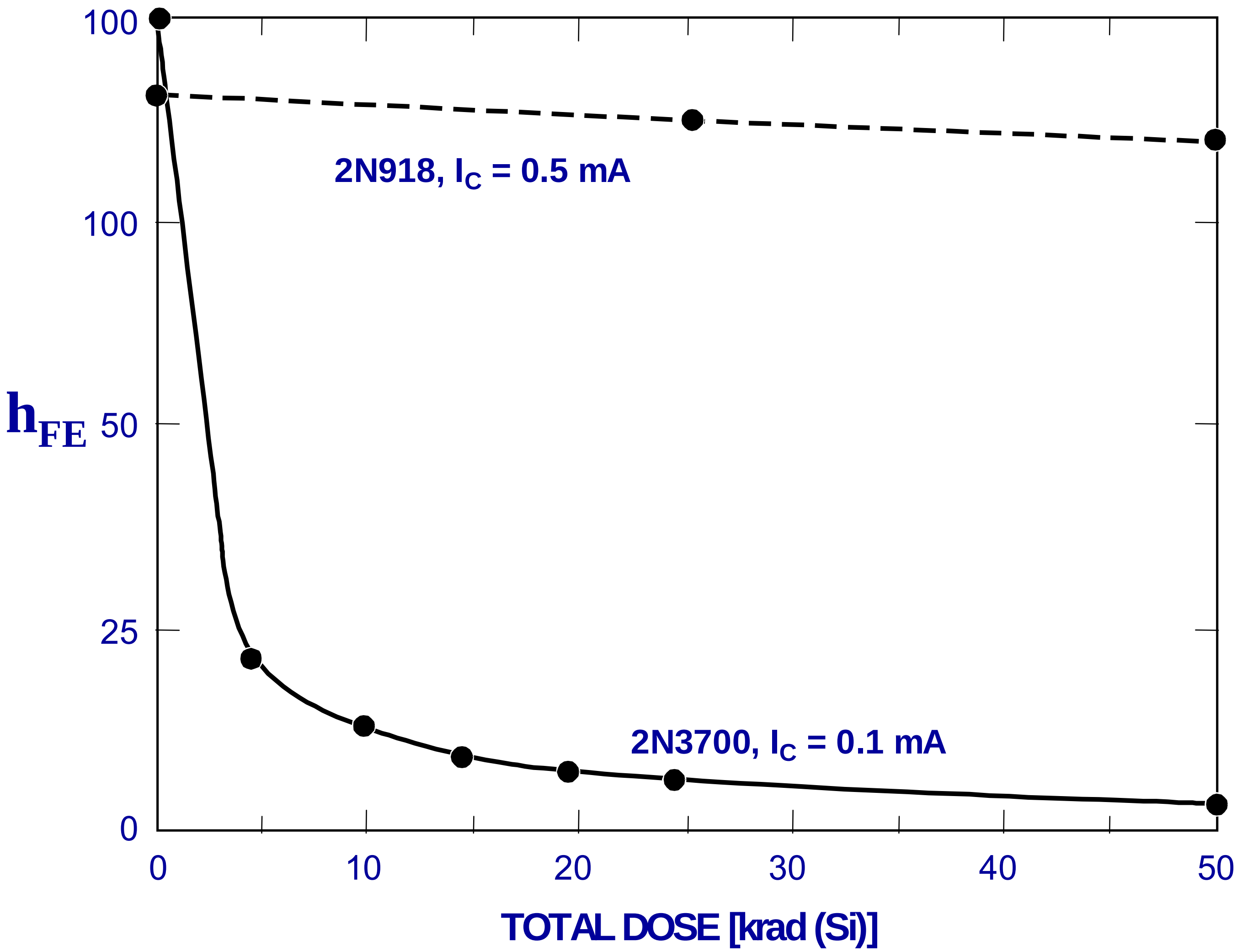


Bipolar Transistor: Gain Degradation

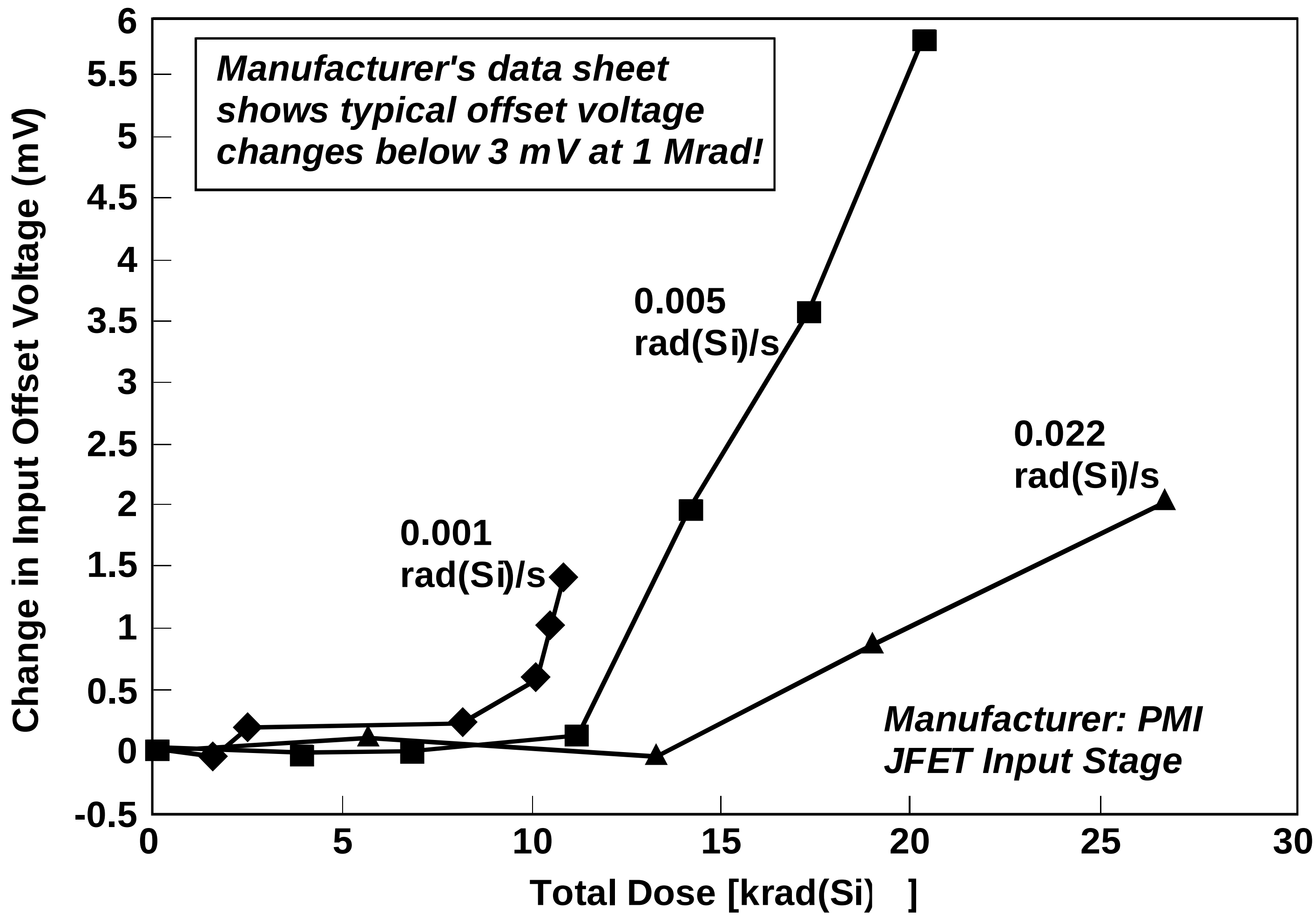


- Charge trapped at and near the interface above the base region can degrade gain and increase leakage.

Gain Degradation of Two Transistor Types Used on Cassini

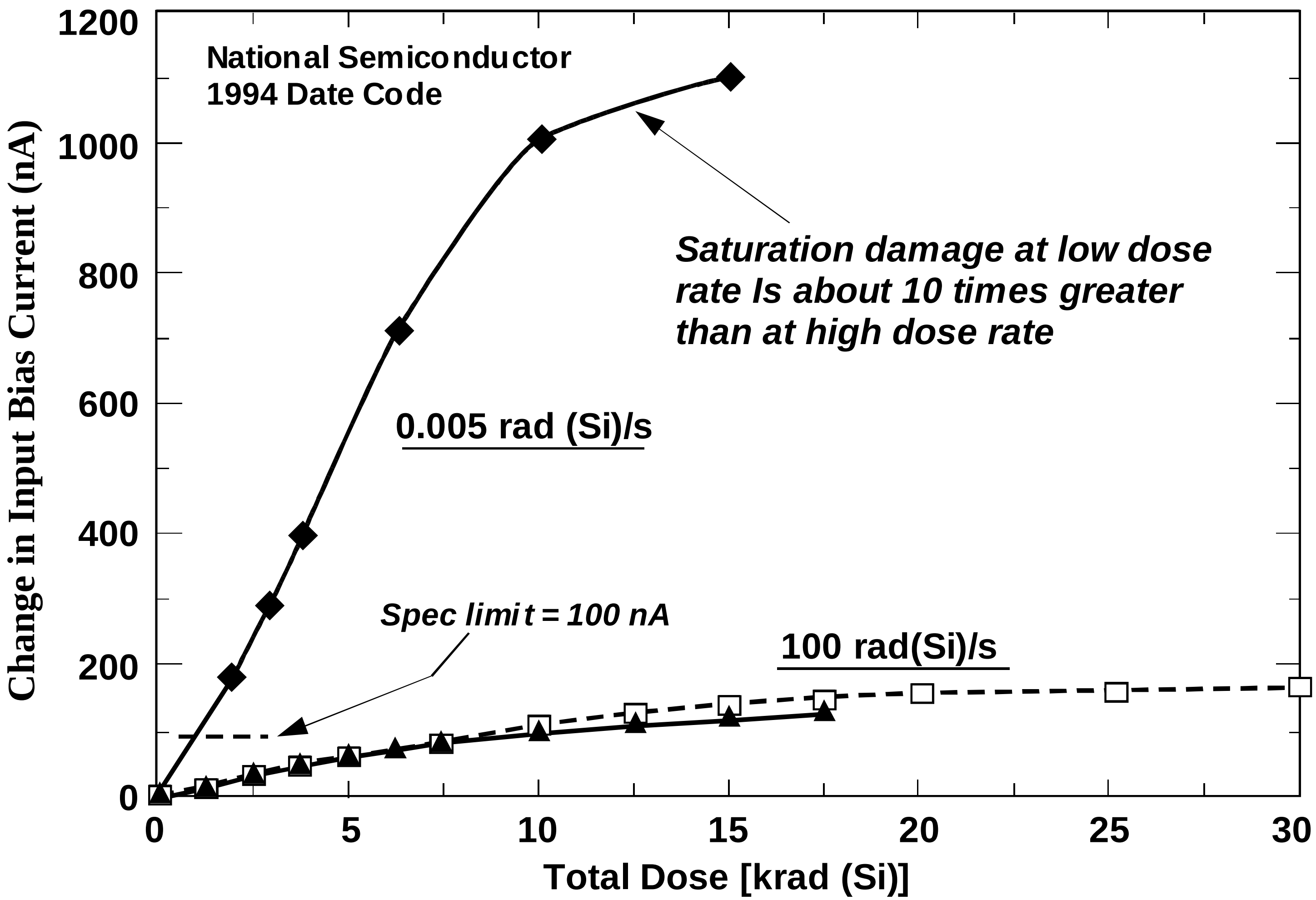


Extremely Low Dose Rate Sensitivity (ELDRS)

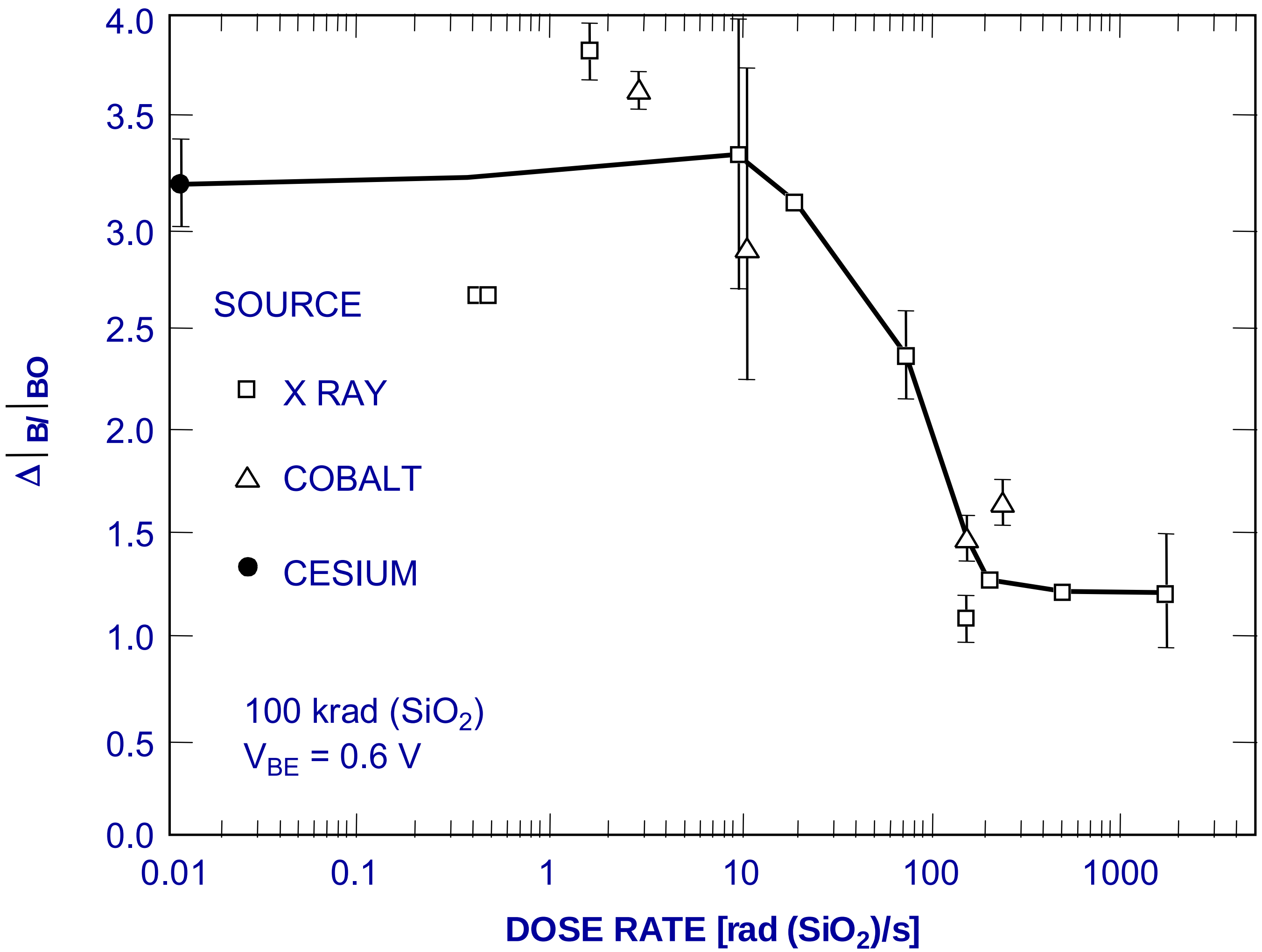


- Some bipolar device show extreme degradation at low dose rates.

ELDRS: Effect of Dose Rate on I_b for LM111 Comparator

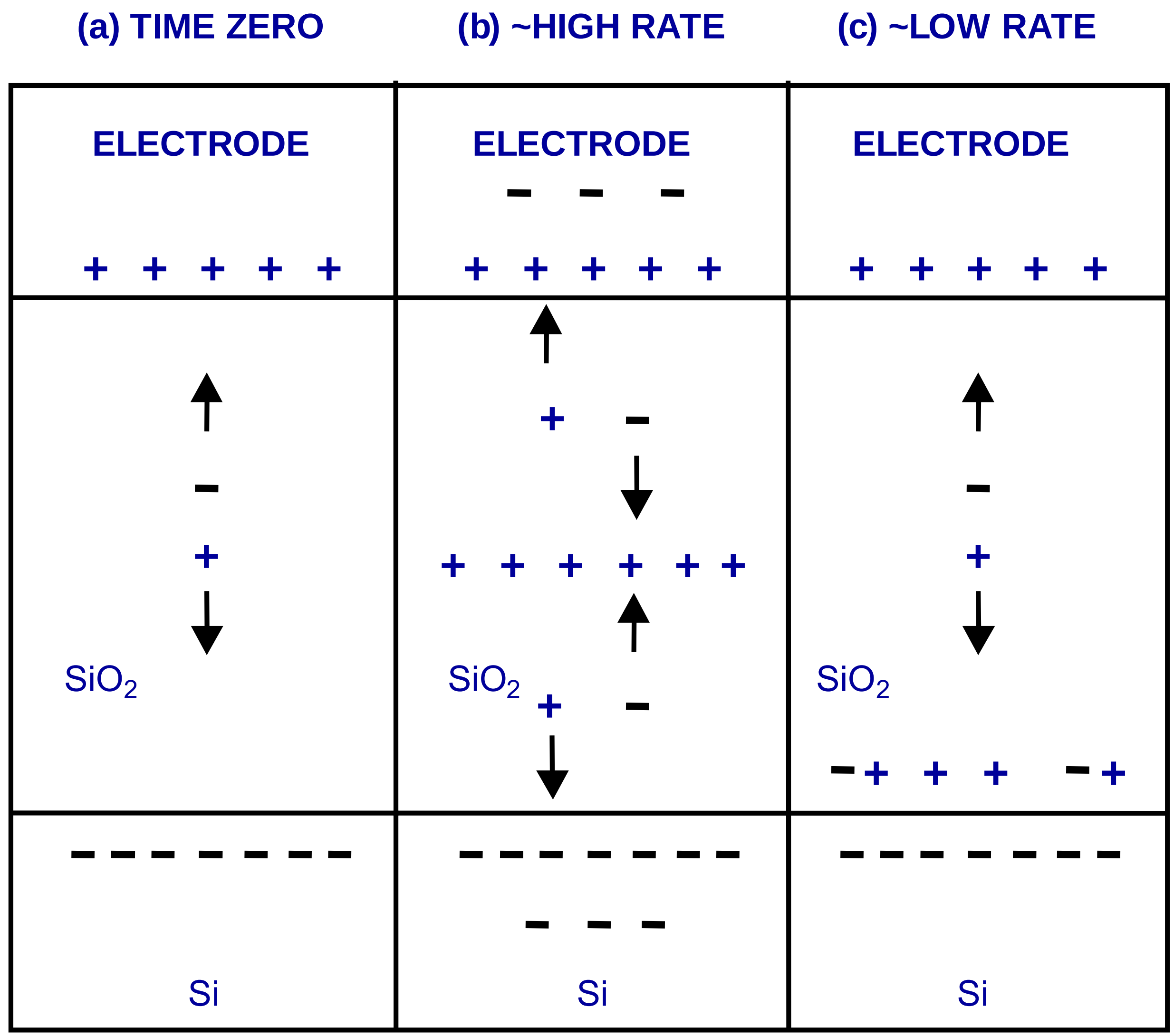


ELDRS

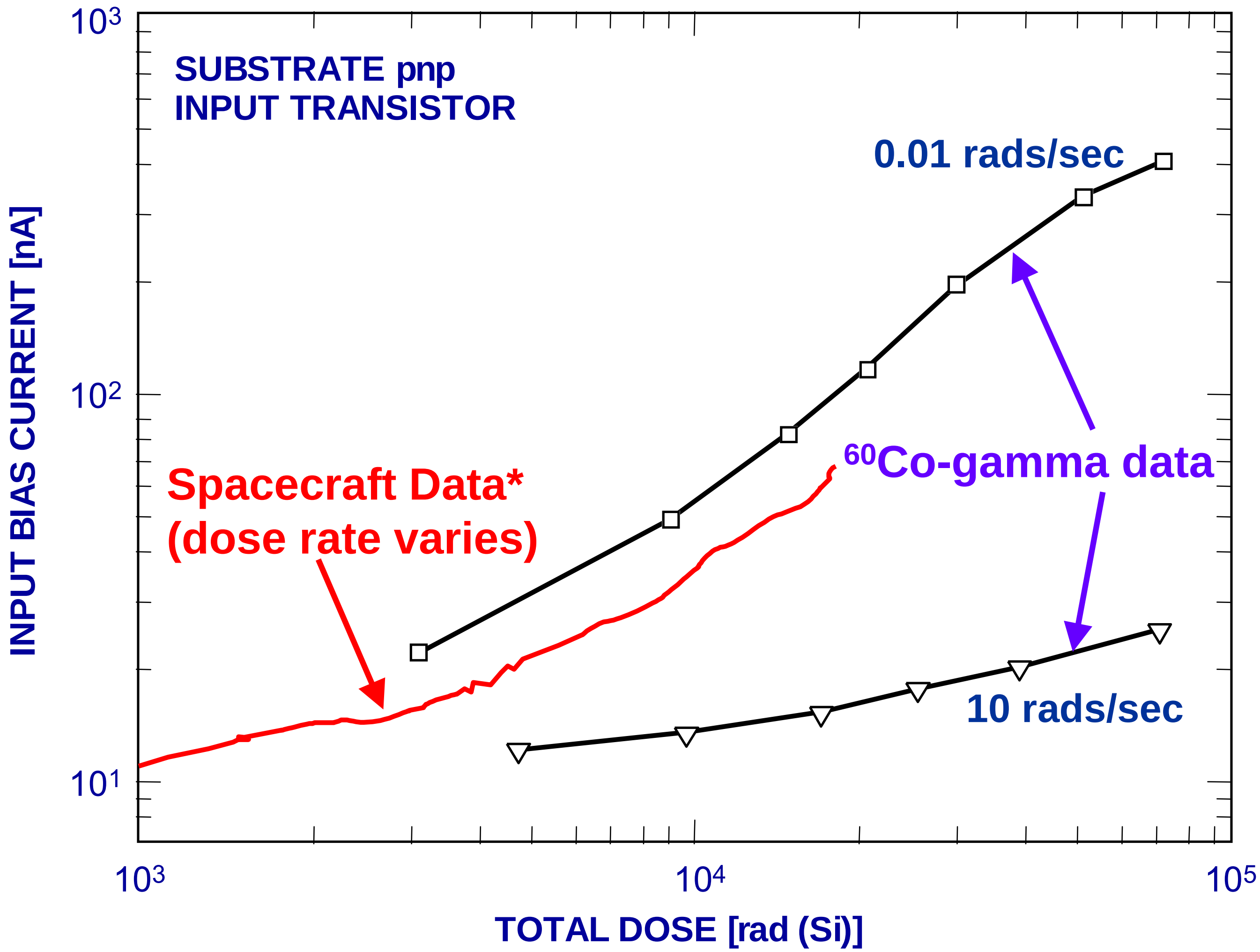


4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
0.01
0.1
1
10
100
1000
DOSE RATE [rad (SiO2)/s]
SOURCE
X RAY
COBALT
CESIUM
100 krad (SiO2)
VBE = 0.6 V

ELDRS Degradation Model - Space Charge Effects



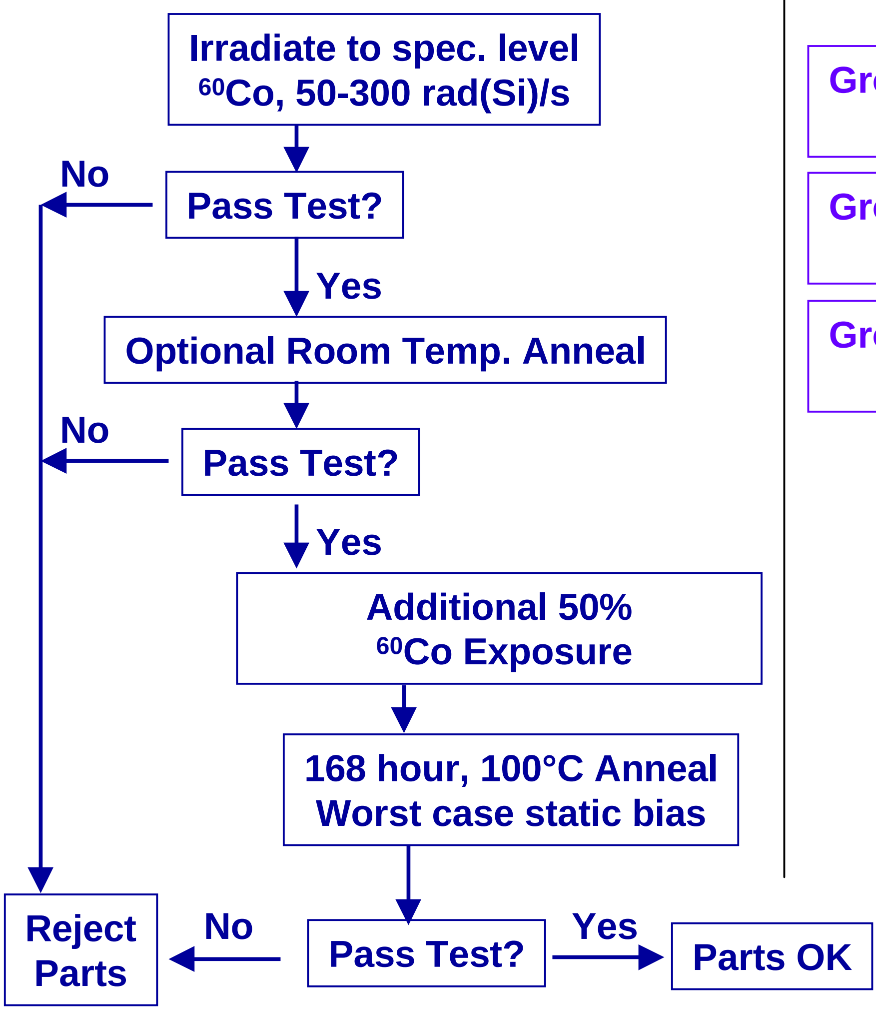
ELDRS in Space: LM124 Op-Amp



*Titus et al., IEEE Trans. Nucl. Sci. 46, 1608 (1999).

Testing

MOS Testing: MIL-STD 883D, 1019



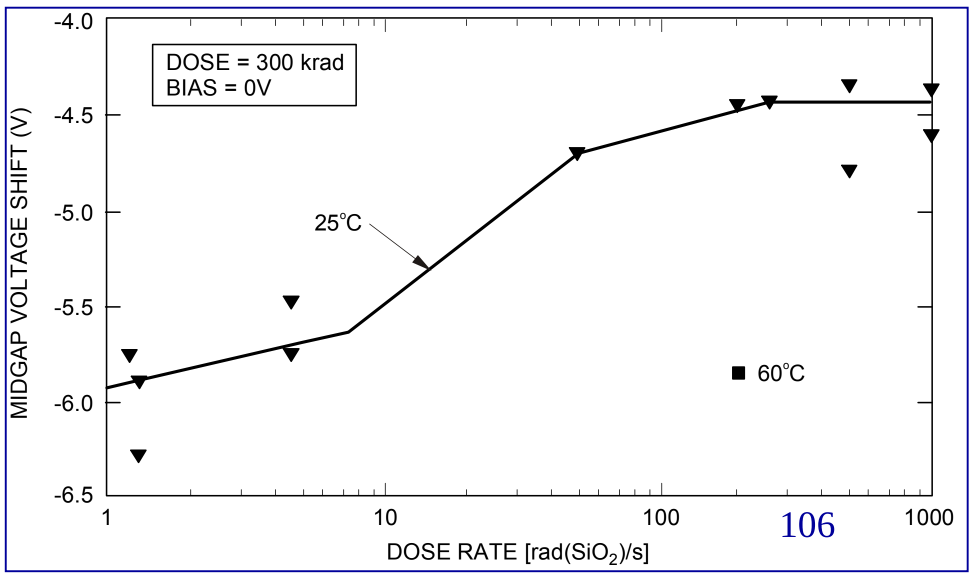
BiPolar/ELDR: ASTM F-1892 Pre-screen

Group 1: Irradiate at ~50 rad(Si)/s & 25°C

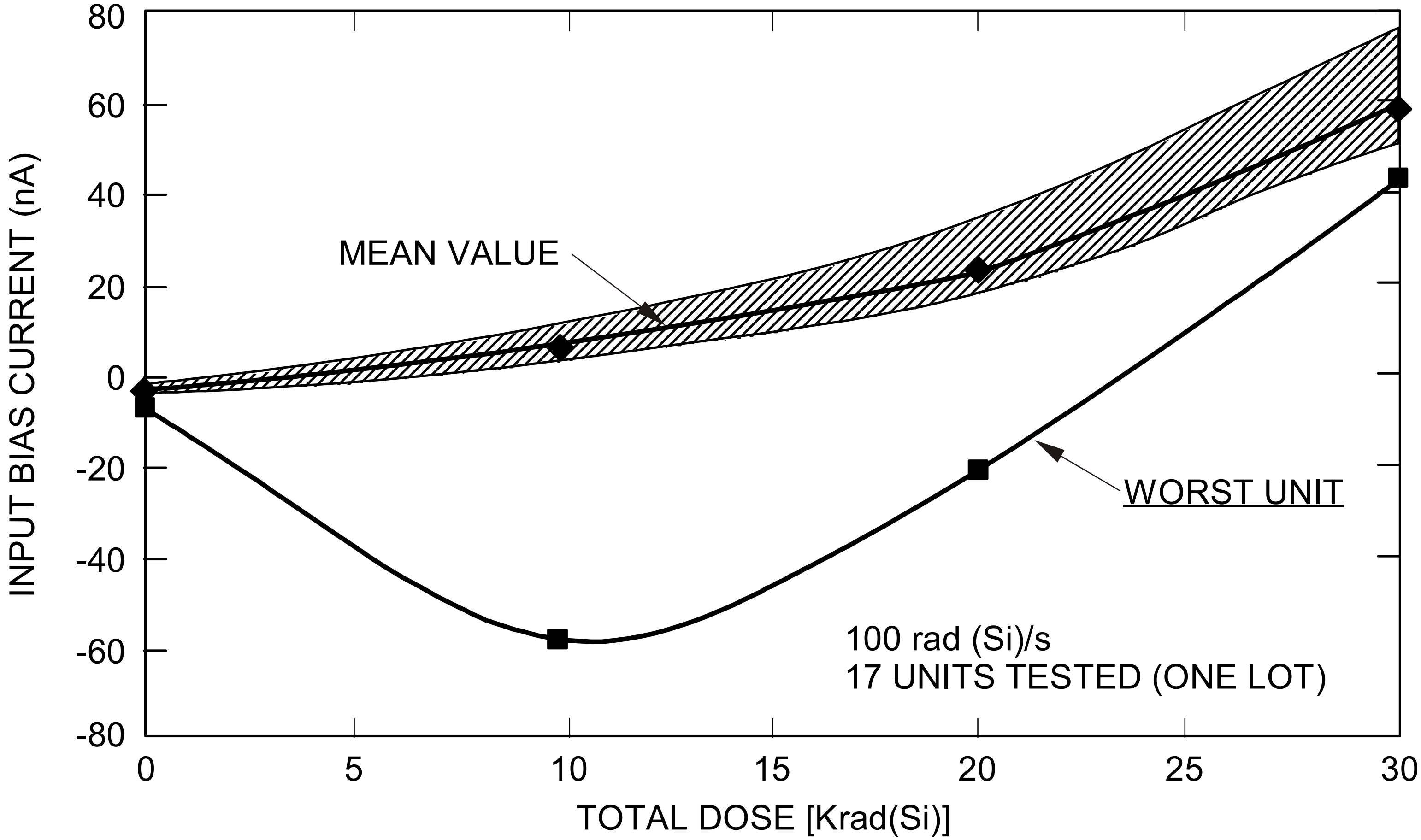
Group 2: Irradiate at ~50 rad(Si)/s & 100°C

Group 3: Irradiate at 0.01-0.1 rad(Si)/s & 25°C

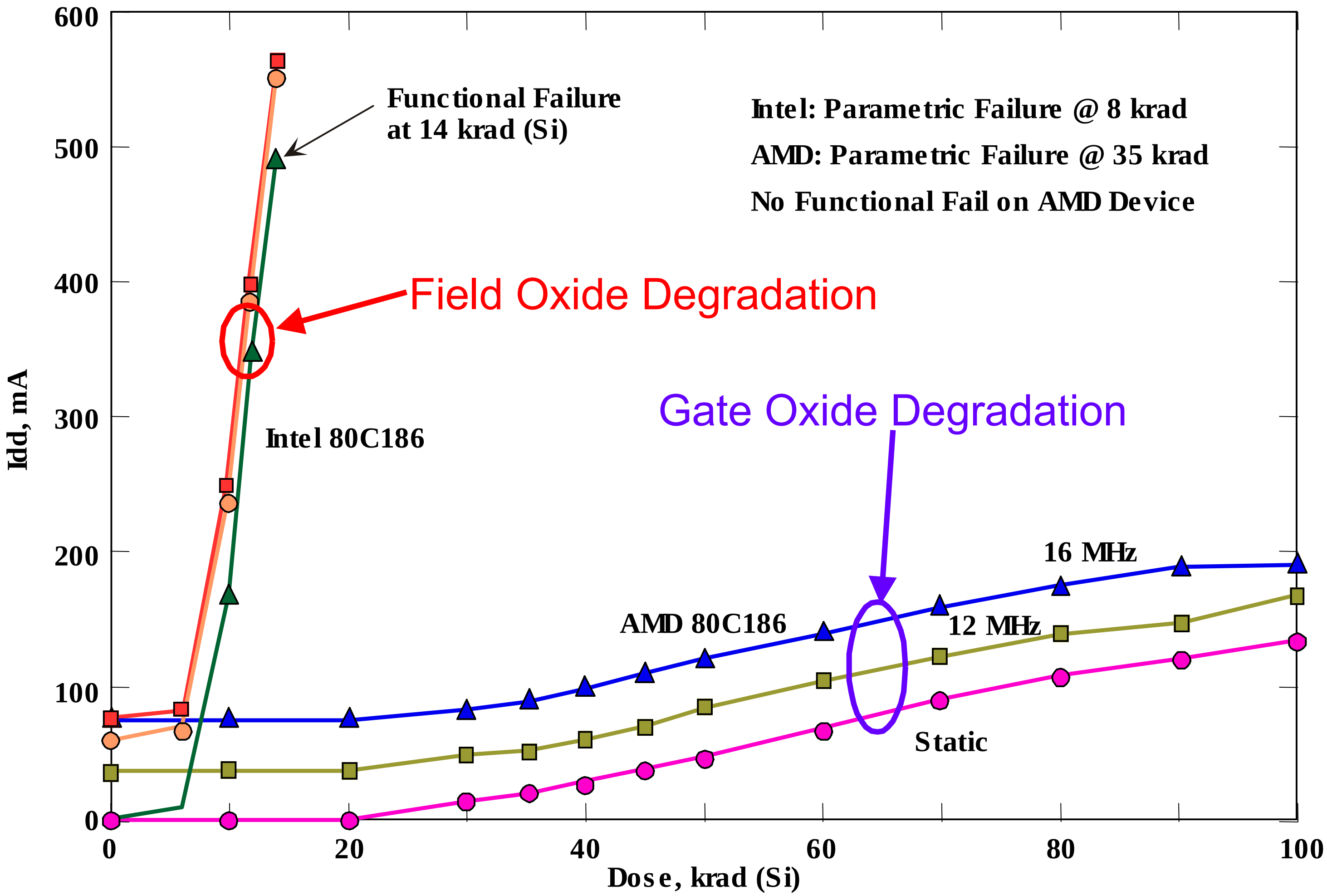
If 2 or 3 worse than 1, then fail part or test further.



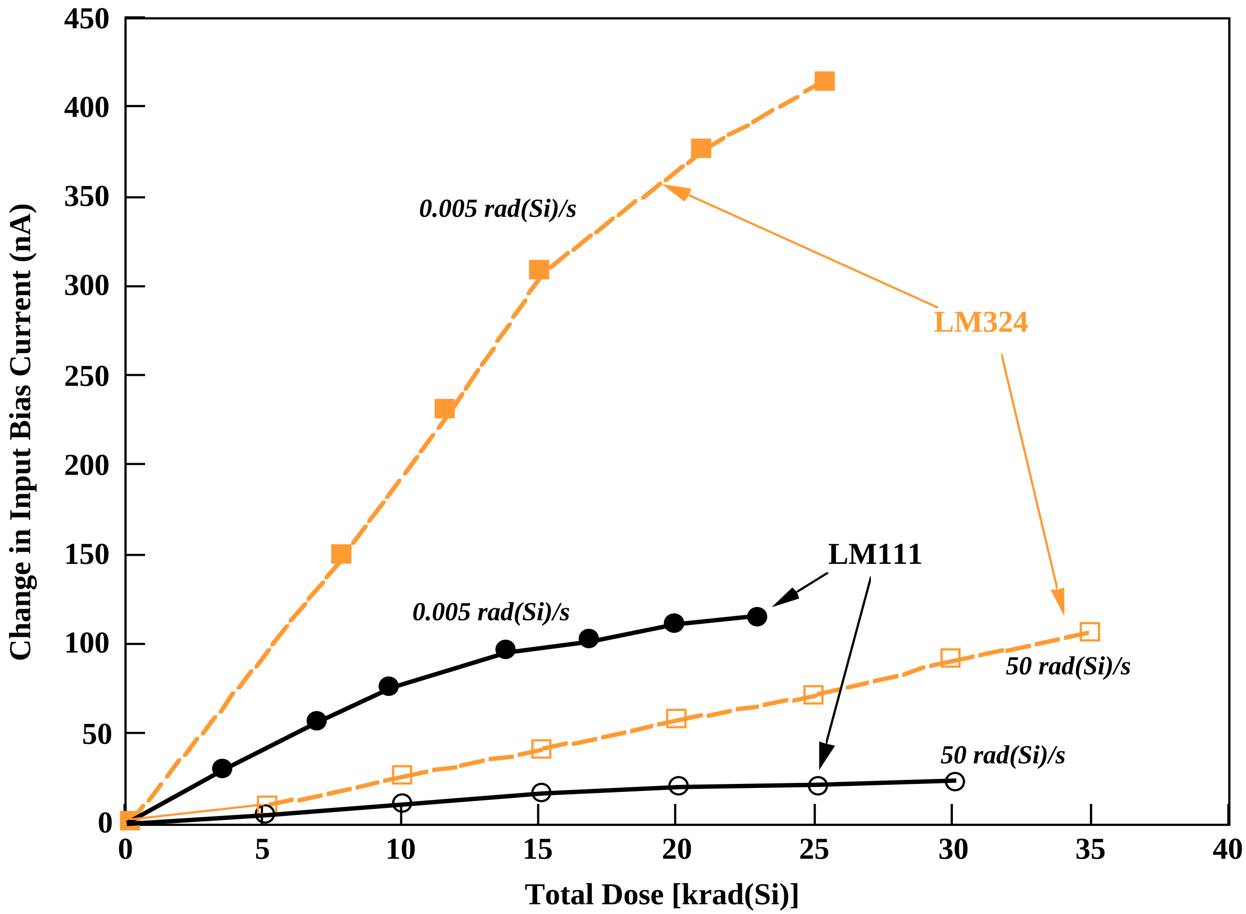
COTS Variability: OP27 Op-Amp



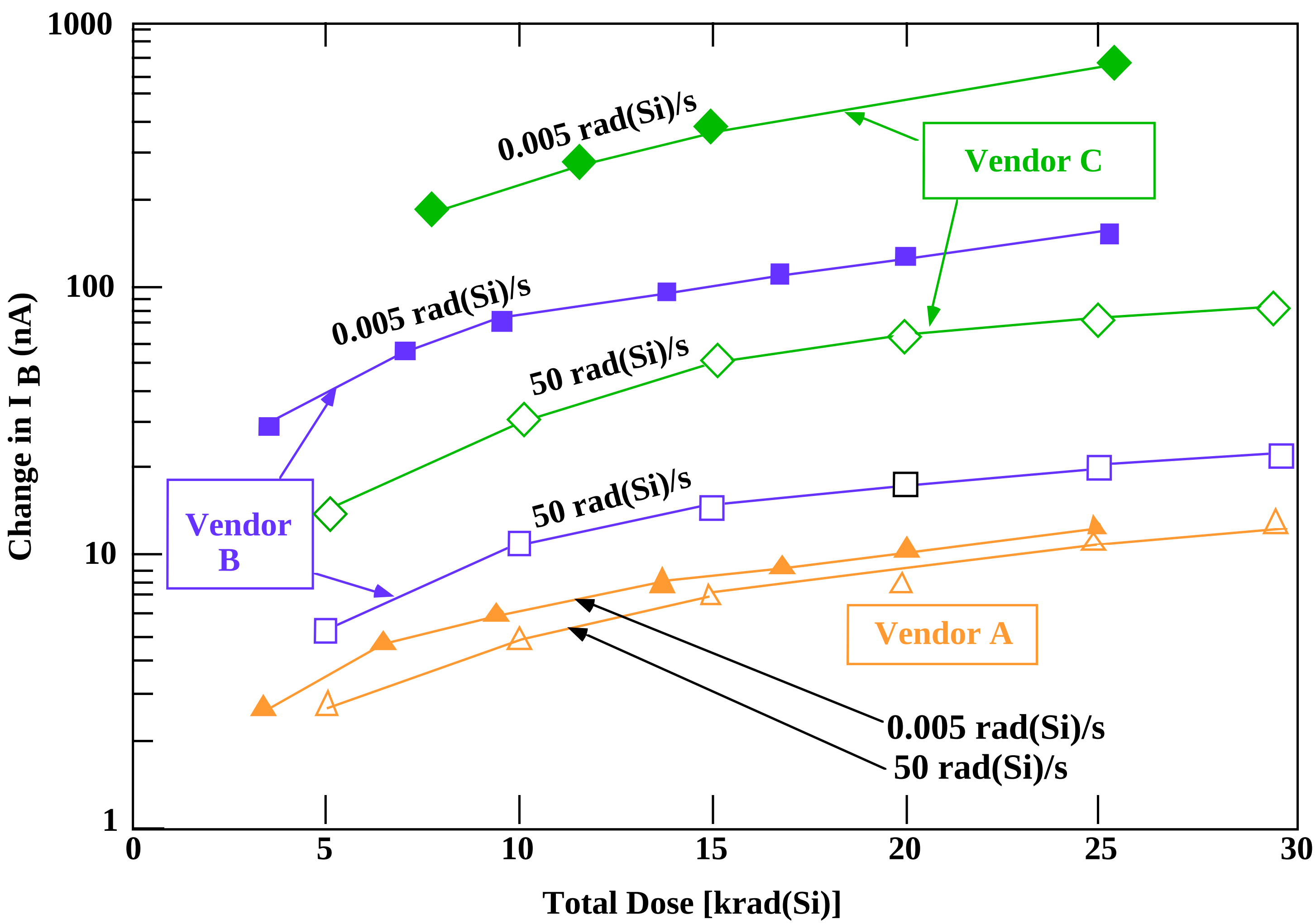
COTS: Same Part, Different Failure Mechanism



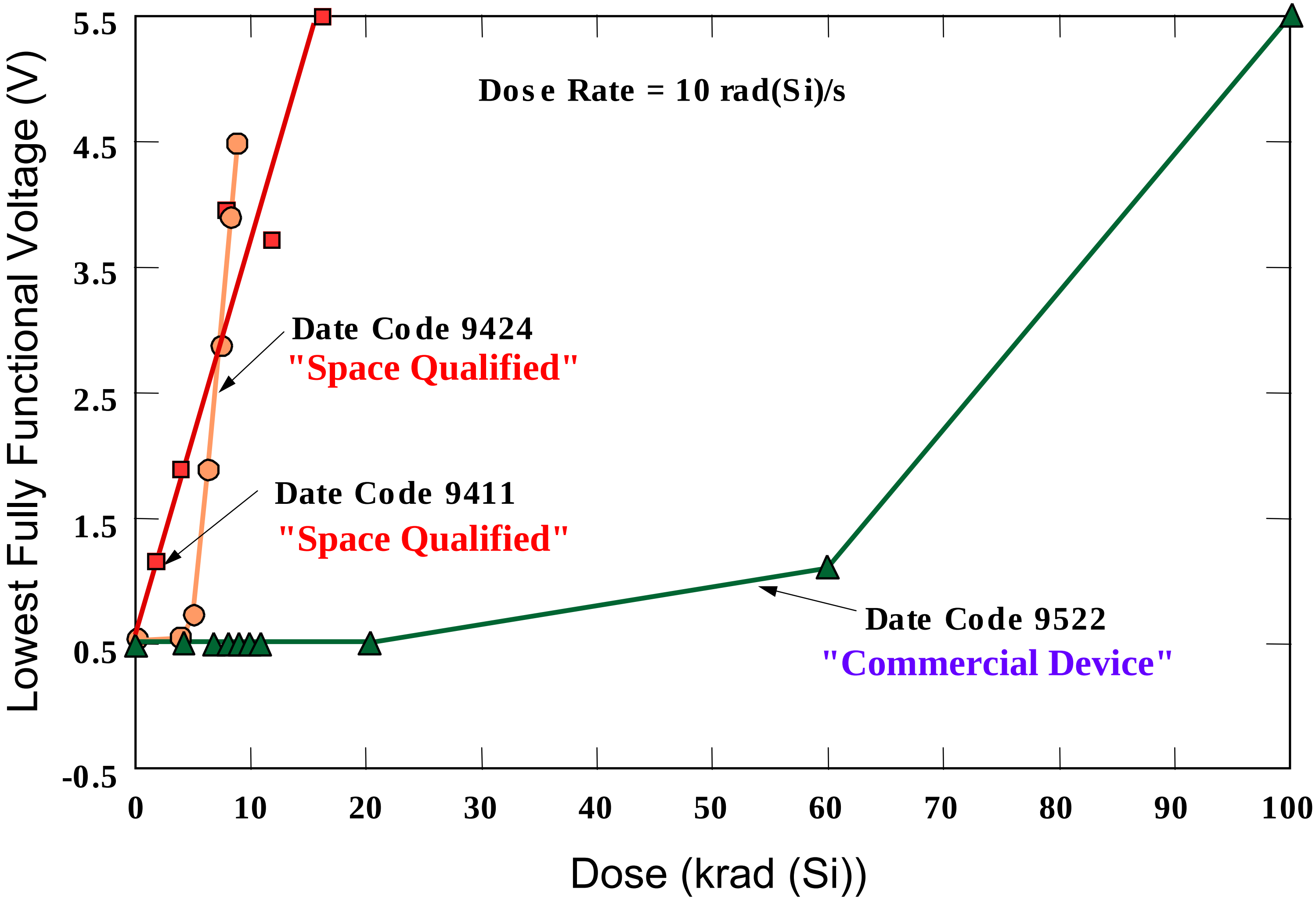
COTS / ELDRS Part Variation: Same Manufacturer



COTS / ELDRs: Manufacturer Variation



Warning: Space Qualified Isn't Always



Warnings / Common Misperceptions

- No bias does not mean that no damage will occur
  - Linear IC's can exhibit more damage when unbiased
  - Discrete transistor damage is about a factor of two lower when unbiased
  - CMOS bias effects are very complex
    - Generally some improvement when parts are unbiased
    - Needs to be checked on part-by-part basis

- Radiation data is not "generic"
  - Do not assume that data from one manufacturer applies to same part type from another manufacturer
  - Radiation response may change as manufacturing process evolves

- Characterization data must encompass use conditions
  - Example: linear IC data with +/- 15V power supplies cannot be used for 5/0 V applications
  - Total dose data bases are of limited value
  - Be aware of ELDRS

Recommendations

1. Get Radiation Testing office involved early

2. Consider using a part where radiation data already exists

3. When radiation testing is done, prepare course of action for parts that fail
   - Shielding
   - Redesign
   - Scheduling delay/cost factors

4. Lot acceptance testing is generally recommended (except for missions with very low levels)

5. Use extreme care when archival data is used

Conclusions

Total dose effects have not been a major factor in older missions

- Thorough radiation testing and parts control
- Conservative design specifications

Total dose effects will be more important for new systems

- Minimal radiation testing and parts control
- Less conservative design specifications
- New effects (particularly ELDRs)
- Subtle failure modes in complex parts

Sensitive Technologies

- Technologies with internal charge pumps (e.g., flash memories)
- High-precision linear integrated circuits
- Field oxide failures in advanced CMOS

Most Total dose problems are avoidable or preventable

- Total dose must be a design criteria

Typical Total Dose Failure Levels of Various Technologies

Technology	Failure Level [Krad(Si)]
Linear IC's	2 - 50
Mixed-signal IC's	2 - 30
Flash Memories	5 - 15
DRAMs	15 - 50
Microprocessors	15 - 70

Further Reading

1. Ma, T.P., and P.V. Dressendorfer, *Ionizing Radiation Effects in MOS Devices and Circuits*, (Wiley and Sons, New York, 1989).
2. P.V. Dressendorfer, “Basic Mechanisms for the New Millenium,” in 1998 *IEEE NSREC Short Course*, (IEEE, Piscataway, NJ, 1998).
3. All IEEE Nuclear and Space Radiation Effects Conference (NSREC) Proceedings (see December issues of IEEE Transactions on Nuclear Science, 1964-present).
4. All IEEE NSREC Radiation Effects Data Workshops (199x-present).
5. All IEEE NSREC Radiation Effects Short Courses (1980-present).
6. J. Bennedetto, “Economy-Class Ion-Defying ICs in Orbit,” IEEE SPECTRUM, March 1998, p. 36-41.
7. T. Oldham, *Ionizing Radiation Effects in MOS Oxides*, (World Scientific, River Edge, NJ, 1999).

Section VI: Displacement Damage and Special Issues for Optoelectronics

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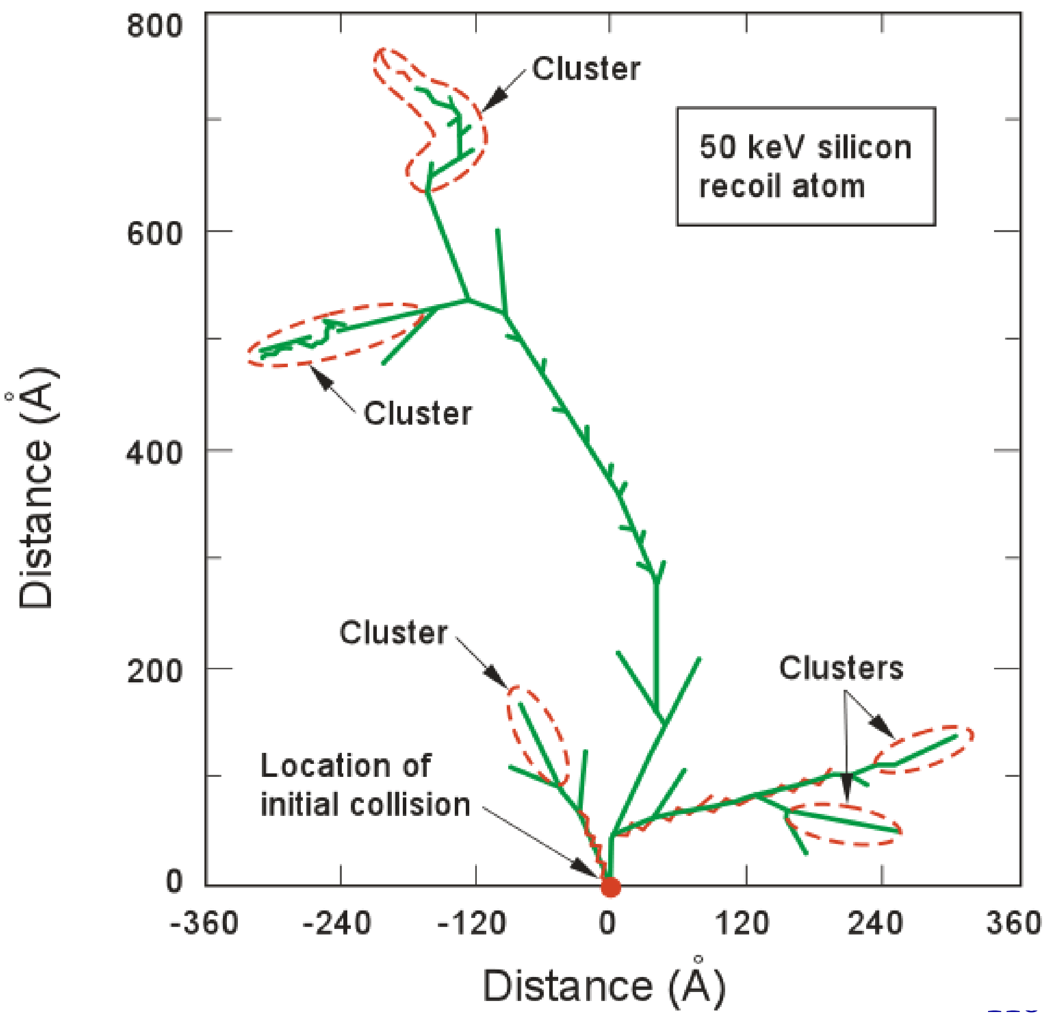
Electronic Parts Engineering Office
Section 514

Displacement Damage for High Energy Transfer

Displacement Cascade

Several damage clusters are produced by the collision

Damage is caused by movement of lattice atom after primary collision



Displacement Damage

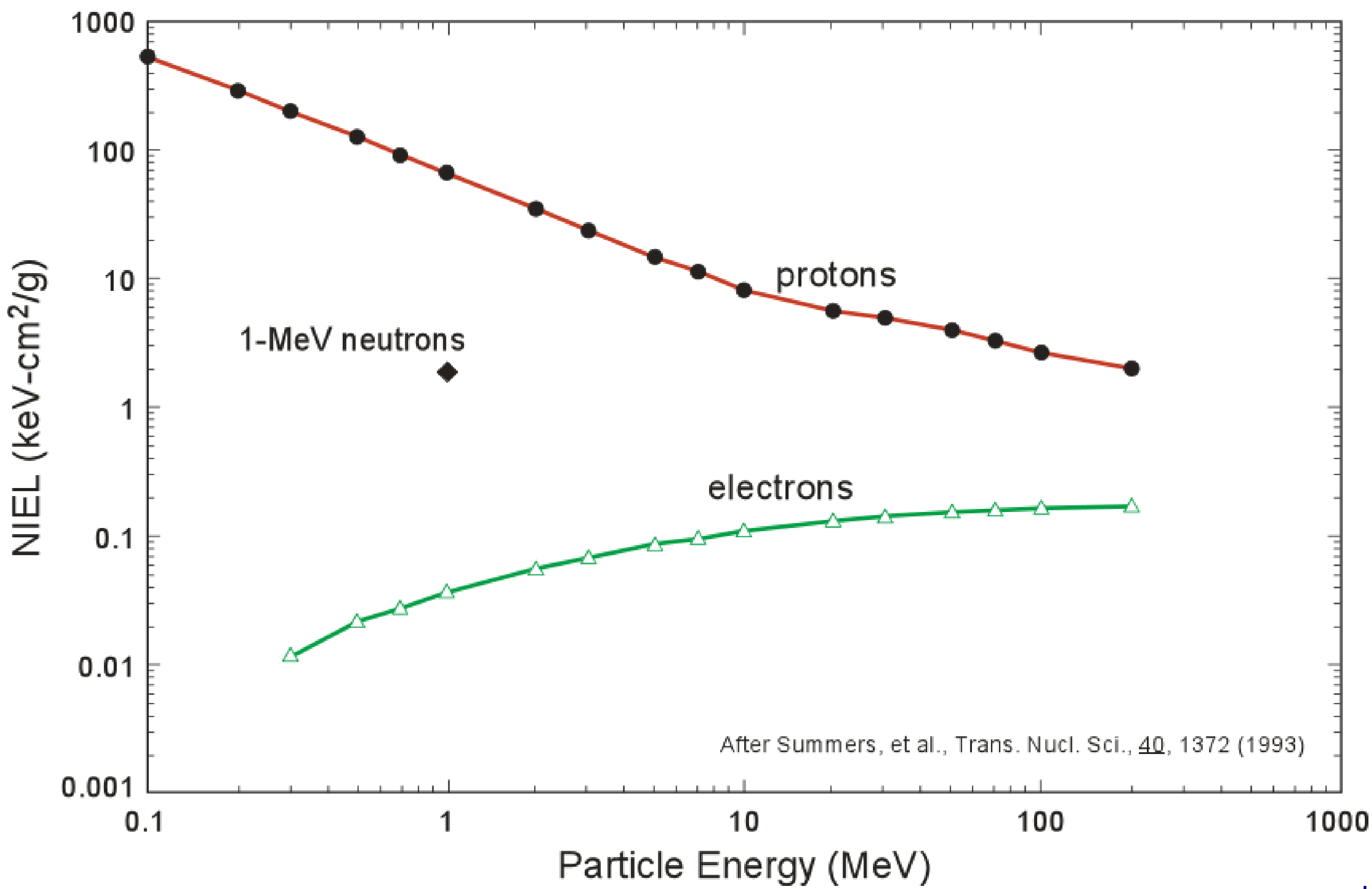
Effects of Displacement Damage in Semiconductors

- Minority carrier lifetime is degraded
  - Reduces gain of bipolar transistors
  - Also affects optical detectors and some types of light-emitting diodes
  - Effects become important for proton fluences above 1×10^{10} p/cm^2
- Mobility and carrier concentration are also affected

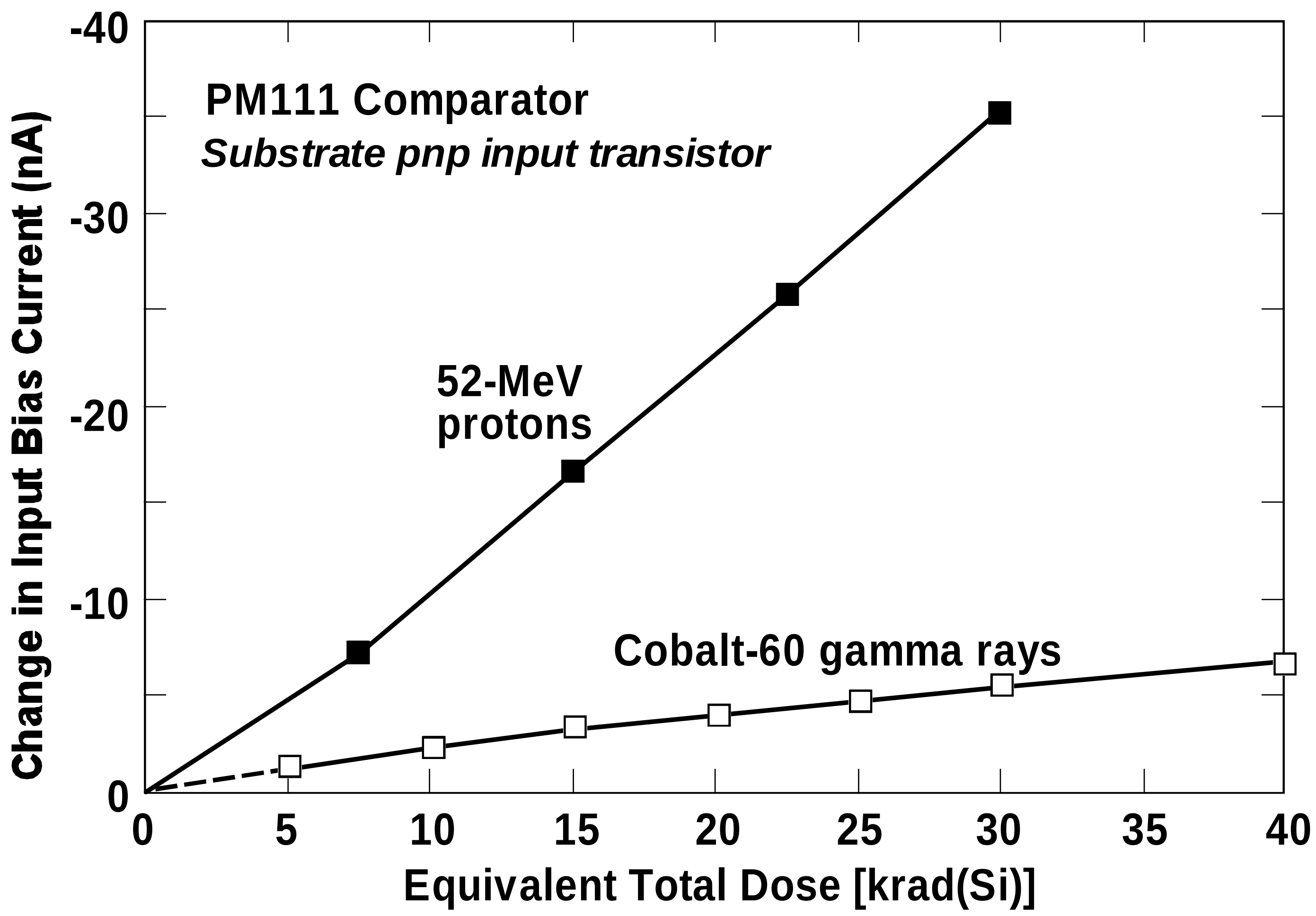
Particles Producing Displacement Damage

- Protons (all energies)
- Electrons with energies above 150 keV
- Neutrons (from on-board power sources)

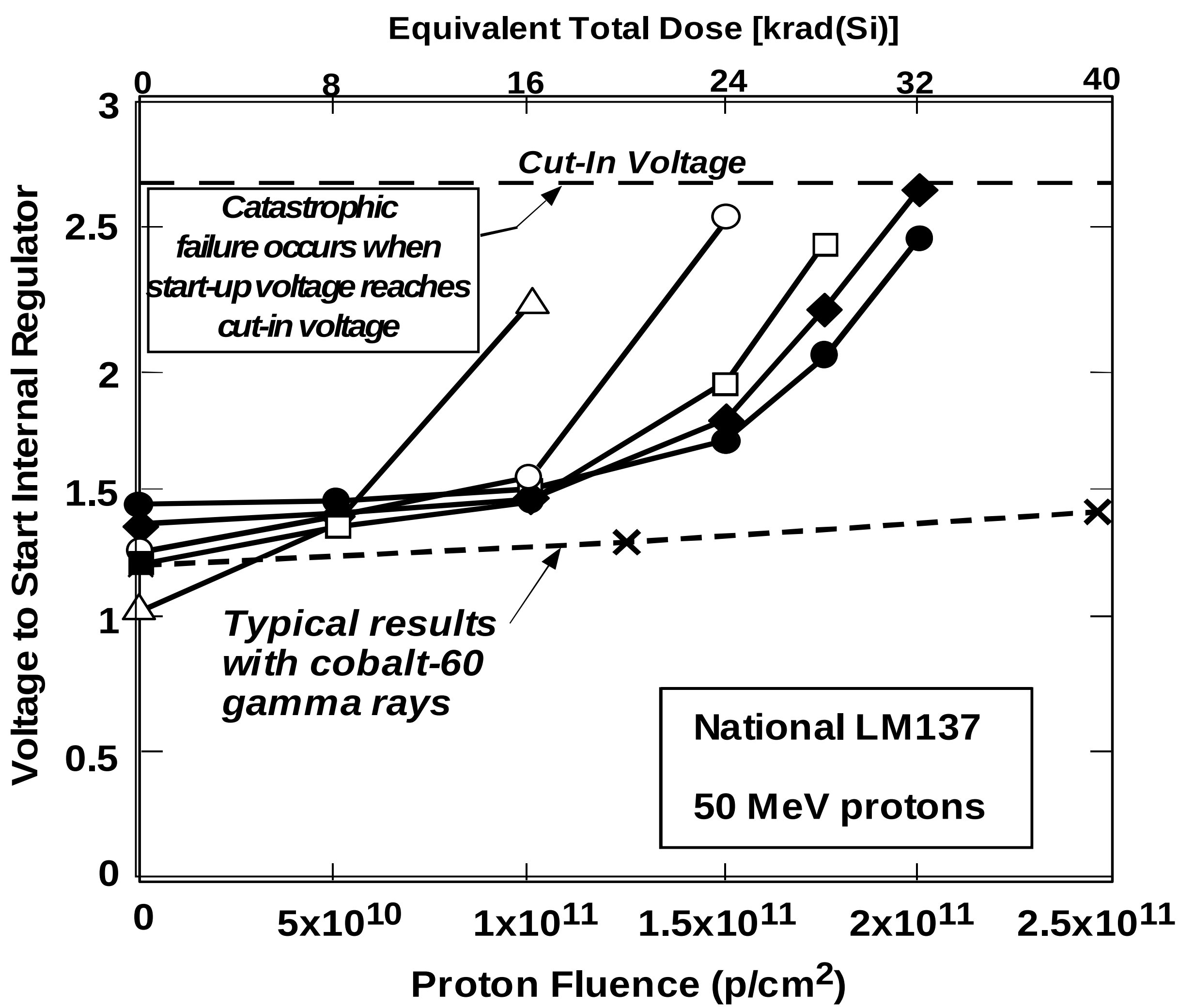
Energy Dependence of Displacement Damage in Silicon



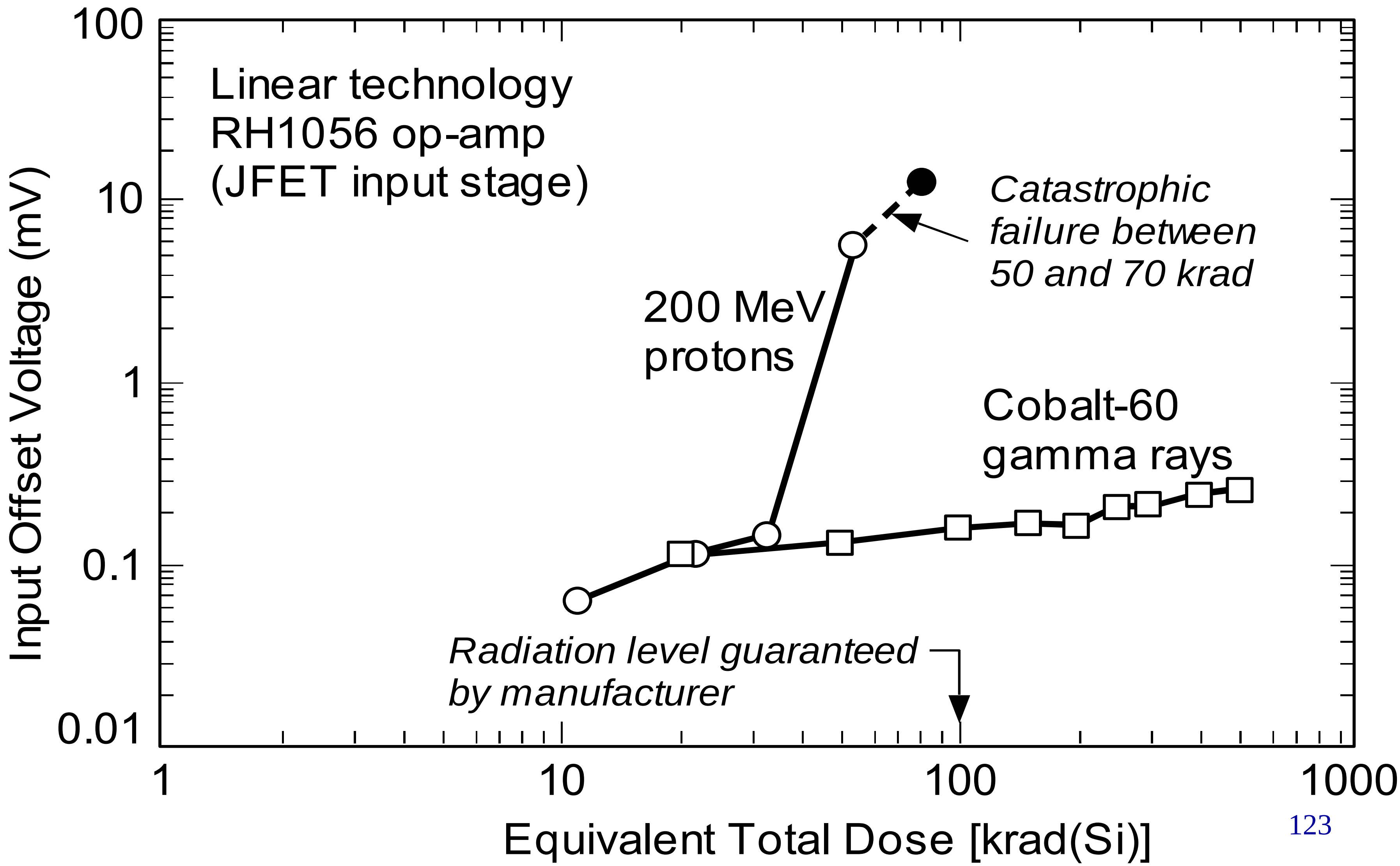
Effects of Gamma and Proton Irradiation on Input Bias Current of a Differential Comparator



Displacement Damage in a Voltage Regulator



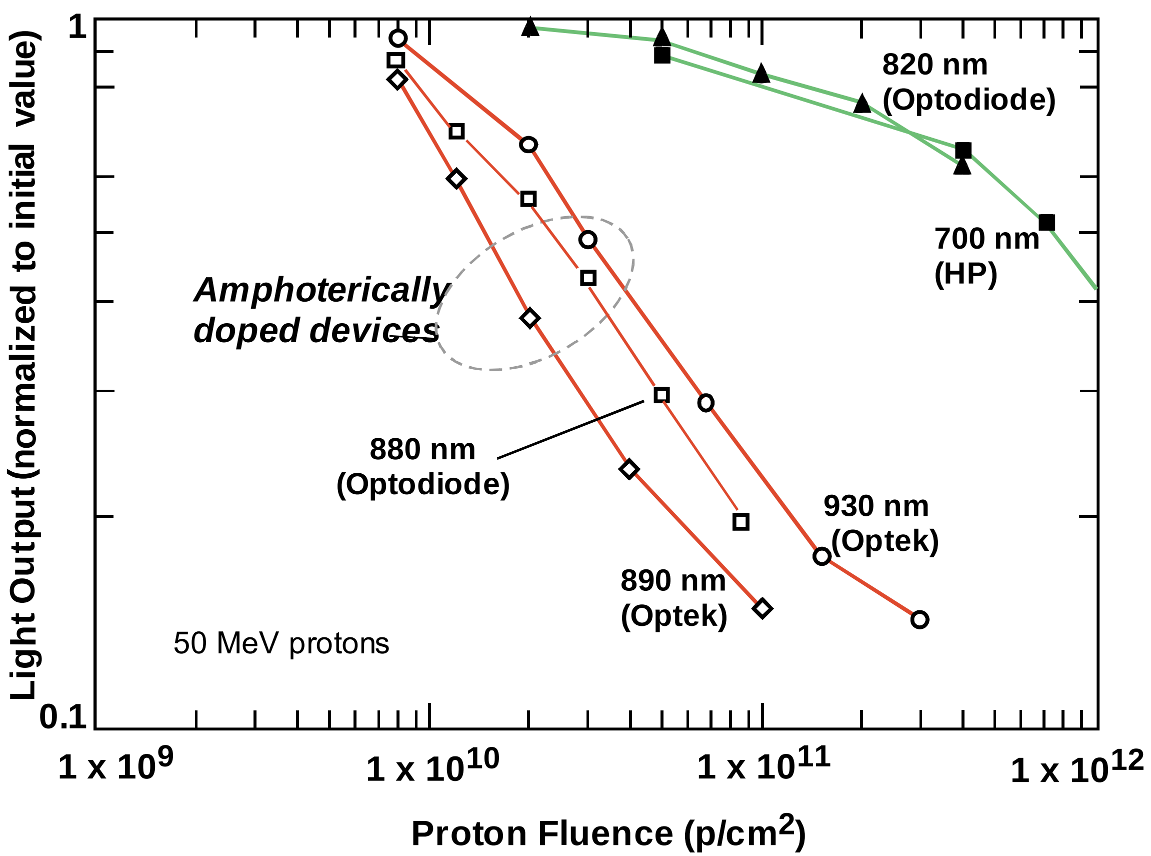
Displacement Damage in a Hardened Op-Amp



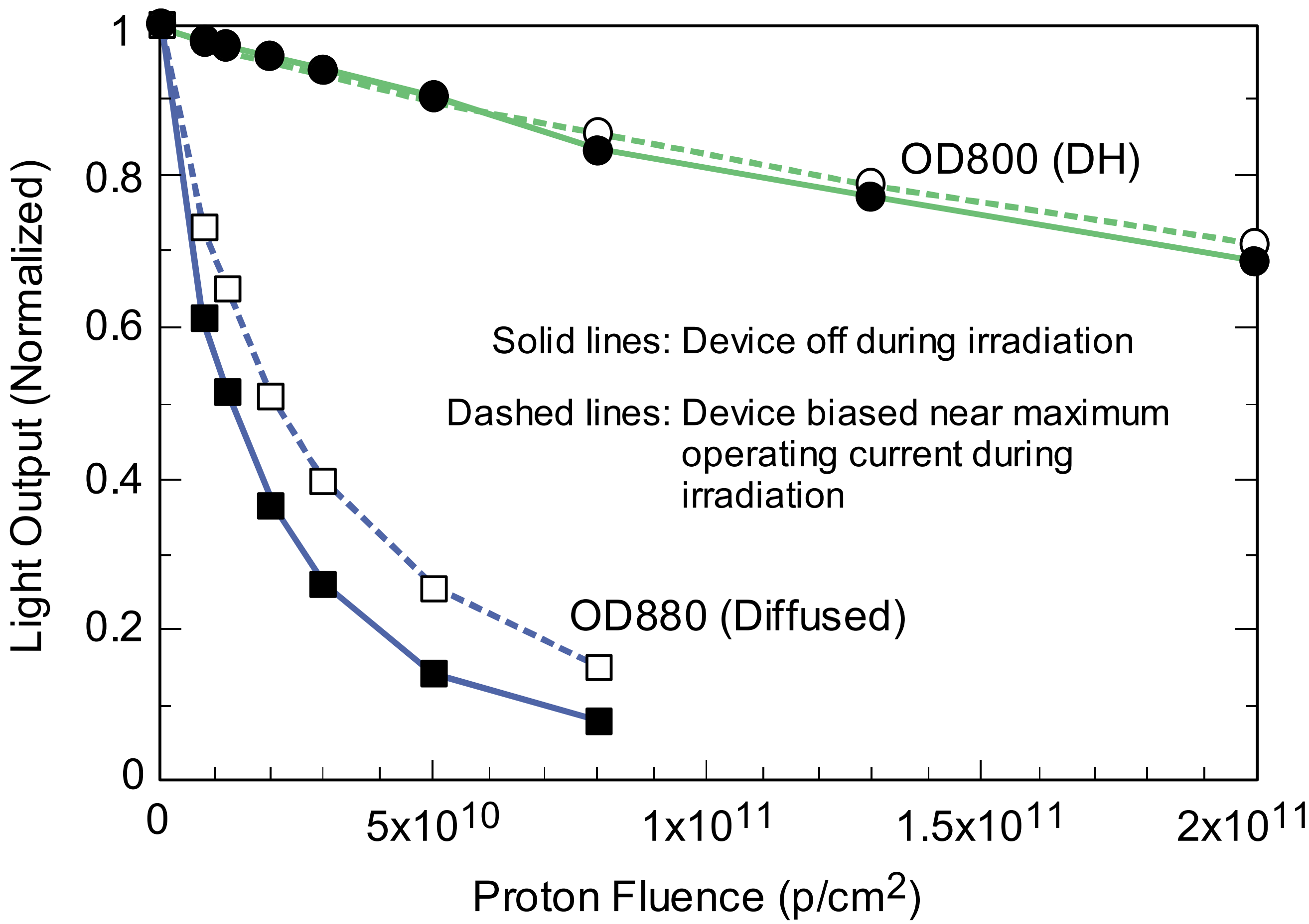
Displacement Damage Comparisons

Particle Type	Total Dose [rad(Si)]	Fluence (#/cm^2)	Equiv. Neutron Fluence (n/cm^2)
electrons (100 MeV)	100k	3.3×10^{12}	3.8×10^{11}
electrons (2 MeV)	100k	4.1×10^{12}	8.6×10^{10}
protons (50 MeV)	100k	6.2×10^{11}	1.4×10^{12}

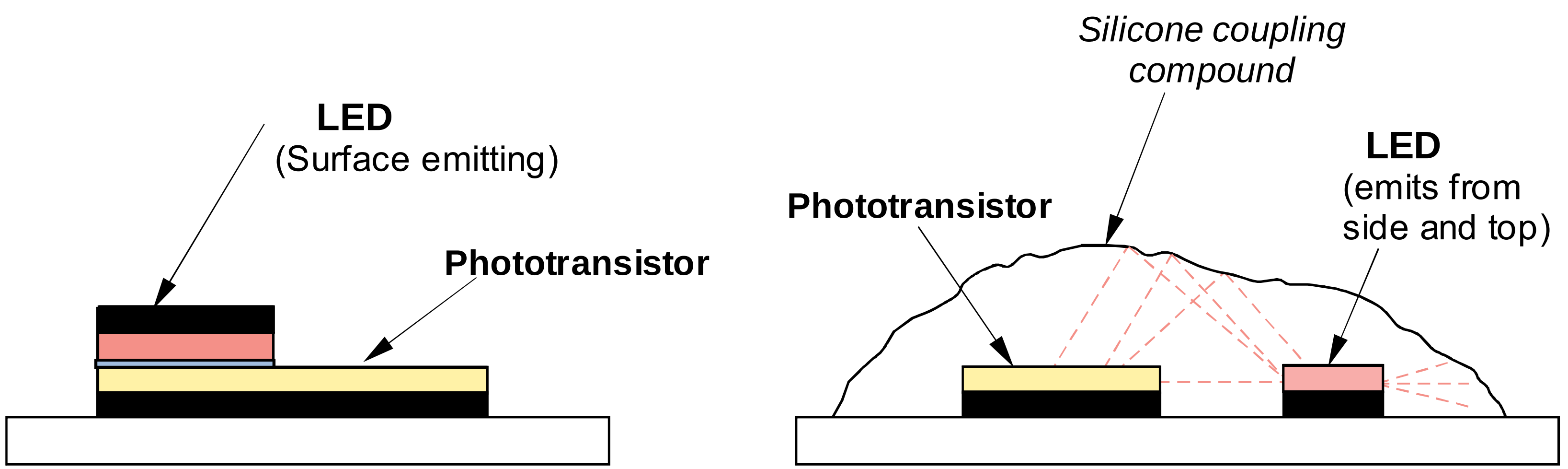
Degradation of Light-Emitting Diodes



Comparison of Two LED Technologies



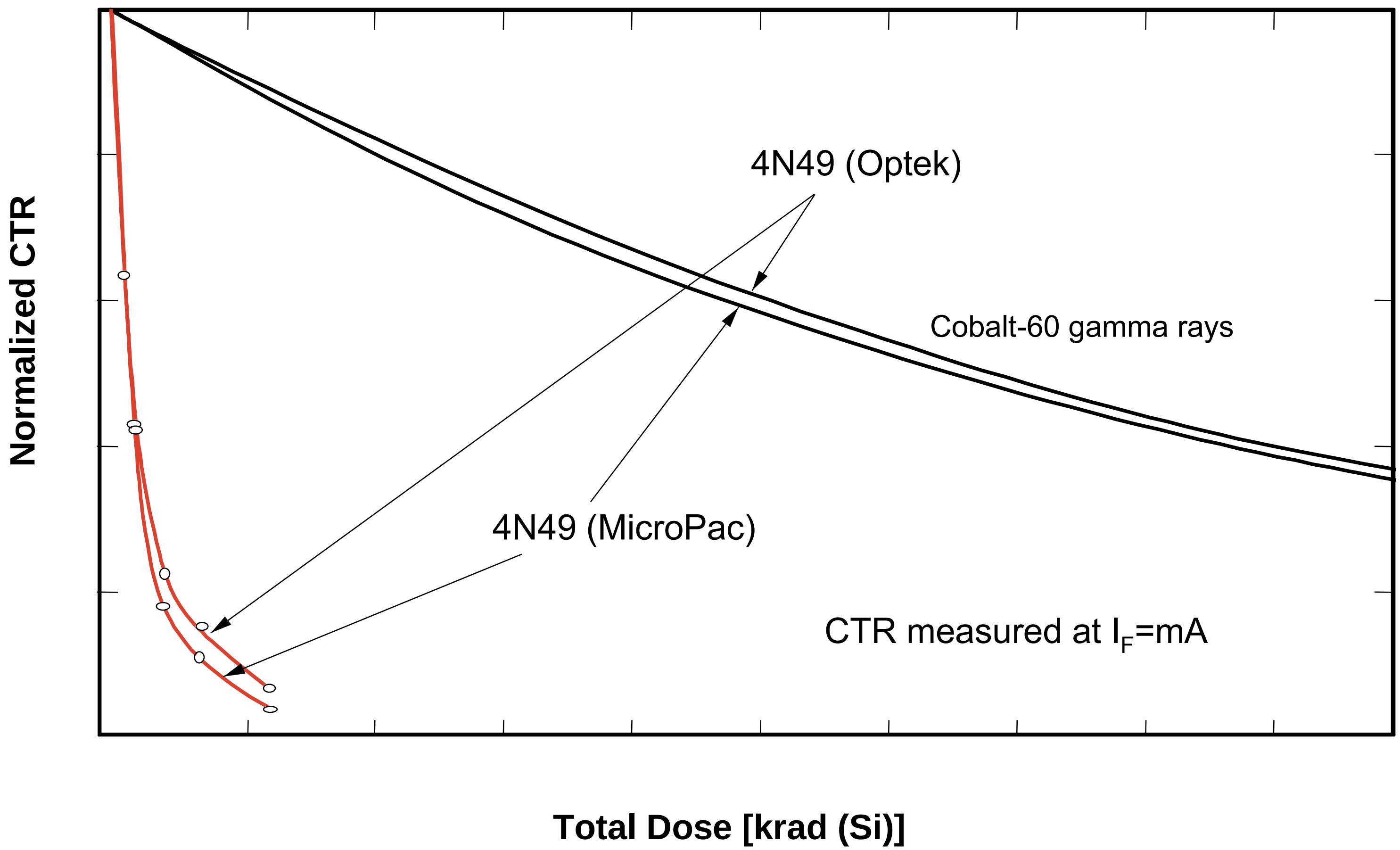
Optocoupler Construction



(a) Sandwich structure
(direct coupling to detector)

(b) Lateral structure
(reduced coupling efficiency)

Optocoupler Degradation



Failure of Optocouplers on Topex-Poseidon

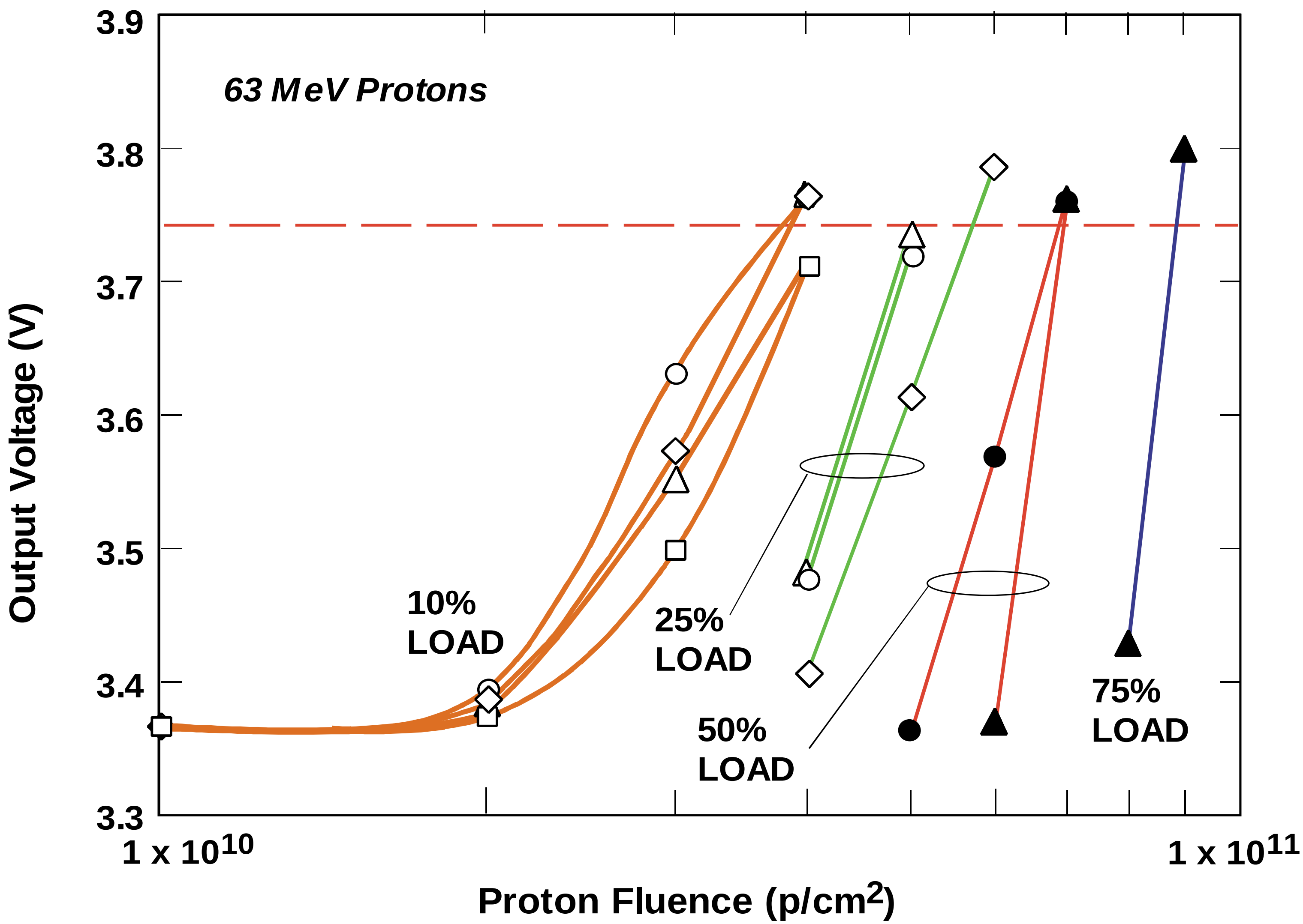
High-Inclination Earth Orbit

- 1300 km, 98 degrees
- Goes through lower edge of proton radiation belts

Optocouplers Used in Five Different Circuit Applications

- Failure occurred in thruster status application after 2.7 years
  - Design did not consider displacement damage
  - Circuit failure corresponds to a factor of four reduction in current-transfer ratio
  - Cold “spares” of little value for displacement damage
- Optocouplers continue to work satisfactorily in thruster firing circuit
  - Consequence of higher circuit margin used by designers

Failure of Power Converters Due to Optocoupler Degradation



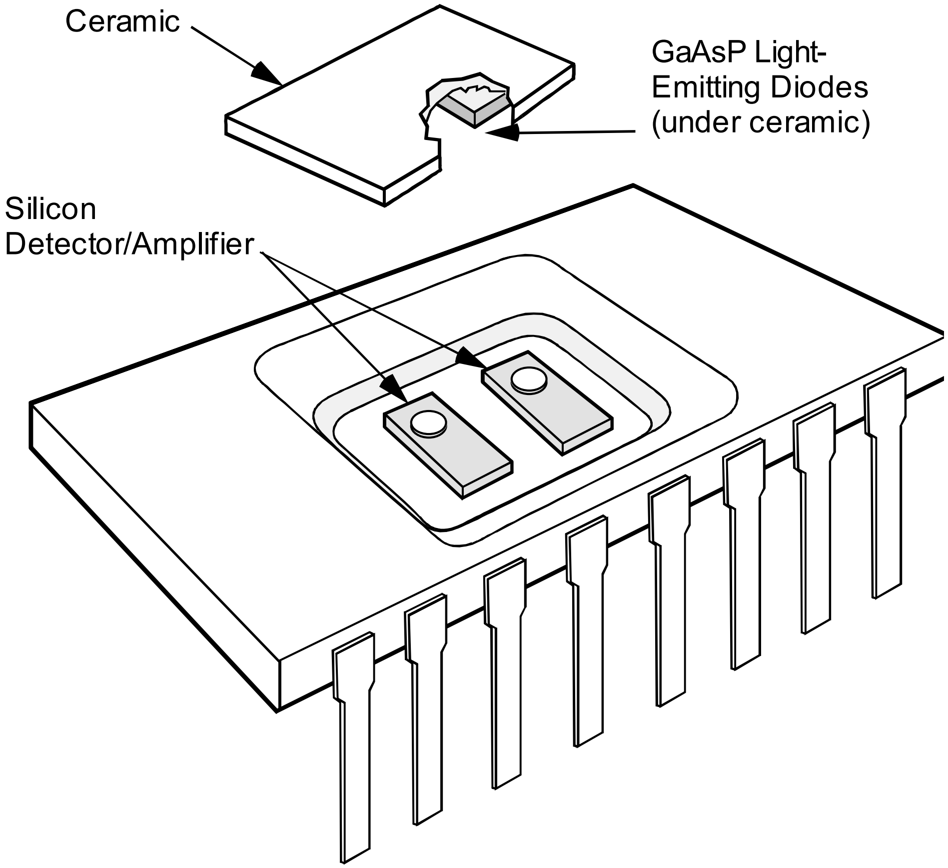
Optocoupler Transients

Voltage System Shutdown Occurred on Hubble Space Telescope

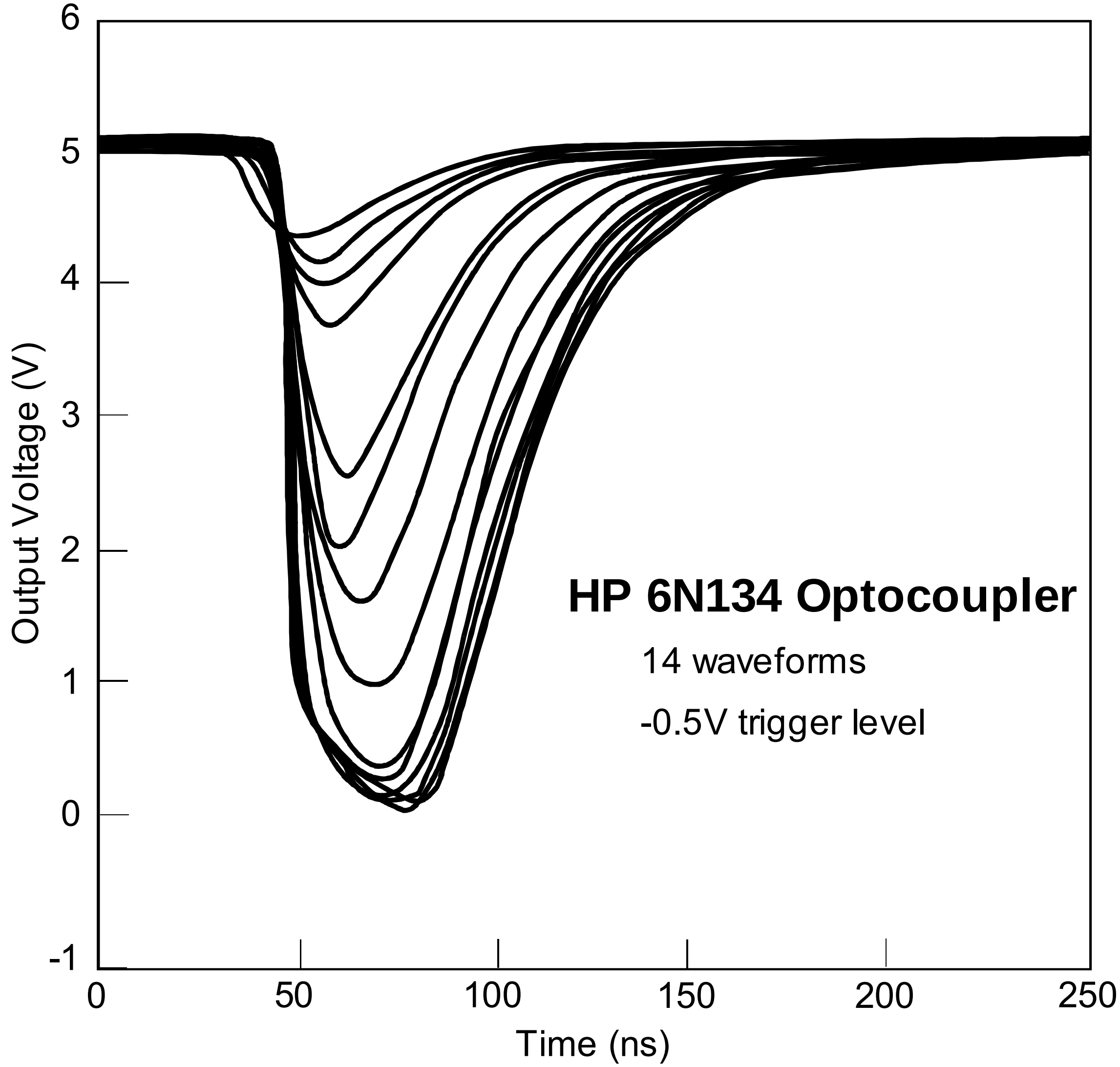
- Observed after upgraded electronics were installed
- Strongly correlated with orbit pattern

Laboratory Tests Showed that Shutdown Was Caused by Transients from Protons

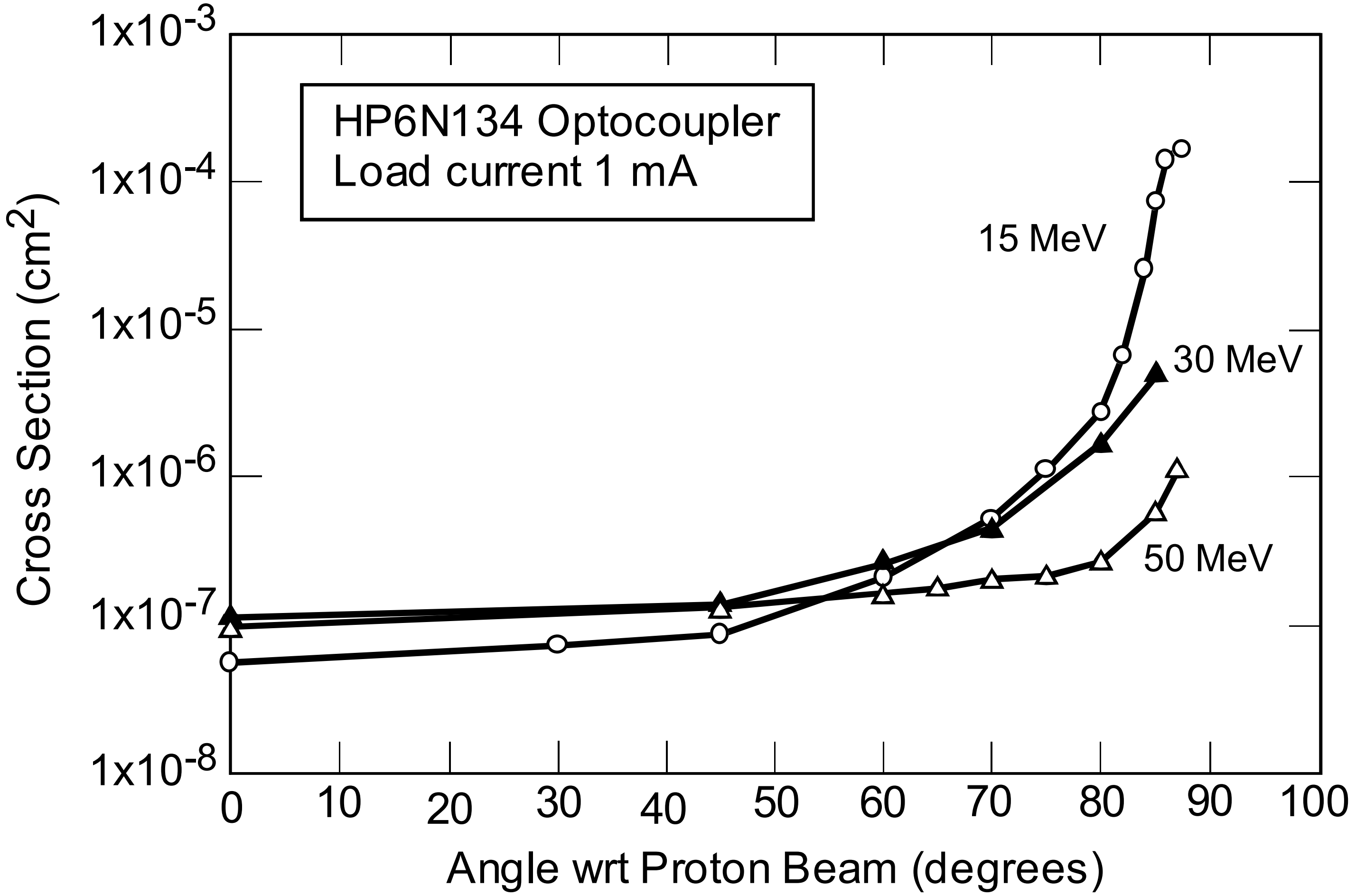
- Dominated by charge in photodetector
- Heavy ions also produce transients



Example of Transients from Protons for 6N134 Optocoupler



Angular Dependence of Proton Upset Cross Section



Course Summary

Environments and System Requirements

JPL Systems Have a Variety of Mission Requirements

- Short duration missions with low radiation levels
- Interplanetary missions with extremely high levels
- Earth-orbiting missions where proton effects dominate

Overall Mission Requirements Must Be Understood

- "Reflexive" policies and procedures should be avoided
- Testing is not always required

Using Parts Where Radiation Data Exists Can Be Cost Effective

Single-Event Upset

SEE Effects Have Become Worse As Parts Have Evolved

- Device scaling
- Complex internal design and architecture
- Functional interrupt problems

SEE Testing Has Become More Complex

- Device complexity
- New phenomena
- Multiple-bit upset

Successful Use of Commercial Parts Depends on System Design

Permanent Damage from Single-Particles

Latchup Is the Most Critical Catastrophic Damage Issue

- Many CMOS circuits are sensitive to latchup
- Difficult and costly to characterize latchup in detail
- Best alternative is to eliminate latchup-prone devices

Gate Rupture and Burnout Effects Are Becoming More Important

- Previously only an issue for power MOSFETs
- Permanent damage has been observed in pulse-width modulators
- Testing and qualification methods need to consider these effects

Total Dose Effects

Total Dose Damage Remains a Key Issue for Many Technologies

- **Field oxide failure causes huge increases and functional failure in CMOS**
- **Gate oxide threshold shift is important in many technologies**
- **Internal charge pumps are usually highly susceptible to total dose damage**

Low Dose Rate Damage Effects Are a Major Issue for Bipolar Devices

- **Problem not completely understood**
- **Wide variation among manufacturers**
- **JPL has an excellent facility for tests at very low dose rate**

Devices with High Maximum Voltage Ratings Are Often a Problem

- **Low doping levels**
- **Increased oxide thickness**

Permanent Damage from Protons and Electrons

Permanent Damage Issues Are Often Overlooked

Technologies Where Displacement Effects Matter

- Linear integrated circuits
- Light emitting diodes
- Optical detectors
- Optocouplers

Cobalt-60 Gamma Rays Are a Compromise

- Cost effective
- Appropriate for technologies where displacement damage doesn’t matter
- Provides no information about displacement damage effects