Chapter 5. Device Modeling

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It is extremely important to complete MMIC device modeling and simulation prior to the fabrication because the technology and design iteration are expensive and the technology often does not allow postfabrication tuning. Therefore, model accuracy is an essential part of first-pass design success. Device modeling is useful not only in design, but also in production control and yield analysis.

This chapter will describe the general subjects related to MMIC device modeling, including the types of models, equivalent circuits, modeling approach, and commercially available modeling software. The issue of model sensitivity will also be discussed. Although the content emphasizes MESFETs, the methodology used can be applied to other MMIC devices, such as HEMTs, HBTs, and diodes.

I. Types of Models

A device model can be composed of a set of equivalent circuit elements in a particular circuit topology or a set of equations that, when evaluated, predict device performance. A modeling process generally includes three steps: characterization, parameter extraction and modeling. The flow chart of a typical modeling process is illustrated in Figure 5-1. Three processes are closely related in a number of important

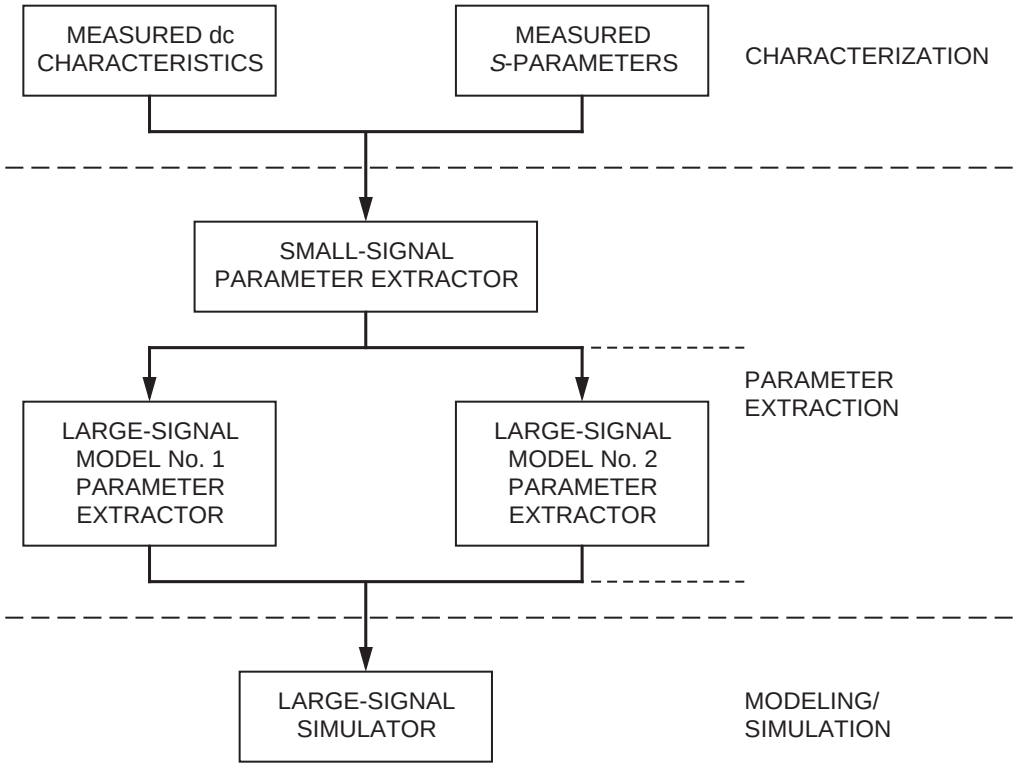

Figure 5-1. Flow chart of the relationship between characterization, parameter extraction, and modeling.

ways. The accuracy of any device model ultimately is limited by how accurately the model parameters are determined. Parameter extraction is dependent on the type and accuracy of available device characterization data. The merits of the device model are partially determined by the amount and type of characterization required. Generally speaking, MMIC device modeling can be classified into three categories: Empirical Device Models (EDMs), Physically Based Models (PBMs), and data-based models.

EDMs use equivalent circuits to simulate the external behavior of devices. Such a model consists of a number of linear and nonlinear elements connected in a predefined topology. Various EDMs, including small signal and large signal, have been widely used in MMIC computer-aided engineering. The advantages of EDMs are simple characterization, implementation, and circuit simulation.

To obtain their performance predictions, PBMs rely on physical parameters that describe the device geometry, materials, and processing parameters. Such parameters typically include gate length, gate width, channel thickness, and doping density. PBMs have an advantage over EDMs: PBMs allow studies of the effects of process variation on the device performance; such effects are critical for process control and yield prediction. However, it is difficult, in some cases even impossible, to obtain the precise physical parameters required to describe the device.

Recently, data-based models (also known as measurement-based) have become popular with device designers. Data-based models are generated directly from measured data without prior knowledge of process parameters. A data-based model can predict behavior exhibited in a new process that may be difficult to represent by empirical functions. However, its lack of physical insight into the actual studied device is a drawback.

II. Equivalent Circuit

The equivalent circuit of an MMIC device is an abstraction and simplification that yields a representation of the device. It must represent adequately all the important physical characteristics of the device. Exploiting the relationship between the equivalent-circuit elements and device physics will be helpful to device modeling.

A. MESFET Equivalent Circuit

The device physics of MESFETs and HEMTs have been discussed in Sections 3-III and 3-IV, respectively. The material and structure features that determine the microwave behavior of a FET are identified on Figure 5-2; some of relevant parameters are [1]

N = doping density in the n - channel layer

W = thickness of the n - channel layer under the gate

Z_G = gate width

L_G = metallurgical gate length

L_{SG} = source – gate separation

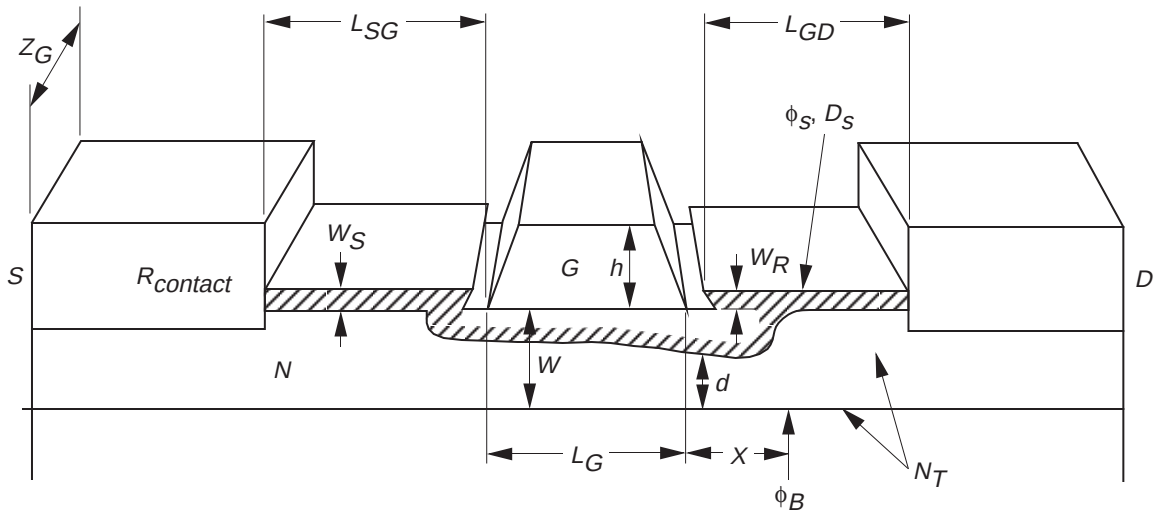

Figure 5-2. Schematic of a MESFET's material and structure.

L_{GD} = drain – gate separation
W_R = depth of gate recess
W_S = surface depletion depth
d = depletion depth
h = gate height
X = extension of the space - charge layer into the gate – drain space

The small-signal equivalent circuit for such a MESFET is presented in Figure 5-3.

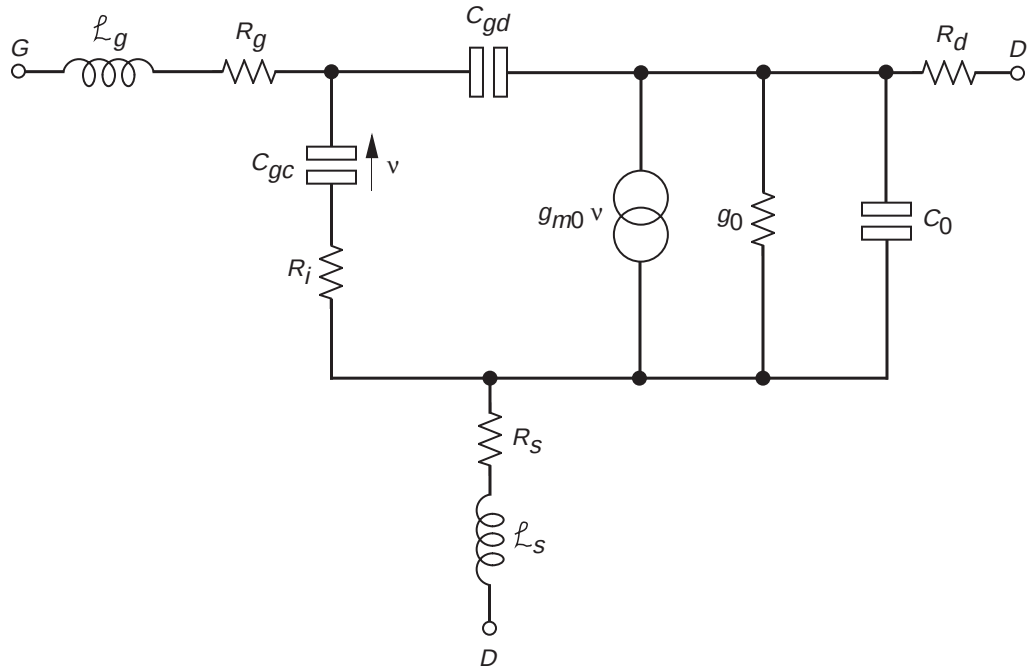

Figure 5-3. Basic GaAs MESFET's equivalent circuit.

In the following, the relationship between some of the equivalent-circuit elements and devices physics will be briefly explained:

(1) Channel resistance, R_i , is the resistance distributed along the channel under the gate, which is the ratio of the potential drop, $E_S L_G$, and the channel current, I_{CH}. The electric field and channel current under the gate are

$$E_S = \frac{v_{sat}}{\mu_0'}; \quad I_{CH} = qNv_{sat}(W-d)Z_G$$

where v_{sat} is the saturated value of electron drift velocity, μ_0' is low-field drift mobility, and q is electron charge. Therefore the channel resistance is

$$R_i \approx \frac{L_G}{\mu_0' qN(W-d)Z_G}$$

(2) Transconductance, g_{m0}, is the ratio of change of drain current and gate voltage. As a first order approximation, it is reasonable to use the channel current to replace the drain current while omitting the substrate current. Using the expressions for I_{CH} and

$$V_{S'G} + V_{BO} \approx \frac{qNd^2}{2\varepsilon}$$

where $V_{S'G}$ is the dc voltage between the gate and virtual source—taking an account of R_S, V_{BO} is the equilibrium contact potential between gate metal and the N-GaAs layer, and ε is permittivity. The transconductance is

$$g_{m0} \equiv \frac{\partial I_D}{\partial V_{S'G}} \approx \frac{\partial I_{CH}}{\partial V_{S'G}} = \frac{\varepsilon v_{sat} Z_G}{d}$$

(3) Gate-channel space capacitance, C_{gc}, is the capacitance of the gate. As a first order approximation, it can be treated as a parallel plate stripline with dimensions of gate length, L_G, and the gate width, Z_G. That capacitance is

$$C_{gc}' = \frac{\varepsilon L_G Z_G}{d}$$

where C_{gc}' is an approximation. Taking account of the capacitance in the velocity-saturated region located near the tail of the gate, the gate-channel capacitance is

$$C_{gc} = \frac{\varepsilon L_G Z_G}{d}\left(1 + \frac{X}{2L_G} - \frac{2d}{L_G + 2X}\right)$$

(4) Gate-drain space capacitance, C_{gd}, is associated with the electron inflow at the right edge of the space-charge layer. The depletion extension X increases slightly as drain–source voltage increases, resulting in charge storage. Assuming W_R equals to W_S, the capacitance is

$$C_{gd} = \frac{2\varepsilon L_G Z_G}{L_G + 2X}$$

(5) Gate series inductance, L_g,, is the inductance determined by the strip's dimension of the gate length, L_G, and the gate width, Z_G. The value of L_g can be assessed by regarding the gate as a section of a parallel plate stripline:

$$L_g = \frac{\mu_0 d Z_G}{L_G}$$

where μ_0 is the permeability of free space.

(6) Gate resistance, R_g, is bulk resistance determined by the strip's dimension in the direction of current flow, which is the cross-sectional area, $L_G \times h$, and the gate width, Z_G. Since h is normally smaller than the skin depth, the whole height of the gate contributes to its conductance. Taking into account the voltage drop across the strip width due to distributed capacitance, the RF resistance, R_g, of the strip is only one third of the dc resistance:

$$R_g = \frac{\rho Z_G}{3hL_G}$$

where ρ is metal resistivity.

(7) Drain resistance, R_d, is the ratio of the voltage change across the length of the bulk region ($L_{GD} - X$) and the channel current, I_{CH}. The channel current in this region becomes $I_{CH} = qNv_{sat}WZ_G$. Thus the drain resistance can be obtained in a way similar to that for R_i:

$$R_d \approx \frac{L_G - X}{\mu_0' qNWZ_G}$$

B. HEMT Equivalent Circuit

The equivalent circuit for HEMT is the same as that for MESFET except for the gate-leaking current in some HEMTs, which may require resistances in parallel with C_{gc} and C_{gd}, respectively. Applying structure and operation conditions, the analytic expressions for some equivalent-circuit elements of HEMTs, such as g_{m0}, C_{gc}, and C_{gd}, can be derived [1].

III. Characterization and Parameter Extraction

The various types of data that might be required for use in the device modeling process include dc I–V characteristics, microwave *S*-parameters, large-signal *S*-parameters or load-pull characteristics, noise parameters, and physical characteristics of the device. The parameter extraction obtains appropriate equivalent-circuit element values from measured data using optimizers to minimize the error between simulated and measured data [2].

A. DC Characterization and Parameter Extraction

The primary advantage of dc data for model parameter extraction is ease of performance. A typical dc-modeling process for MESFET devices is shown in Figure 5-4. Although dc data fail to describe the RF characteristics of the device—such as strong frequency-dependent output conductance, g_0—they are quite useful as first-order estimates of device performance characteristics.

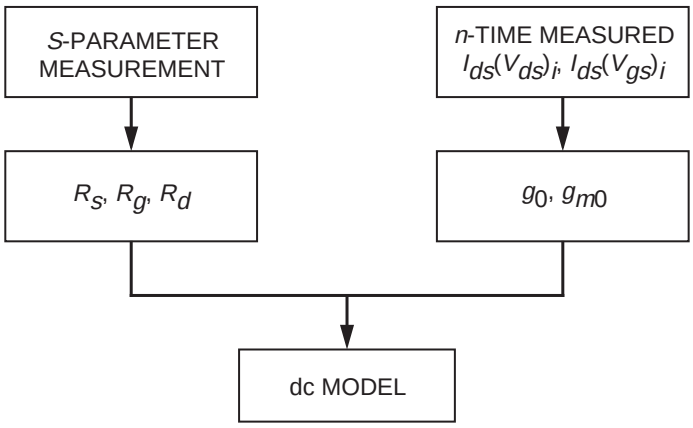

Figure 5-4. Flow chart of dc modeling.

B. RF Characterization and Parameter Extraction

RF or small-signal characterization of devices commonly uses microwave *S*-parameter measurement. Typically, *S*-parameters taken at 5 to 20 frequencies between dc and the upper frequency of interest are sufficient to determine element values. Automated measurement equipment that performs these measurements is readily available. The flow chart for RF characterization and parameter extraction is presented in Figure 5-5. With selected equivalent-circuit topology, the initial value of the circuit elements, which is estimated using a combination of the dc-parameter extraction technique and RF measurement, can be determined. An optimization routine is then run to refine the estimates of the element values until an appropriate agreement between the measured and modeled values is reached. However, the model is valid only under linear operating conditions.

C. Large-Signal Characterization and Parameter Extraction

Large-signal, or nonlinear characterization is important to any MMIC device whose performance objects include gain compression, saturated power, efficiency,

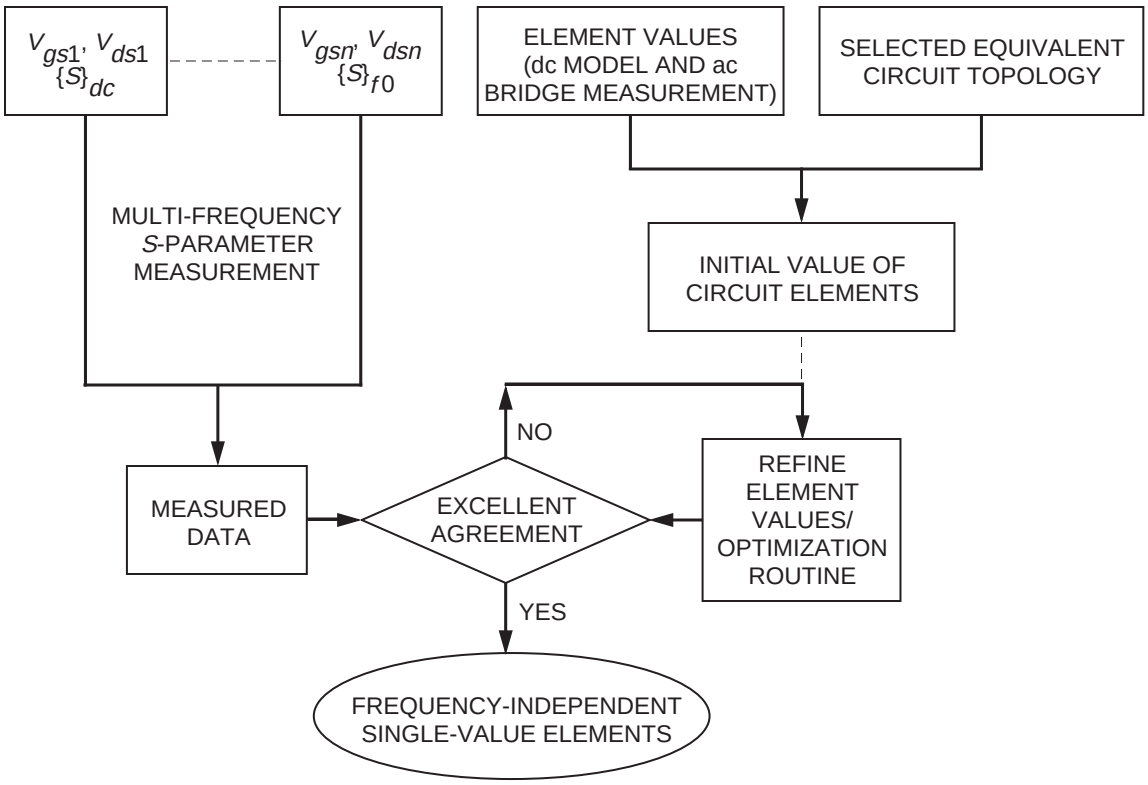

Figure 5-5. Small-signal direct model extraction process for *S*-parameter measurement at multiple frequencies.

harmonic distortion, and multitone intermodulation distortion products. There are a number of models for large-signal GaAs MESFETs; among the popular industry standards are the Curtice quadratic, Curtice cubic, and Statz(Raytheon) models. The equivalent circuit and I–V expression are different from model to model. Taking the Curtice cubic model for example, nonlinear I–V is expressed using a cubic approximation [3]:

$$I_{ds} = \left(A_0 + A_1 V_{in} + A_2 V_{in}^2 + A_3 V_{in}^3\right) \bullet \tanh\left(\gamma \bullet V_{out}(t)\right)$$

The coefficients A_i and γ are arbitrary empirical parameters whose values can be determined through parameter extraction, such that the evaluation of the equation is consistent with measured characteristics.

Large-signal characterization can be accomplished by two commonly used measurement techniques: load-pull and large-signal *S*-parameter characterization. Both techniques require measurements carried out on multiple signal levels to obtain complete characterization. The flow chart for device characterization and parameter extraction of large signal is shown in Figure 5-6. Large-signal models are applicable for both linear and nonlinear applications.

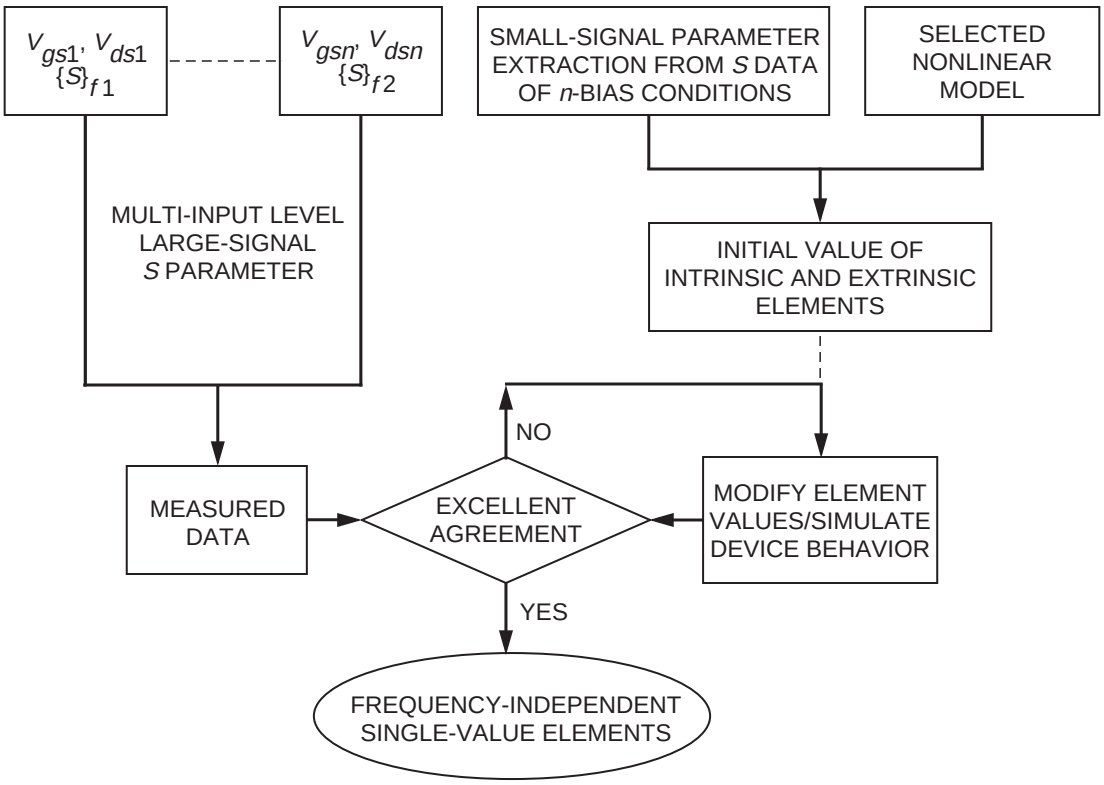

Figure 5-6. Typical flow chart of characterization and parameter extraction for large-signal model.

D. Noise Figure Characterization

A prime application of GaAs MESFETs has been in low-noise amplification. It is important to derive a simple analytic expression for calculating the minimum noise figure of a FET. Since the noise figure of a FET is affected by both bias point and generator impedance, the minimum noise figure, NF_{min}, defined here is an absolute minimum noise figure obtained by adjusting both bias and generator impedance.

Using the four equivalent element values—g_{mo}, C_{gc}, R_s, and R_g, determined by *S*-parameter measurement and small-signal parameter extraction—Fukui empirically derived a simple expression for NF_{min} [4]:

$$NF_{\min} \approx 1 + K_F \omega C_{gc} \left(\frac{R_s + R_g}{g_{mo}} \right)^{1/2}$$

where the factor $K_F \approx 2.5$ to 3.0 for FETs and $K_F \approx 1.5$ to 2.0 for HEMTs. The factor K_F is a gross simplification of the drain-current noise contribution to the overall noise. A noise model with an equally simple expression but retaining more comprehensive physics was derived by Delagebeaudeuf et. al. [5]:

$$NF_{\min} \approx 1 + 2\left(\frac{\mu_0' I_{CH}}{g_{mo} v_{sat} L_G} \right)^{1/2} \omega C_{gc} \left(\frac{R_s + R_g}{R_i} \right)^{1/2}$$

The first bracket is the expression for K_F in Fukui's model, which is related to channel current, I_{CH}, transconductance, gate length, and the saturated value of electron drift velocity. Using the relationship of the equivalent circuit elements and physical parameters presented in Section II, the expression can be further simplified:

$$NF_{\min} \approx 1 + 2\omega \frac{C_{gc}}{g_{mo}} \left(\frac{R_s + R_g}{R_i} \right)^{1/2}$$

Delagebeaudeuf et. al. have concluded that the equation also applies to HEMTs.

In a practical case, the generator impedance, $Z_g = R_g + jX_g$, connected at the input port, is a key factor influencing the noise figure of a circuit. The effect of this on the noise figure is given by [4]

$$NF = NF_{\min} + \frac{R_n}{R_g} \left[\frac{\left(R_g - R_{op}\right)^2 + \left(X_g - X_{op}\right)^2}{R_{op}^2 + X_{op}^2} \right]$$

where R_n is the equivalent noise resistance, and R_{op} and X_{op} are the optimum generator's resistance and reactance, respectively. Therefore, NF_{min}, R_n, R_{op}, and X_{op} are commonly defined as the characteristic noise parameters of the device.

IV. Modeling Software

MMIC modeling software includes device modeling and process modeling. Since there are a number of device-modeling softwares available, it is necessary to examine the compatibility of the software used by customers and the foundry, and between that used for modeling and simulation.

A. Device Modeling Software

HP/EEsof's Integrated Circuit Characterization and Analysis Programs (IC-CAP™) modeling suite Release 4.4 (HP 85190A) is a UNIX-based device-modeling toolset. The software allows users to develop their own model equation and extraction techniques, but also provides turn-key modules for a wide range of popular device models, including MESFET, HEMT, and HBT EDMs, as well as PBMs and HP Root data-based models. The software modules include measurement set-up, mathematical transforms, automation macros, and optimization routines to facilitate modeling. The model parameters are extracted by applying mathematical transforms to measured data. A Parameter Extraction Language (PEL) is built-in to facilitate creation of the transforms. The results of simulation based on the extracted model parameters can be plotted together with the measured data. IC-CAP contains three SPICE simulators and provides direct links to external simulators. The software has several optimization algorithms and user-controlled optimization settings. The sensitivity analysis mode provides information on important parameters for a particular optimization. The distinct feature of this software is the combined capabilities of instrument control, data acquisition, graphic analysis and optimization for device modeling. The software is compatible with HP/EEsof's Series IV™ and MDS™ simulation tools.

Optimization Systems Associates' (OSA) HarPE 2.0™ is a workstation-based nonlinear device-modeling software that includes parameter extraction and advanced statistical modeling. The built-in intrinsic nonlinear models include most popular models in the industry, such as several nonlinear FET models, a Gummel-Poon model for BJTs, models for HEMTs, and models for HBTs. It allows users to modify the built-in models or create user-defined models. It is capable of parameter extraction from harmonic data obtained under RF large-signal excitation or small-signal *S*-parameters taken over a number of bias conditions. It offers the option of extracting the extrinsic parameters from cold (unbiased and pinched-off) measurements. The software statistic modeling capability provides realistic yield analysis and optimization. It accepts *S*-parameter files in the touchstone format or the MDIF format, as well as on-wafer measurement data produced by Cascade Microtech's MicroCAT Test Executive system. The gradient-based minimax, L1, least-square, and Huber optimizers provide flexibility and accuracy in the modeling process. HarPE™ runs under X-windows on Hewlett-Packard, Sun, and DEC workstations.

Compact Software's Compact Scout™ is a PC- and workstation-based active device parameter-extraction and large-signal modeling software. It is based on the Modified Materka-Kacprzak model. The software uses measured data provided by the users to extract and fit the nonlinear model. It has interactive modeling features, which allow the users to modify parameter values and quickly observe the effect on both dc and *S*-parameter. It can optimize the model coefficients to fit both dc and *S*-parameter. An extensive parasitic model has been built around the intrinsic model for chip and package parasitic modeling. The software is compatible with Compact's Super-Compact and Microwave Harmonica.

Optotek's Small and Large Signal Analysis (SALSA™) is a PC-based software dedicated to MESFET and HEMT modeling. For large-signal modeling, it includes most of the popular nonlinear I_{ds} MESFET models, nonlinear C_{gs} and C_{gd} MESFET models, nonlinear I_{ds} HEMT models, and one nonlinear PBM. The software also offers small-signal parameter extraction programs for both intrinsic and extrinsic elements. Two types of Newton optimizers and two types of random optimizers are provided for solving and fitting the measured and modeled data. The automated data acquisition is realized using an automated network analyzer and two programmable power supplies. It is compatible with Optotek's simulation software MMICAD™.

B. Processing Simulation Software

Stanford University Process Engineering Model (SUPREM™) is one of the widely used process simulation programs developed by Integrated Circuit Laboratory of Stanford University. SUPREM-IV.GS™ is an advanced 2D process simulator, which models GaAs and its dopants in addition to modeling silicon fabrication. The software provides physical models for ion implantation, and diffusion and annealing on a cross-section of arbitrary device structures. It also includes basic models for simulating etching and the deposition of thin films on the semiconductor surface, or it interfaces with other programs to accurately simulate these processes. SUPREM-IV.GS™ can model stress gradients produced by overlaying film. The implantation, diffusion, and annealing models are point-defect-based simulations.

SUPREM-IV.GS™ incorporates most features of the previously developed SUPREM 3.5's 1D GaAs models and parameters. SUPREM 3.5™ is primarily designed for modeling processes used to make simple ion-implanted MESFET and JFET structures in semi-insulating GaAs, with or without buried p-layers. The main processes modeled

are ion implantation and active annealing. The dopants modeled are Si, Se, Ge, and Sn (n-type), and Be, Mg, Zn and C (p-type). Also modeled is the diffusion for non-implanted dopants, such as those incorporated during MBE or MOCVD GaAs growth.

Based on SUPREM™ 3.5 and its added 2D capability, SUPREM-IV.GS™ includes some new features. The Pearson-IV implantation parameters have been included. The electron- or hole-dependent diffusion coefficients have been added for the eight dopants. Segregation coefficients, intrinsic carrier concentrations, and defect energy levels have also been included. Furthermore, compensation mechanisms for dopant activation and different diffusivities for implanted versus grown-in dopants have been added.

V. Model Sensitivity

The design of a device always begins with initial fixed parameters. The next problem is to determine the sensitivity of the device to variations in all those parameters, which include material and process parameters along with other factors, such as temperature and bias. A robust design may be achieved with a thorough sensitivity analysis.

A. Sensitivity Analysis

The fabrication of MMIC devices involves a large number of interrelated material and process parameters that influence the performance of MMIC devices. In practice, the material and process parameters inevitably will be different from the designed values, because of the control in the fabrication process. Therefore, it is important to determine the sensitivity of the circuit to the variation of each parameter [1].

Sensitivity analysis includes two levels. The first level analyzes the correlation between variation in a single material or process parameter and variations in equivalent circuit elements. For example, a single variation in the layer of doping, N, leads to correlated changes in C_{gc}, C_{gd}, R_i, g_{mo}, and the gate transit time, τ_{gm}. Other parameters, such as W, Z_G, and L_G also cause correlated changes in various equivalent-circuit elements. The second level analyzes the correlation between the material and process parameters themselves. For instance, the size or position error of the gate strip, L_G, in Figure 5-2 brings correlated changes in L_{SG} and L_{GD}. A typical flow chart for MMIC sensitivity analysis is presented in Figure 5-7.

B. Temperature Effect

The effects of temperature on MESFET performance include variations in transconductance, input capacitance, and device resistance. Transconductance variations are caused by an increase in electron mobility in the active channel as the temperature decreases. Variation of input capacitance is induced by an increase in the built-in Schottky voltage as temperature decreases. Resistance variation is caused by changes in the metallurgical nature of ohmic contacts in the source and drain areas at low temperature. Temperature changes have an impact on device equivalent circuit models and *S*-parameters, as well as noise-figure models. Using extensive *S*-parameter measurements at different temperatures, a modified model including the effects of temperature can be created. The modified GaAs FET model should accurately predict the

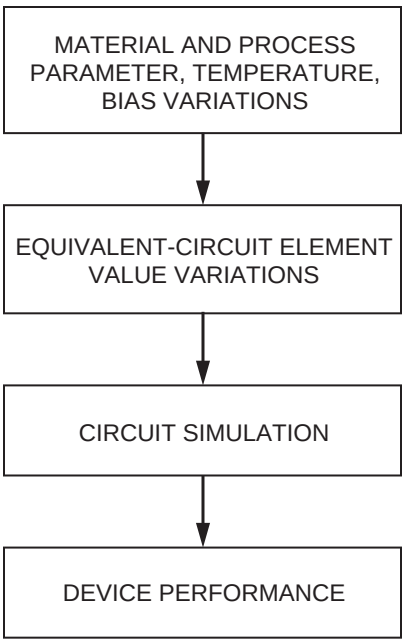

Figure 5-7. Flow chart for MMIC sensitivity analysis.

gain and noise figure at any temperature. Compact Software's Version 4.0 of Supercompact™ PC microwave simulation software has the capability of temperature-sensitivity simulation.

C. DC Bias Effect

As the discussion in Section 5-II indicates, the values of equivalent-circuit elements are directly or indirectly affected by dc biases. Therefore, the analysis of model sensitivity has to take dc bias effects into consideration.

Some elements, such as C_{gc}, C_{gd}, R_d, and τ_{gm}, are affected by the extension X of the depletion layer into the gate-drain space. X increases as $V_{D'G}$ increases and decreases as $V_{S'G}$ increases. Table 5-1 lists some important elements and their variation with biases.

Table 5-1. Relationship between variations of bias and element values.

Bias	Equivalent circuit element
$V_{GS'}$ ↑	g_{mo} ↑
$V_{GS'}$ ↑	R_i ↓
$V_{GS'}$ ↑	L_g ↓
$V_{D'S'}$ ↑, $V_{S'G}$ ↑	g_o ↓
V_{DS} ↑, V_{GS} ↑	C_{gc} ↑
V_{DS} ↑, V_{GS} ↑	C_{gd} ↓
V_{DS} ↑, V_{GS} ↑	τ_{gm} ↑

D. Statistical Analysis

In reality, the material and process parameters vary together, along with temperature and bias, unlike the previously described scenario in sensitivity analysis, where the effect of only one parameter variation is analyzed at a time. To assess the sensitivity of an MMIC to a given process parameter, it is better to approach the problem with an analysis that progressively restricts the parameter in question while continuously varying all others within known statistical limits; such a process is called statistical analysis [1]. The prerequisite for this technique is to establish the statistical distribution of all material and process parameters.

The Monte Carlo method is a popular and powerful technique for statistical analysis. Figure 5-8 is a flow chart of the Monte Carlo method applied to MMIC-yield forecasting. To have a reliable yield forecast using the technique, a large enough trial must be performed. The random values of material and processing parameters should duplicate exactly the empirically determined distribution. Where two or more tightly correlated distributions are involved, only one computer-generated random number is used to generate the correlated values. The Monte Carlo method can be applied not only to yield forecasting but also to assessment of design robustness and process control. It offers an alternative to the vastly expensive and time-consuming approach of practical trial and iteration of MMIC design and fabrication.

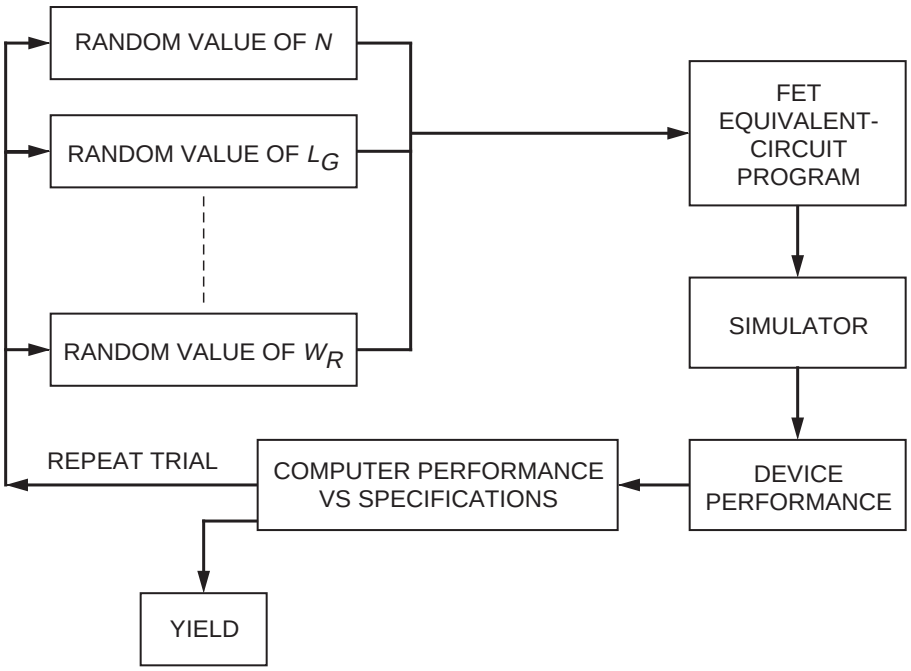

Figure 5-8. Application of the Monte Carlo method to MMIC yield forecasting.

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