Chapter 6.   MMIC Design Methodologies and Verification

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The implementation of a MMIC design involves a number of circuit simulation, layout, fabrication, and testing steps. The large number of variables involved in these steps makes it imperative that all facets of the implementation be documented to assure repeatability of similar designs and improve the yield of the final product.

This chapter will describe the general aspects of MMIC design and the necessary tools available to both the user and manufacturer. This chapter will also provide a typical design methodology and flow used by MMIC foundries.

I.   Foundry Documentation

A well-documented MMIC design methodology ensures a much smoother and faster turnaround of circuits. Circuit designs along with information relating to layout, processing, and testing can be preserved and used for future applications, thereby eliminating duplication of effort and providing substantial time and cost savings. This will not only assure a well-controlled and repeatable environment, which is essential for high-volume and high-yield applications, but also increases the probability of first-time success for new designs. As an added benefit, detailed documentation also guarantees a shorter period for the assimilation of new employees.

Documentation of a foundry's capabilities and design rules is necessary for internal use of the foundry's personnel and for external customers using the foundry's services to fabricate their own MMICs. Literature related to design rules, processing, and testing also provides the customer with an overall understanding of the end-to-end MMIC implementation.

In general, the available documentation should provide the interested customer with a description of the CAD tools, semiconductor processing steps, and test methods used at the foundry. From a users perspective, the level of documentation available at a MMIC foundry is a reflection of the maturity of the facility and the extent of process control being applied and practiced. Some typical documentation may include:

(1)   Semiconductor processing capabilities.
(2)   Design and layout rules used at the foundry.
(3)   Design and layout tools used at the foundry.
(4)   Available library designs.
(5)   Available simulation tools.
(6)   Available device and circuit element models.
(7)   Design and processing flow.
(8)   Design verification and review.
(9)   Design and processing schedule information.
(10)   Test methods.

II. MMIC Simulation

Circuit simulation is an essential step in the design and fabrication of MMICs for production purposes. Simulations can provide a first-order approximation of circuit functionality and performance under various input and output conditions prior to committing the design to fabrication. Since most simulators also include an optimization capability, circuits can be fine tuned, or in some cases synthesized, to meet the required performance specifications. This greatly reduces design turnaround time and increases the chances of first-time success. With the increased affordability of computing power and the recent advances in software development, many new software techniques and systems have become available for interactive MMIC design. The development of commercial software that integrates the various stages of MMIC design, such as schematic capture, simulation, and layout, has been the result of recent technology advancements and initiatives on MMIC CAD motivated by the identified need in the marketplace for these tools.

One of the biggest obstacles in transferring a customer-developed MMIC design to a MMIC foundry is the issue of design-tool compatibility. The customer must verify that the tools used by both entities for the design and simulation are compatible. The most common MMIC design and simulation tools are offered by HP/EEsof and Compact Software. Both companies provide a wide variety of tools for both linear and nonlinear simulations and links to layout.

Compact Software's Microwave Harmonica® is one of the primary design and simulation tools used for GaAs MMICs. This tool is used for both linear and nonlinear microwave circuit simulations. Microwave circuit structures are simulated using distributed element models, where nonlinear circuits are simulated by using harmonic balance techniques at the interface between the linear and nonlinear portions of the circuit. All the necessary components can be entered in either schematic or netlist form. This simulator also includes optimization, statistical analysis, yield optimization, and voltage synthesis, as well as oscillator and phase-noise analysis and optimization. Various portions of this software package can be used to address specific aspects of MMIC design.

The Compact Software Microwave Explorer® is a 3-D electromagnetic analysis tool used the for simulation of planar passive structures in both open and packaged environments. Circuits can be entered into the program through the use of either the Integrated Polygon Editor or the GDSII import utility. This package includes a graphics interface for viewing results on Smith charts, rectangular plots, or current distribution plots.

The Compact Microwave Success® is a block-level simulator used for examining such data as S-parameters and noise parameters for communication systems consisting of RF and microwave components. Success® systems can be built from a large set of models such as mixers, filters, antennae, and amplifiers. The package will also generate data in several other standard formats; it can provide analysis as a function of temperature, frequency, power, and other user-defined variables. The results can be displayed as time-domain waveforms, spectrum plots, sweep results, intermodulation results, and budget analysis.

HP EEsof's Libra® is another primary design and simulation tool used for both linear and nonlinear GaAs MMIC microwave-circuit simulations. Libra® performs frequency-domain simulations by using distributed element models for microwave circuit

structures. Nonlinear circuits are simulated by using harmonic balance techniques. Different portions of this software package can be used for the simulation and optimization of specific aspects of MMIC design. The HP/EEsof Libra Design Suite® is a simulation and layout toolset developed for RF and microwave design engineers. The Series IV Project Design Environment® is a graphical design environment for the design, simulation, layout, and documentation of high-frequency circuits and systems. This package includes capabilities for schematic capture, high-frequency circuit simulation, electromagnetic simulation, system simulation, and circuit layout, along with an extensive design library and various tools and links to third-party software.

The HP/EEsof Microwave Design System® is a UNIX-based computer-aided engineering (CAE) toolset tailored for high-frequency circuit and system design. This package has linear, nonlinear, transient-simulation, and sensitivity analysis capabilities and provides electromagnetic simulation and yield analysis. Design capture and circuit layout are also provided.

Other available simulation tools include Mathematica®, which is an interactive software package used primarily for the solution of complex mathematical problems and the development of mathematical models for microwave components and systems. Microwave Spice® is a time-domain circuit-simulation tool similar to the Berkeley Spice® package. This package includes many microwave effects and components that make it useful for microwave MMIC designers. This package is particularly useful for the development of microwave oscillators.

The Cadence Analog Artist Microwave Simulator Interface® is a linear frequency domain simulation tool that can be used within the Cadence IC environment of Analog Artist® with microwave extensions. The package can provide simulations using HP/EEsof or Compact software tools. Simulations can also be provided using Microwave Interconnect® layout format. Additionally, Cadence Spectre® and SpectreHDL® support frequency-domain blocks in time-domain analysis and behavioral modeling in the time domain; it is written in the SpectreHDL® language. The package can provide transient analysis via S-parameter blocks for microstrip lines, behavioral modeling for devices and circuit blocks, and mixed-level time-domain simulation.

EM simulation tools used either in conjunction with time- and frequency-domain simulators or as stand-alone EM simulators include Ansoft Maxwell Eminence®, which is a 3-D EM simulation tool consisting of a solid modeler for model entry, a simulation engine, and several data analysis features. The simulation engine creates its own mesh by way of an adaptive meshing algorithm. The user can specify both the convergence criteria and the maximum number of iterations in order to balance accuracy and time. Sonnet® is another 3-D EM simulation tool capable of accepting inputs in GDSII, HP/EEsof, Cadence, and AutoCAD formats. Outputs are generated as S-parameters, current distributions, or radiation patterns.

III.   MMIC Layout

Conversion of the MMIC design into a layout can be accomplished in two ways; the first uses a commercially available CAD software program to manually perform the layout from a hard copy of the schematic or netlist. The second uses advanced software tools, such as Cadence or HP/EEsof, to transfer the schematic to layout in real time. The output from these programs can then be modified to comply with foundry design rules.

There are several layout tools available for GaAs MMICs. CALMA was one of the early programs. The GDSII format, developed by CALMA, has become an industry standard for data communication and file transfer, regardless of the actual program being used. The universal acceptance of the GDSII format and its ability to handle up to 63 layers makes it the preferred method of data communication and design file transfer.

Mentor Graphics and Cadence packages offering complete MMIC design capability, including simulation, optimization, and layout, are two of the most commonly used software layout tools in the GaAs MMIC industry.

Tools specializing in design layout verification compare the actual chip layout to the circuit schematic and physical design rules and then provide specific error reports with defined locations. Some packages can also provide suggested corrective actions. One of the most common of these tools is ECAD Dracula® Integrated Circuit Layout Verification System, which provides layout-vs-schematic comparison and design rule checks.

Design rule checks are performed by comparing the geometric spacings of the MMIC layout against predefined physical design rules. These rules depend on the technology and processing capabilities of the foundry and are therefore generated by individual foundries; they are applicable to the foundry's processes only. Advanced trapezoidal approaches along with the introduction of electrical node determination and multilevel conjunctive rule capability can eliminate false errors.

In general, design rules take into account orientation effects, device spacing limitations, and probe and pad placement, among other parameters and physical restrictions. The relative placement of elements such as FETs and diodes at the die and wafer levels can have an impact on the performance of these devices, while most passive components are not sensitive to this effect. For power transistors, the spacing between the gate fingers can have a direct impact on the channel temperature and the overall performance, reliability, and stability of the device. These effects are considered in the design-rule-check stage and should be taken into account during the initial design and layout of MMIC.

IV.   Typical Design Methodology

In the competitive marketplace, cost reduction at all stages of design, fabrication, and test is of prime importance. The use of CAD simulation and layout tools plays a pivotal role in first-time success and yield of a MMIC design.

Designing a MMIC involves two critical stages: performance specification, and circuit design and simulation. Other functions such as fabrication and test must also be considered during the design stages to arrive at a manufacturable product with high yield and the desired performance.

The definition of performance specifications must take into account customer needs, the technology, and the processing capabilities. Detailed understanding of the system requirements is necessary to arrive at design parameters applicable to the technology desired by the customer. Attempts to force-fit a design into an unsuitable process or to require performance parameters that cannot be supported by the process can

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create substantial cost and schedule delays, low yield, and a product of suspect reliability. In typical applications, the following must be addressed:

    (1)   Translation of customer requirements to design instructions.

    (2)   Suitability of technology and process to design requirements.

    (3)   Availability of existing designs.

    (4)   Cost, schedule, and performance trade-off.

The translation of the customer's requirements into the manufacturer's design instructions is another critical point in the process. The MMIC design approach must take into account the available CAD software tools and identify the relevant cell libraries and applicable models. The choice of software tools depends on the need for linear or nonlinear simulation, time or frequency simulation, EM simulation, and the desired use of schematic capture for layout.

In the early stages of the MMIC design, the customer must examine the available cell library devices and components to determine their applicability in meeting the performance requirements. Usually, multiple iteration of a design is a common practice and helpful in identifying, through simulation and optimization, the best possible performance characteristics. Conducting a yield and sensitivity analyses as part of this iterative process will enhance the probability of first-time success and ensure an acceptable yield.

MMIC layout is also an important process that makes use of design-rule checks against circuit schematics to arrive at the final layout. A layout review prior to pattern generation is a normal practice.

Design reviews should be an integral part of the overall MMIC design process and should occur at various steps during that process. An initial design review normally examines the performance requirements, the choice of technology, and the identified cell libraries. A preliminary design review examines the suitability of the initial design in meeting the requirements and includes the circuit simulation results. A critical design review is normally used to finalize the chip design and identify the layout approach. A final design review addresses the complete design, simulation results, chip layout, and manufacturing procedures. These reviews may be conducted internally at the foundry or may include customer participation, which is highly desirable at least in the initial and final design review stages.

V.   Design for Reliability and Manufacturability

Several factors may have a direct or an indirect impact on circuit yield and reliability. Device parameter variations as a result of process limitations or level of control, raw material variations, and EM proximity effects all play roles in determining overall circuit reliability and yield. The approach for achieving a reliable design should take into account the following:

    (1)   Definition of realistic performance requirements.

    (2)   Documentation of design methodology.

    (3)   Material and processing characterization and variation.

(4)   Understanding of potential failure mechanisms.

(5)   Use of adequate simulation and test tools.

The definition of realistic and achievable performance requirements is probably the most important initial step in MMIC design. Pushing the design-performance boundaries may result in selection of devices that fall at the edges of the normal Gaussian distribution. This will result in low yield and may have an impact on the reliability of the selected components. Therefore, design-performance requirements should fit very comfortably into the high-yield and assured-performance window of a MMIC foundry's process.

A documented design methodology can provide a clear path for device design, simulation, layout, and fabrication. This approach will also allow a smoother design implementation and identification of unacceptable design limits or points of possible yield loss. Figure 6-1 shows a typical design flow and the various necessary inputs.
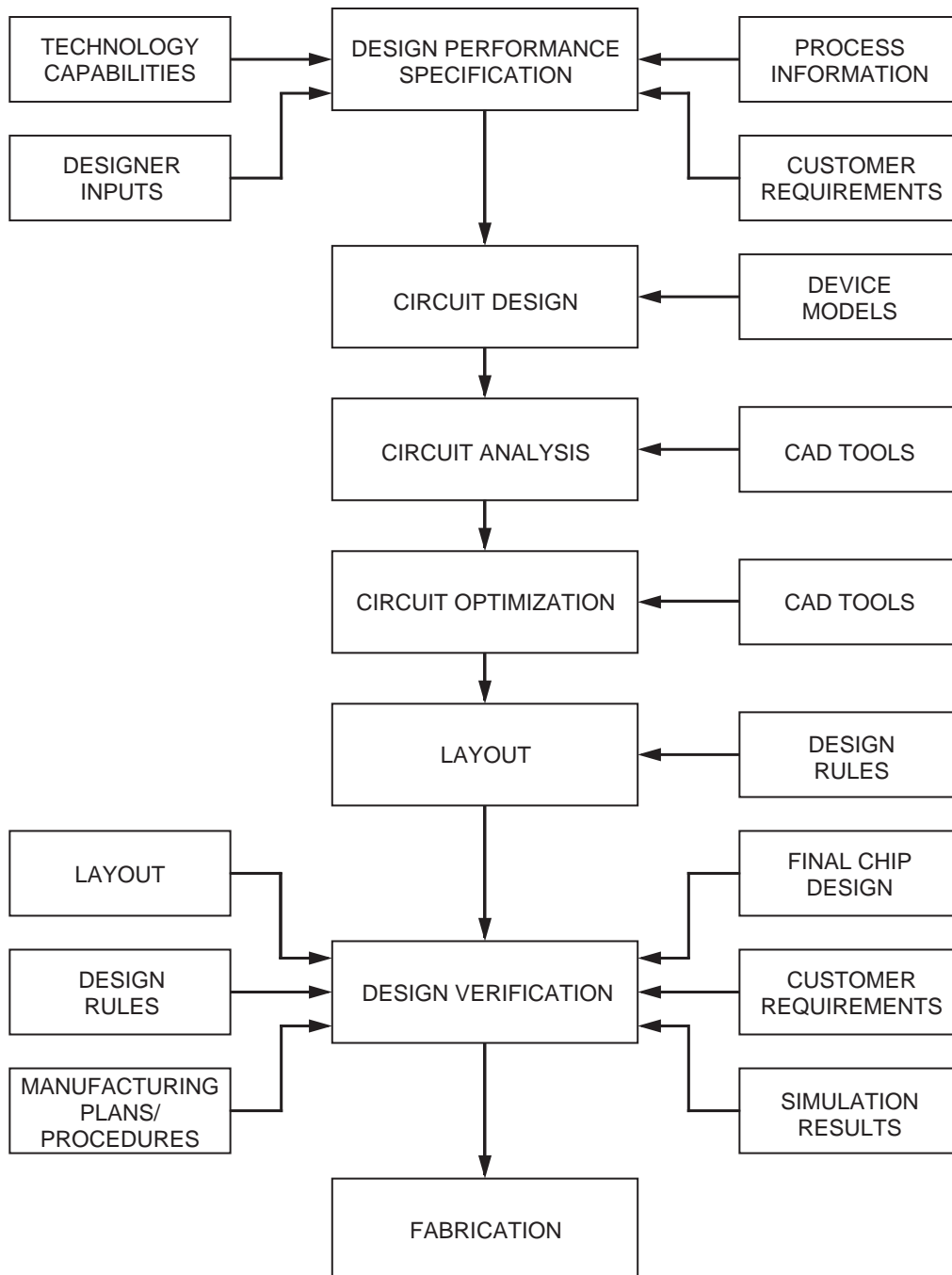
The characterization of the processes and materials used throughout the fabrication cycle is also connected to an understanding of the common failure mechanisms and other reliability aspects of device and circuit design. As an example, gate length and placement-variation effects have been shown to be the dominant factors in limiting the yield of semiconductor devices. To meet performance requirements at higher operating frequencies, shorter gate lengths are normally required. However, this results in smaller gate-metal-to-semiconductor contact area, which is more critical from the yield and reliability aspect. Another parameter of importance is the chip length-to-width aspect ratio; it should be kept as close to 1:1 as possible to increase overall yield and reduce chip breakage during the dice and sort operations. A maximum chip length-to-width ratio of 3:1 is the normally recommended ratio for MMICs.

Layout design rules, derived from empirical and process-variation data can be very valuable in increasing the yield and reliability of a MMIC design. Considerations for circuit element placement, sizing, process variations, and physical tolerances play an important role in determining the reliability, yield, and final cost of the product. Yield analysis techniques are normally practiced to determine the overall yield and identify areas of poor yield performance. Additionally, sensitivity analysis techniques are commonly employed to determine a design's sensitivity to variations in bias point, device process parameters, tolerances, and thermal conditions.

In-process and on-wafer testing of MMIC components can provide valuable information on the performance and yield of the final product. Comparison of these data with those of the process can indicate the manufacturability of the design for a particular foundry.

Additional Reading

M. Gillick and I.D. Robertson, "Passive Components," *MMIC Design,* I. D. Robertson, Editor, The Institution of Electrical Engineers, United Kingdom, 1995.

Ladbooke, P. H., *MMIC Design: GaAs FETs and HEMTs,* Artech House, Boston, 1989.

Figure 6-1. Typical design flow.