Chapter 7. Testability and Test Structures

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A major concern in the use of advanced technology in a high-reliability application is the quality and reliability of the product. Generally, the user's confidence that the product will meet an expected level of reliability and quality is based on documented data supplied by the manufacturer. To give the data significance, the manufacturer of the product to be validated for use in a space or other high-reliability system must have the user's expectations defined in a measurable set of values. These expectations and performance values for reliability and quality assurance are often incorporated in a "product specification." A typical product specification identifies electrical and environmental screening tests and visual inspection requirements to be performed on the product at various steps in the manufacture of the unit. These tests and visual inspection requirements are not usually done as part of the product fabrication process, but are rather a verification of conformance after the process has been completed. As such, they require additional handling and may impose stress to the part. Also, it is possible that deficiencies affecting the quality and long-term reliability of the product could be due to the design limits of the technology or the validity of the fabrication process control limits. These deficiencies are usually not found by performing a qualification based on the screening tests and inspections associated with the "product specification."

The qualification methodology proposed in this document includes process and product qualifications to help ensure that the technology, the fabrication, and the MMIC performance meet the expected level of quality and reliability. The MMIC process qualification is an evaluation of the technology's ability to attain certain defined reliability and performance levels using the manufacturer's documented processes. The process qualification usually identifies the design limits and the process deviation limits accepted by the manufacturer. The MMIC product qualification is a validation of the circuit design to perform to a minimally defined electrical performance under stress and environmental conditions.

Elements that allow the measurement of parameters that document the evaluation of the technology and validate the fabrication process are known as test structures. The definition of these structures and when, where, and how to measure these parameters are the testability criteria.

I. Test Structures

Test structures similar to those described in the following subsections are usually employed by the manufacturer. It is important that these test structures be understood by the user for their value in validating the level of expected quality and reliability of the MMIC. The usual documents that describe these structures include design files, simulation results, rationale for the proposed design, and other documents.

A. Technology Characterization Vehicle

The technology characterization vehicle (TCV) is a structure that can be used to characterize a technology's susceptibility to intrinsic reliability failure mechanisms such

as electromigration, interlayer dielectric integrity, and metal diffusion. The TCV can be composed of basic active and passive elements from the cell library including specific elements relevant to the technology. Typical elements contained in the TCV are (1) the basic FET; (2) diodes; (3) usually capacitors of two values, the lowest value in the design and a value between 1 pF and 10 pF; (4) inductors, usually the highest value; (5) resistors, all types in the design (e.g., implanted and metallic); (6) air bridges; (7) via holes; and (8) calibration elements, such as open and short circuits. Parametric Monitor (PM) elements may be included within the TCV or be the actual TCV. The TCV is usually designed close to or at the limit of the design rules and the test structures should verify all relevant material, process, and various fixed-cell dc parameters such as

interface properties	ohmic contacts
sheet resistance	implantation
etching	via hole
side/back gating	air bridge
interconnection layer	leakage currents
discrete capacitors	mask alignment
wire and die bonding	

In general, TCV certification includes subjection of a sufficient number of test structures for each wear-out mechanism to an accelerated life test to produce an estimate of the mean-time-to-failure (MTTF) and a distribution of the failure times. The MTTF and failure distribution are then used to predict a worst-case failure rate or worst-case operating lifetime at the normal operating conditions. The accelerated life tests are usually performed on packaged TCV structures. The TCV is packaged using the same packaging material and assembly procedures as those used for standard circuits in the technology. An example TCV is shown in Figure 7-1. The acceptable certification of the TCV is an integral part of the MMIC process reliability evaluation.

B. Standard Evaluation Circuits

Typically, the manufacturer has a standard evaluation circuit (SEC) used to demonstrate fabrication process reliability for the technology to be validated. The SEC design documentation usually includes the design methodology, the software tools used in the design, simulation of design performance, the design function, and the fabricated size in terms of the utilized transistor or gate count. The documentation for the SEC can be the same as that for a production circuit. The SEC can be designed solely for its role as a quality and reliability monitoring device, or it can be a production or subset of a production circuit. Typical SECs include low-noise-amplifier and high-power-amplifier production level circuits. The SEC can exercise the worst-case design rules, or, if it is a standard product, the normal design-rule limits allowed in the manufacturer's design guideline. The complexity of the SEC should be at least one half of the number of transistors or gate count of the largest MMIC to be fabricated. Usually the SEC is dc life tested if it is a small signal device process and dc and RF life tested if it is a power device process. Generally, temperature-accelerated life testing is used as the aging test. As with the TCV, the accelerated life tests are usually performed on packaged structures. The SEC is packaged using the same packaging material and assembly procedures as those used for standard circuits in the technology.

Unlike the TCV, which includes elements only from the design cell library, the SEC is a circuit device or an actual circuit that can be used as an indicator of the process stability through microwave parameter measurements. The parameters measured on the SEC are usually implemented in a data base to establish comparisons from wafer to wafer

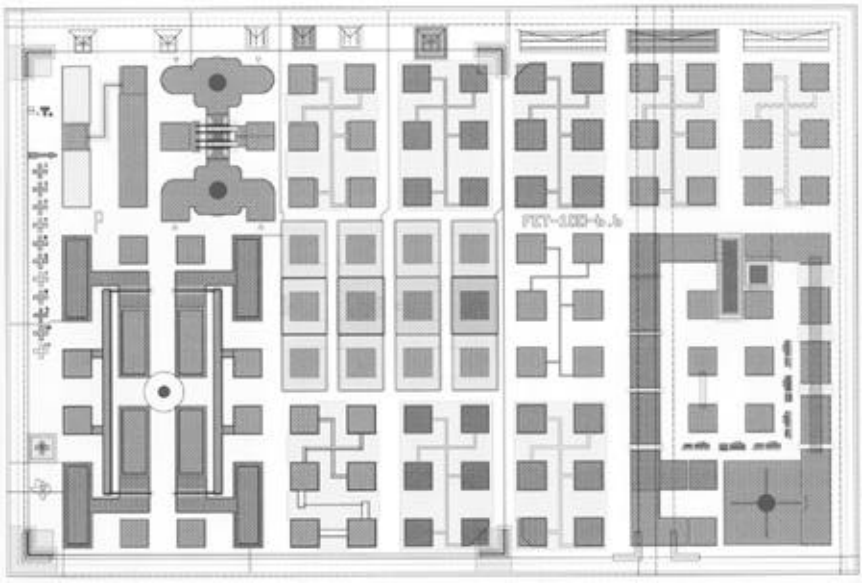

Figure 7-1. TCV example. (Courtesy of Texas Instruments.)

and lot to lot. Acceptable certification of the SEC is an integral part of the MMIC process reliability evaluation.

C. Parametric Monitors

Parametric monitors (PMs) are used as a means of measuring electrical characteristics of each wafer in a specified technology. The PM test structure can be implemented in one of several ways: incorporated into the grid, located within a device chip, designed as a dedicated drop-in die, or any combination of these. Usually several areas on each wafer are reserved for PMs. The location of the PM structures should allow the determination of uniformity across the wafer. An example of the PM locations across a wafer is shown in Figure 7-2. The manufacturer usually documents these PM locations for the user. The manufacturer's documentation could establish reject limits, record retention for wafer-to-wafer variation, and describe measurement procedures, critical parameters used in process control, and how routinely these parameters are scrutinized for statistical process control (SPC) analysis. Table 7-1 gives examples of various PM test structures and the parameter to be monitored by the structure.

Technology characterization vehicles, standard evaluation circuits, and parametric monitors required for design verification, process reliability, and performance information should be described in the Quality Management Plan. Typical information that should be addressed in the Quality Management Plan on test structures is shown in Table 7-2.

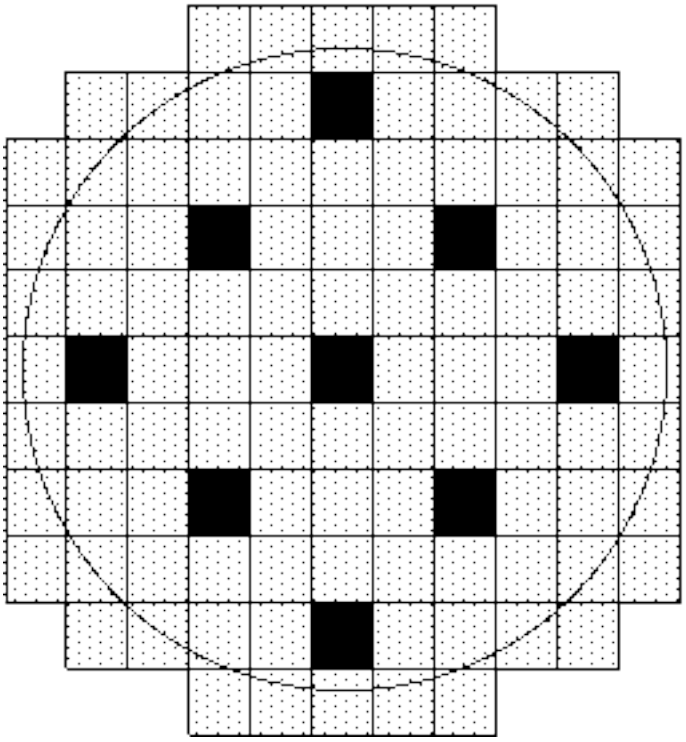

Figure 7-2. Example of parametric-monitor locations across the wafer.

Table 7-1. Common parametric monitors.

Structure	Monitored Parameter
Van der Paaw Cross	Sheet resistance
	Line width
MIM capacitor	Capacitance
	Leakage current
Transmission line structure	Contact resistance
	Sheet resistance
	Transfer length
	Saturation current
Isolation gap	Isolation gap breakdown voltage
Air-bridge chain	Air-bridge defect density
FET	Diode characteristics
RF-probeable FET	Dc characteristics
	S-parameters
	Extracted small-signal model
Via-hole alignment structure	Misalignment resistance

Table 7-2. Typical test structure information.

Test Structure	Typical Information
TCV	Failure mechanism identification. Failure mechanism method of test. Suitability of TCV to identify failure mechanism. Method of TCV implementation. TCV design parameters and applicability. Test conditions and parameters.
SEC	SEC determination methodology. SEC suitability to desired product function and design. SEC test conditions and parameters. Level of available reliability information.
PM	Description of the PM. Function of the PM. Location of the PM and method of determination. Suitability to the technology and design. Test conditions and parameters. Method of test.

II. Testability

Testability is the ability to measure defined parameters associated with the MMIC fabrication process. These measurements can be used to validate the MMIC design, to evaluate the technology in terms of reliability, as a catalog for statistical process control (SPC) to indicate the process stability, and as device/wafer acceptance data records. The manufacturer and user should be in agreement as to the definition of the test structures and the when, where, and how of parameter measurement. The following subparagraphs give information on the levels of testability and typical parameters measured on test structures and MMIC devices.

A. Wafer-Level Testability

Usually dc on-wafer testing is performed on the test structures and MMICs with traceability and wafer mapping included in the measurement documentation. These tests are usually done with an autoprobing instrument. The dc autoprobe is used to test individual FETs, resistors, and capacitors on the circuit for dc characteristics and functionality. The tests are a key screening procedure and are used to ensure that all parts delivered have fully dc functional FETs, resistors and capacitors, and that the parameters for these components are within standard or desired specifications. The FET gate functionality (pinch-off) test is particularly important since it ensures gate functionality across the entire gate width. Usually, dc probing is performed after frontside processing and before backside processing. The lack of "via" connections to a backside ground plane allows for better dc isolation of circuit components. Measurements are taken on several parameters, such as transconductance (g_m), breakdown voltages (V_b), and pinch-off voltage (V_p), to address yield analysis.

Dc wafer probing can also be used at several steps during fabrication: after ohmic contact formation, after gate formation, after interconnect/air-bridge metal deposition, and after final frontside and backside processing are complete. This in-process

monitoring can help catch problems early in the fabrication of the wafer so that further processing of out-of-tolerance wafers can be avoided. This minimizes cost and helps to identify process control problems as early as possible.

Some manufacturers have the capability to perform on-wafer RF measurements for SECs and MMICs. Usually this probing is done by connecting RF measurement equipment such as network analyzers to specialized probes for injecting and detecting the microwave frequency signal through the device. RF measurements are made after both frontside and backside processing is complete but prior to chip separation and normally under the same bias conditions used in the application of the device. The technique generally used in RF probing is to place pads or "footprints" for signal connection at each RF port. The footprints are typically coplanar waveguide topologies and can be designed to be ground-signal (G-S) or ground-signal-ground (G-S-G) configuration depending on the type of probe to be used. On-wafer testing of high power devices can cause a thermal problem because of the relatively high currents that must be provided for bias and the usually poor thermal environment of the wafer probe system. This problem can be minimized by pulsing the dc bias to the device, but it is still a difficult measurement. Also, testing high-frequency devices on-wafer can cause an instability problem at lower frequencies because of the high forward gain of the transistors. Often the probe equipment and data logging equipment cannot detect this oscillation condition, and measurement errors or damaged parts may result. Table 7-3 lists several dc and RF parameters that are typically measured during on-wafer probing.

Table 7-3. Examples of dc and RF autoprobe test parameters.

DC Parameters
Saturated drain current (I_{DSS})
Transconductance (g_m)
Pinch-off voltage (V_p)
Gate-source breakdown voltage (V_{BGS})
Gate-drain breakdown voltage (V_{BGD})
Gate leakage current (I_{lk})
Capacitance (pF)
Resistance (Ω)

RF Parameters
Scattering parameters (S_{nn})
Associated gain (G_a)
Noise figure (NF)
Small-signal gain (SSG)

B. MMIC-Level Tests

Once the wafer has been tested and accepted, it is diced, sawed, or scribed, and the good dies are identified for MMIC chip delivery or evaluation test. At this point in most certification, acceptance, and/or qualification programs, several samples are further tested for individual MMIC reliability or design validation. Usually the test structure or MMIC is packaged using the same packaging material and assembly procedures as standard circuits in the technology. The packaged circuit is then dc and RF tested for validation to the performance level of the design limits. The MMIC validation program should validate, in terms of electrical performance and reliability, all the MMIC functions assessed at the technology evaluation and design review. The electrical performance testing done at this time is usually more detailed than the wafer-level testing described in the previous section. The device can be rigorously tested for design validation since it is packaged and precautions for oscillations and thermal issues can be more easily handled.

The following list gives examples of the RF tests that are typically performed on the MMIC:

Scattering parameters (S_{nn})	Power added efficiency
Associated gain (G_a)	Isolation
Noise figure (NF)	Switching time
Small-signal gain (SSG)	Intermodulation (distortion)
Output power at 1-dB gain compression	Phase linearity

The information collected from test structures can be a very valuable tool in understanding the overall stability and long-term reliability of the product. Also, data collected from test structures at various processing and manufacturing steps can be excellent indicators of the quality of the manufactured lot. The use of test structures and planning for testability are very common practices in the industry and should be used to their fullest potentials in developing the MMIC qualification plan.

Additional Reading

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