

Advanced Memories for Space Applications

John Rodgers, Ron Brown, Nadim Haddad

[**\(john.rodgers@baesystems.com\)**](mailto:john.rodgers@baesystems.com)

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A decorative graphic on the left side of the slide, featuring several overlapping circles and lines in shades of gray, creating a complex, abstract pattern.

Agenda

- **Radiation Hardened Memory Generations**
- **Commercial SRAM for Space**
- **Commercial DRAM for Space**
- **Advanced Packaging**
- **Future Memories for Space: C-RAM**
- **Conclusion**

Generations of Radiation Hardened Memory for Space



Memory Die	64K	256K	Enh 256K	1M	4M*	Enh 4M **
Technology Generation (RHC MOS)	-2 (1.0µm)	-2E (PS 0.8µm)	-4E/-4S (0.8 µ)	-5ML/-5M (0.5µm)	-5XL/R25 (0.4/0.25µm)	R25 (0.25µ)
Organization	X1,X8	X1,X8	X1,X8	X1,X4,X8	X8	X1,X16,X32
Die Size (mmxmm)	8.0X5.8	12.0X9.4	9.4X5.8	12.0X11.6	18.0X18.0	15.0X15.0
Cell Size (mm2)	430	285	135	89	50	35
Min. Lithography (mm)	1.0	1.0	0.7	0.5	0.5	0.24
Leff (mm)	1.0	0.8	0.5	0.5	0.3	0.18
Vdd (V)	5.0	5.0	5.0/3.3	5.0/3.3	3.3,2.5	2.5
Performance (ns)	40	30	25	25	30	12
Power (mW/MHz)	50	30	20/10	20/10	10,5	5
Qualification	QML	QML	QML	QML	2002	2002
Radiation Levels	Strategic	Strategic	Strategic	Strategic	Strategic/ Space	Space

64K SRAM developed under the Air Force GVSC contract: #29601-87-C-0006

256K SRAM developed under the Air Force contract: #29601-89-C-0016

Enh 256K SRAM developed under the DTRA contract: # DNA001-91-C-0117

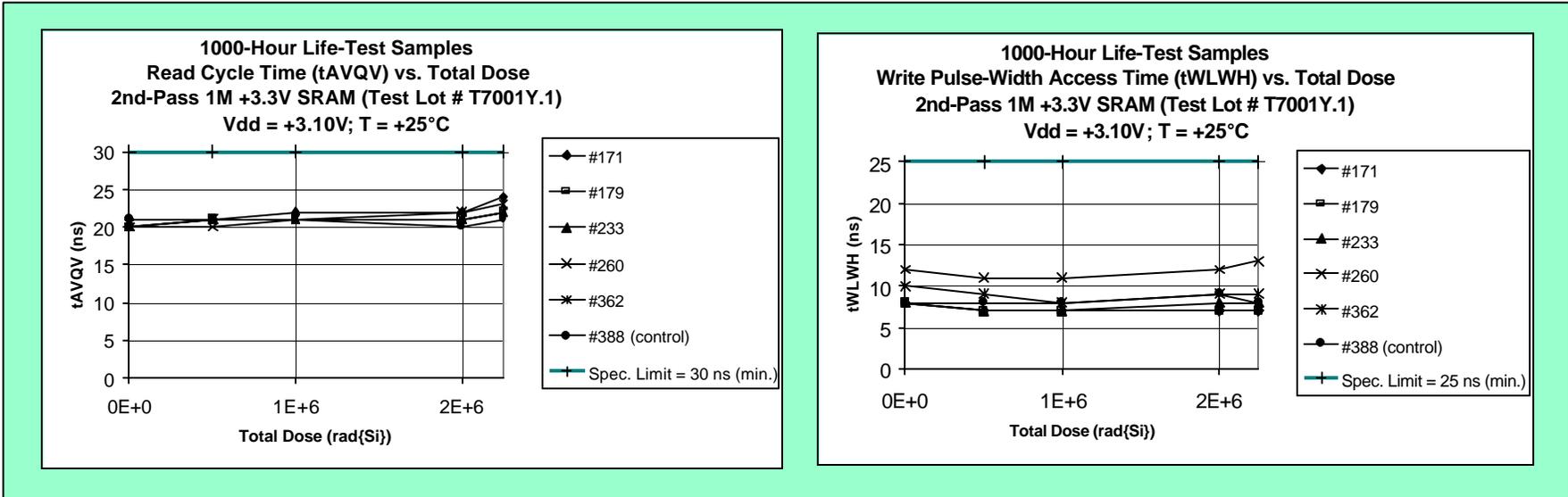
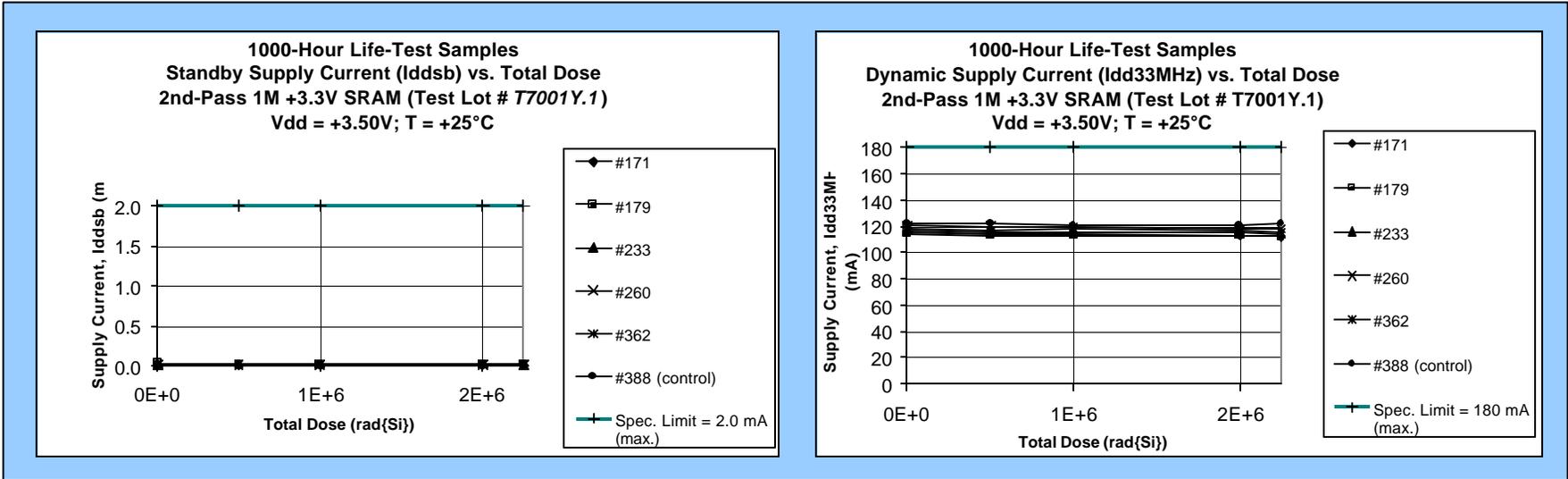
1M SRAM developed under the DTRA contract: # DNA001-91-C-0117

4M SRAM developed under the DTRA contract: # DSWA01-96-C-0106

* (DTRA,Quantum)

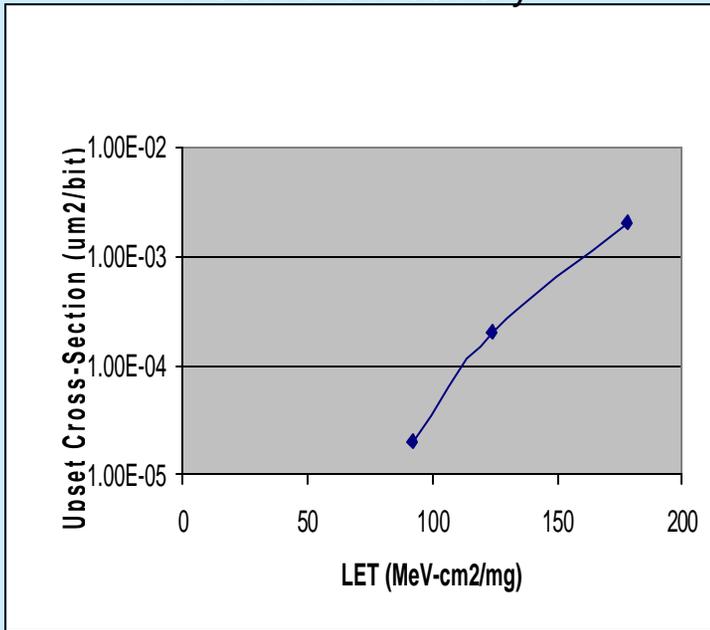
** Millennium

Total Dose Response of RH 1M SRAM (Rad Hard Foundry)



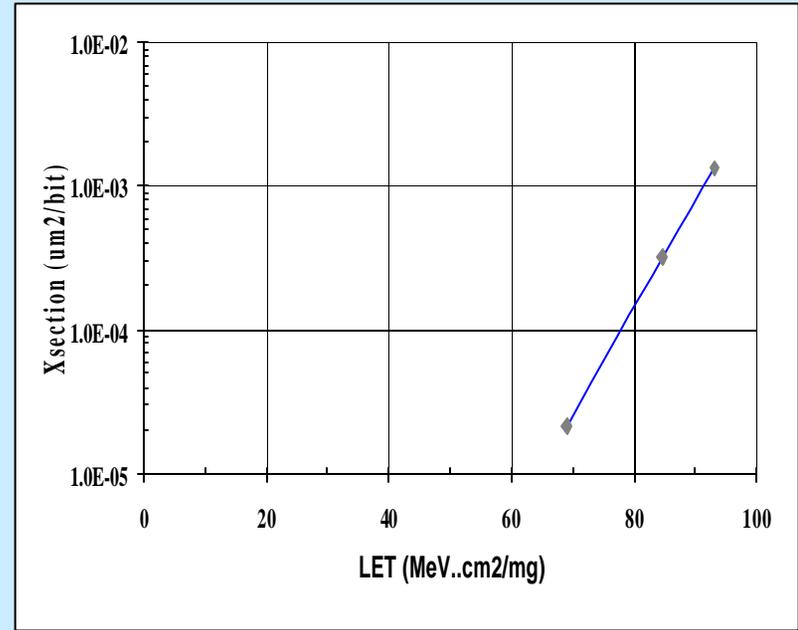
Rad-Hard Memory Heavy Ion Test Results

1M SRAM
Rad Hard Foundry



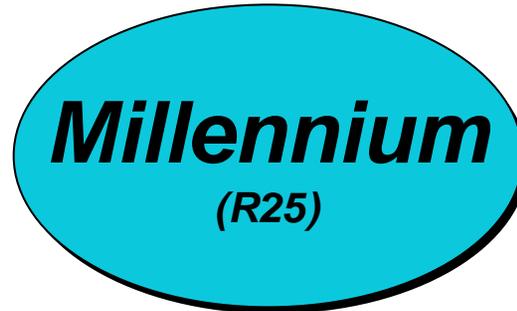
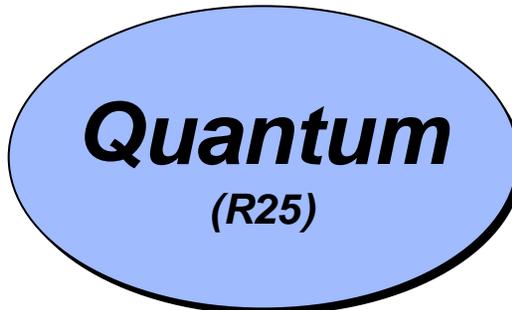
SER < 1E-12 Upset/Bit/Day
No Latch-Up

4M SRAM
Rad Hard Foundry



SER < 1E-12 Upset/Bit/Day
No Latch-Up

4M SRAM Derivative Product Objectives



0.5µm CMOS (Leff 0.3 µm)
512Kx8
3.3V
25ns / 2mA
7mW/MHz
Cold Spare + Interoperable I/O
40 lead flat pack
1Mrad (Si)
1E-10e/b-d 90% WC GEO
upper rad hard capability
Validated 2Q1999
Production 2002

0.25 µm Partially Scaled CMOS
512Kx8
3.3 & 2.5V
25ns / 1mA*
3-5mW/MHz (at 2.5-3.3V)
Cold Spare + Interoperable I/O
40 lead flat pack
200Krad (Si) Natural Space
1E-10e/b-d 90% WC GEO
Design Release 4Q1998 (2.5V)
Production 2Q2001 (3.3V)

0.25 µm Fully Scaled CMOS
128Kx32 / 256Kx16 / 512Kx8
2.5V
10ns / 1mA*
3mW/MHz
Cold Spare + Interoperable I/O
SCM/MCM/Stack
200Krad (Si) Natural Space
1E-10e/b-d 90% WC GEO
Design Release 1Q2002
Production 3Q2002

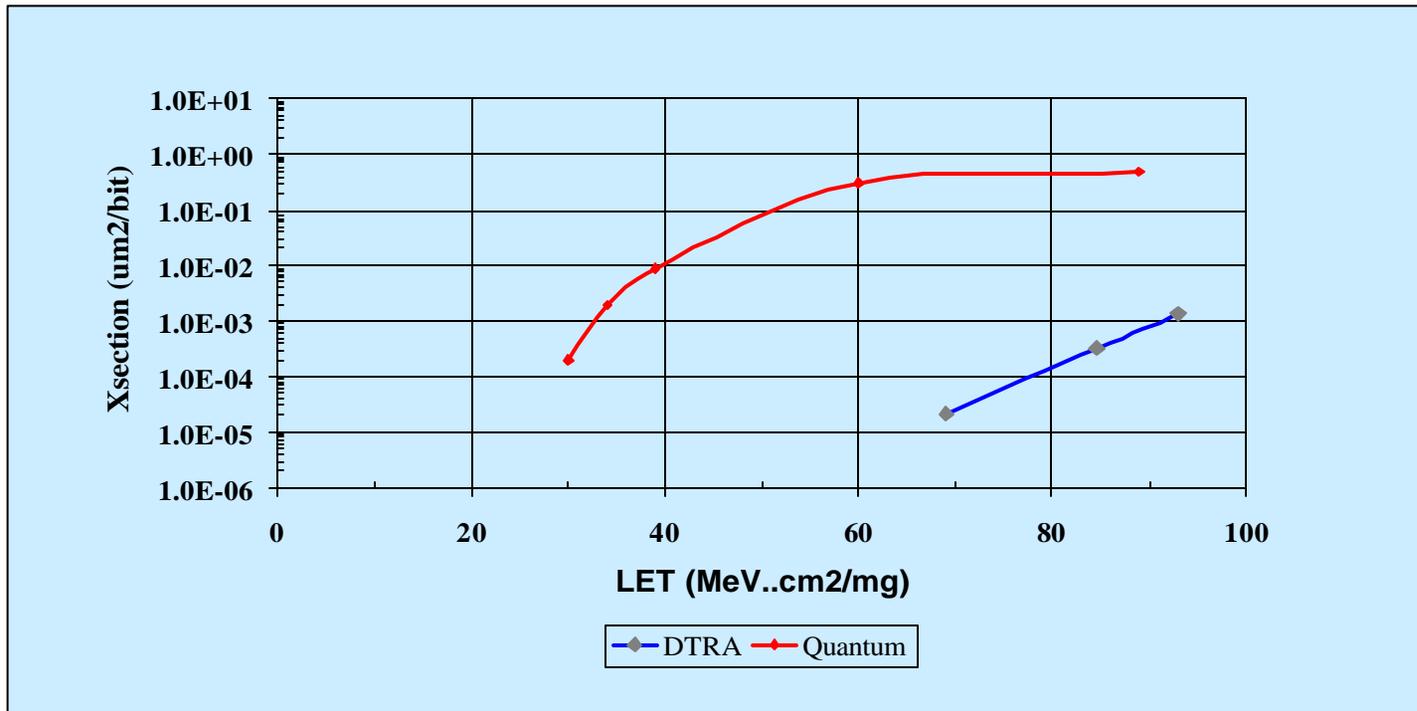
* Iddq tradeoff and temperature range to be evaluated

Radiation Hardened 4M SRAM Successfully Migrated to 0.25 µm CMOS

Rad-Hard Memory Heavy Ion Test Results



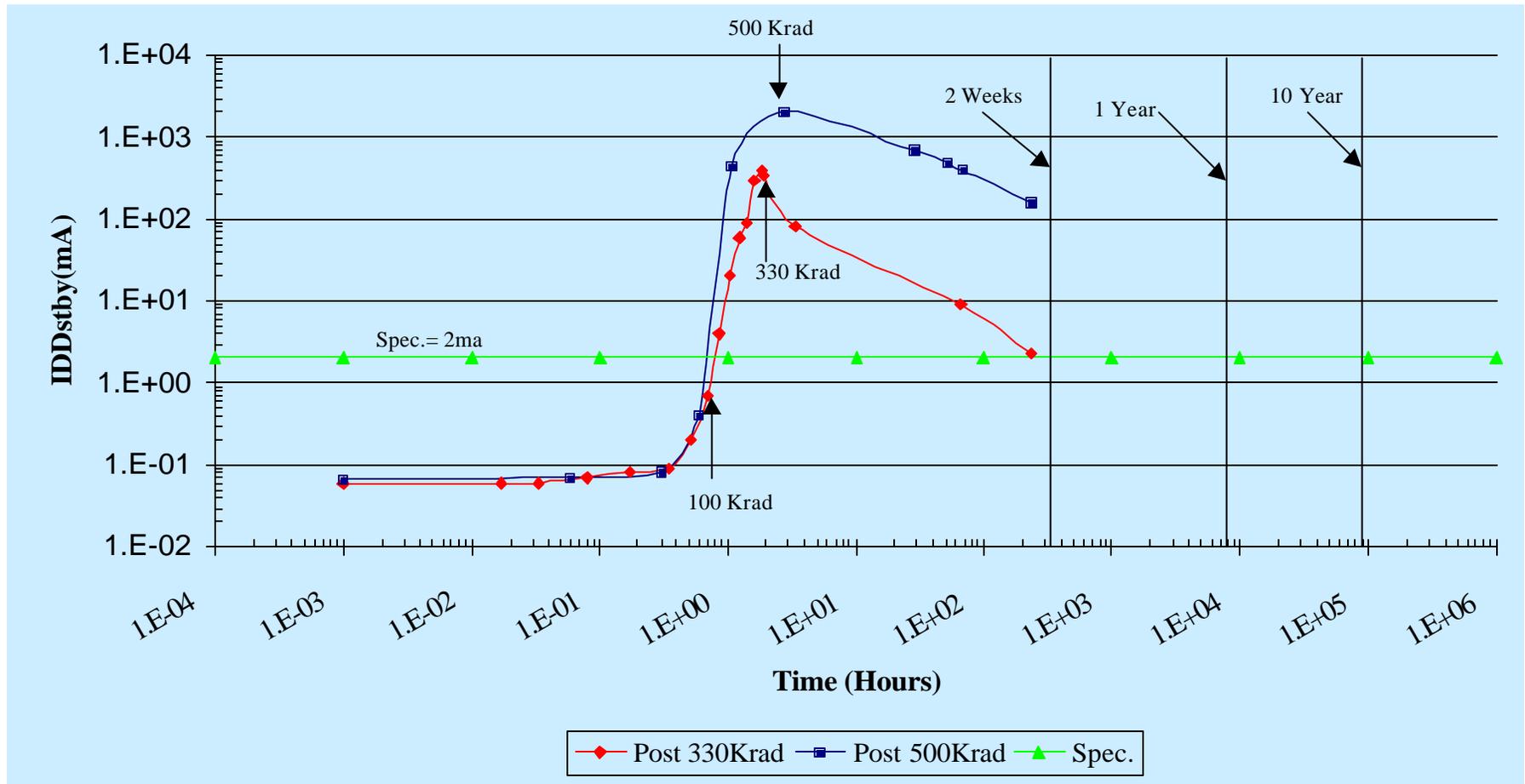
4M SRAM - Rad Hard and Commercial Foundries



SER < 1E-12 Upset/Bit/Day (Rad Hard Foundry) / No Latch-up

SER < 1E-10 Upset/Bit/Day (Commercial Foundry) / No Latch-Up

R25 4M SRAM (Commercial Foundry B) Total Dose Radiation Response



Dose Rate = 50 rad(Si)/s. Anneal is at room temperature

Specification is supported after 140Krad(Si) @ 50rad(Si)/s,
330Krad(Si) @ 0.03rad(Si)/s, or 500Krad(Si) @ 0.001rad(Si)/s

Standard QML Screening Flows



<u>Screening Flow</u>	<u>QML Q / T</u>	<u>QML V</u>	<u>Comments</u>
Wafer Foundry	Radhard / Commercial	Radhard	
Wafer Lot Acceptance	✓	✓	Internal Procedure
Serialization	✓	✓	Die Traceability
Internal Visual	✓	✓	MIL-STD-883, TM 2010, Condition A
Temperature Cycle	✓	✓	MIL-STD-883, TM 1010, Condition C
Constant Acceleration	✓	✓	MIL-STD-883, TM 2001
Particle Impact Noise Detection (PIND)	✓	✓	MIL-STD-883, TM 2020, Condition A
Radiography	N/A	✓	MIL-STD-883, TM 2012
Electrical Test	✓	✓	Device specification
Dynamic Burn-In	160 hours	240 hours	MIL-STD-883, TM 1015
Static Burn-In	N/A	144 hours	MIL-STD-883, TM 1015
Final Electrical	✓	✓	Device specification (3 temp); Group A test
Percent Defective Allowable (PDA)	5% Functional	5% Overall, 3% Functional	Internal Procedure
Fine and Gross Leak	✓	✓	MIL-STD-883, TM 1014
External Visual	✓	✓	MIL-STD-883, TM 2009

Technology Reliability Failure Rate Database



Failure Rates are calculated from life test data.

(# fails) / (effective stress hours)

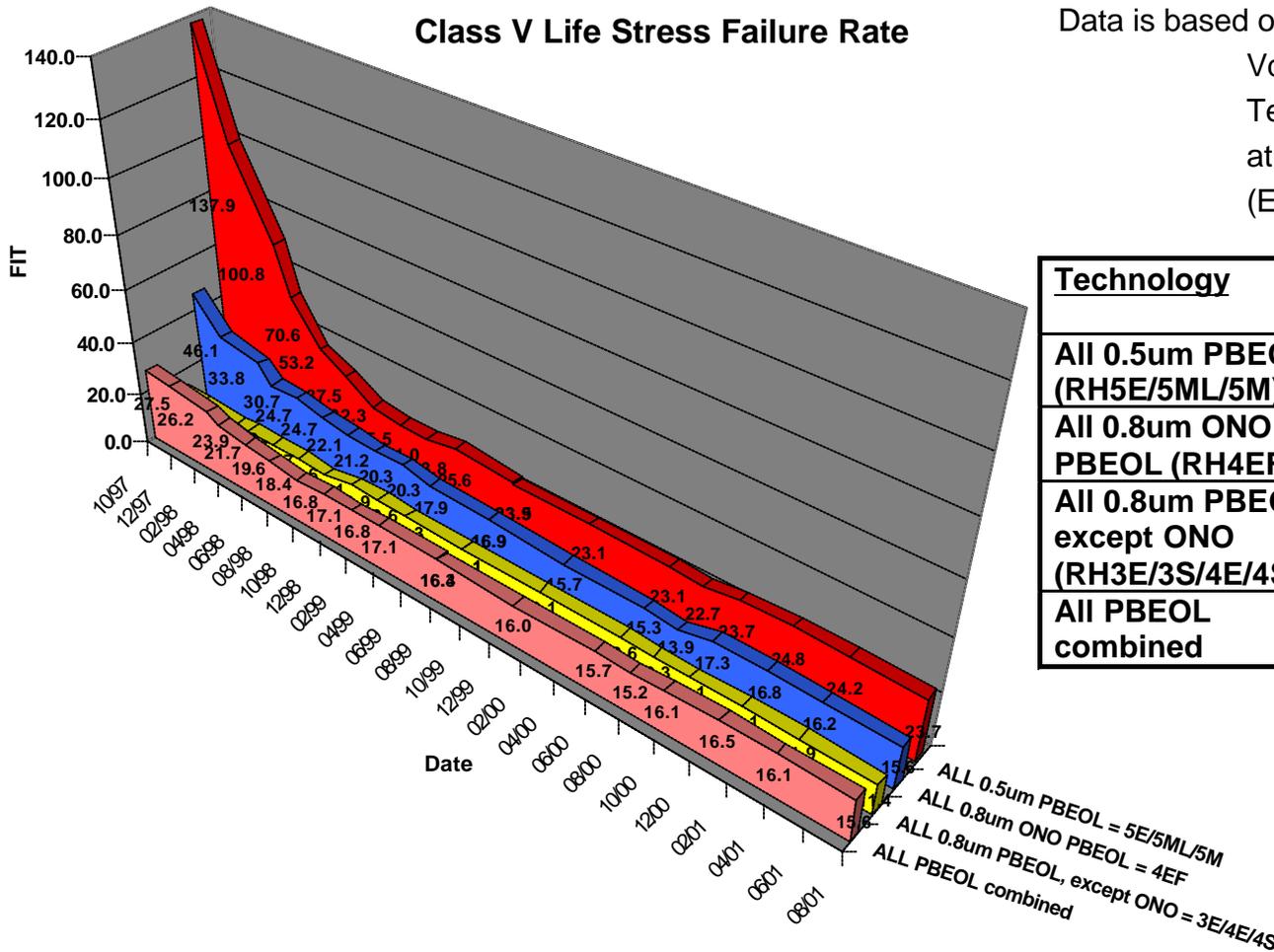
Data is based on Class V hardware with

Vdd = nominal voltage,

Temp = 60°C

at 60% Confidence Level

(Ea = 0.70, Beta = 2.5)



Technology	Class V FITs	Class Q FITs	# Devices / # Stress Hrs.
All 0.5um PBEOL (RH5E/5ML/5M)	23.7	32.8	1432 devices / 1.84M hours
All 0.8um ONO PBEOL (RH4EF)	15.6	29.3	1040 devices / 1.14M hours
All 0.8um PBEOL, except ONO (RH3E/3S/4E/4S)	11.4	21.8	2048 devices / 2.12M hours
All PBEOL combined	15.6	26.3	4520 devices / 5.09M hours

Commercial DRAM for Space

- Higher density drives interest in using DRAM
- Cassini and other programs have used Solid State Recorders made from DRAM
- DRAM suffers from susceptibility to SEU, latch-up, low TID response, stuck bits and multi-bit upsets
- General approach is:
 - Screen multiple vendor designs for latch-up
 - Use Error Detection and Correction (EDAC) and scrub entire memory often for stuck bits
 - Shield for total dose
- Still exposed to hazards of commercial world, however
 - Latch-up susceptibility varies by design implementation
 - Simple process change can effect radiation response significantly
 - No notification of process changes within part number or by date code
- Additional complication of DRAM is necessity of refresh
 - Adds overhead to system design
 - Requires constant interaction with external system

Commercial DRAM for Space

- **More advanced DRAM, i.e., SDRAM, attractive but have new problems due to complexity**
 - High density, pipelined for fast throughput
 - SEU on control circuits may cause block errors of 128, 512 or 1024 when active bank information is lost
 - Mode register upset dumps entire RAM
 - CAS latency, Block length set during initialization
 - Data may survive in cells but is irretrievable in coherent form
 - Re-initialization sequence required to recover from upset
 - Refresh can be even more complicated, requiring 4096 processor commands per 64mS operation
 - Still have underlying DRAM characteristics for stuck bits, multi-bit errors, latch-up
- **Due to vendor variability and duplication of effort in screening multiple vendors and multiple date codes the cost to qualify a single DRAM/SDRAM lot date code can be very high**

Heavy ion testing of commercial SDRAMs

	Vendor	LET Threshold (MeV/mg/cm ²)	Error Types
<ul style="list-style-type: none"> 64Mbit Synchronous Dynamic Random Access Memory (SDRAM) Multiple vendors Tests performed at Brookhaven and Berkeley Labs 	B	≤ 75	<ul style="list-style-type: none"> Destructive Latchup No SEU Characterization due to destructive latchup.
<p>(1) Control circuit could have been hit to cause address re-map. Error occurred in 1024 bit jumps</p> <p>(2) Single Event Functional Interrupt. Mode register appears to have been hit causing loss of functionality until device is reset.</p>	D	2.0 – 4.0 6.0 – 7.0 59.0 – 60.0	<ul style="list-style-type: none"> Multi-bit SEU/Stuck Bits SEFI (2) Non-destructive Latchup
	E	1.5 – 5.5 7.0 ≥ 87.0	<ul style="list-style-type: none"> Multi & Single SEU / Stuck Bits SEFI (1)(2) No Latchup observed through 87.0
	F	≤ 75	<ul style="list-style-type: none"> Non-destructive Latchup No SEU Characterization Performed.
	G	1.5 – 3.0 5.0 – 10.0 60.0 – 75.0	<ul style="list-style-type: none"> Single Bit SEU/Stuck Bits SEFI (2) Non-destructive Latchup

Most contemporary SDRAMs display high sensitivity to latch-up and SEU errors, creating challenge for use in space

64M SDRAM Upset Rates



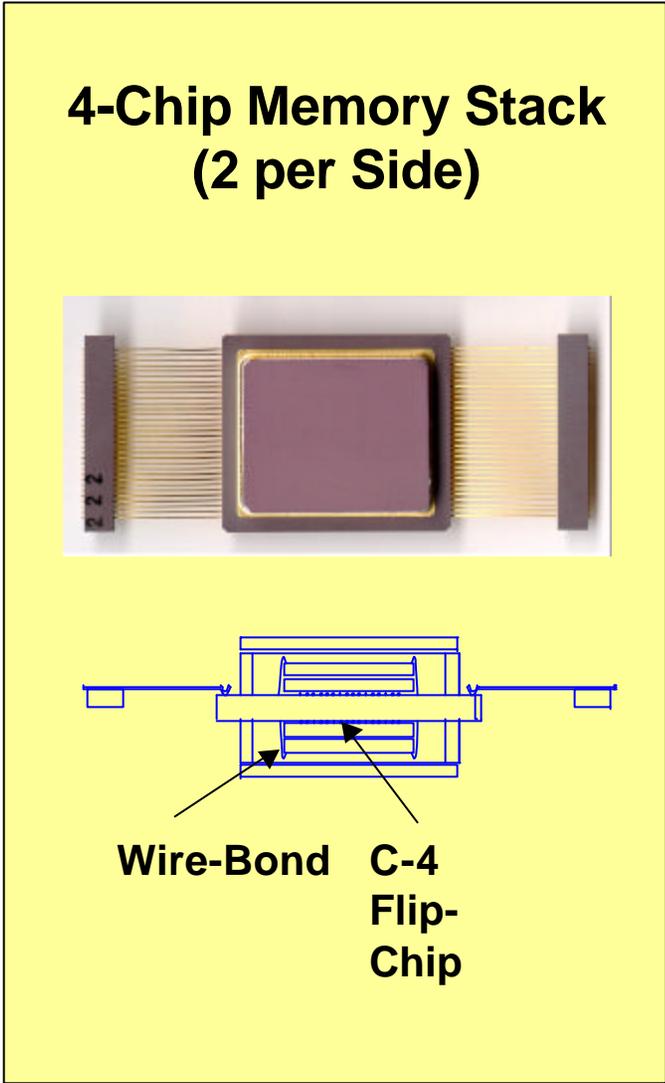
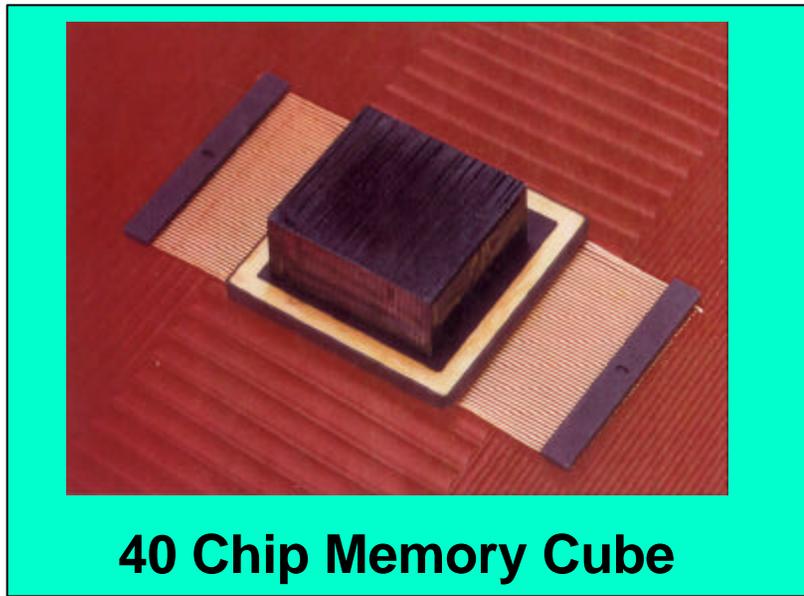
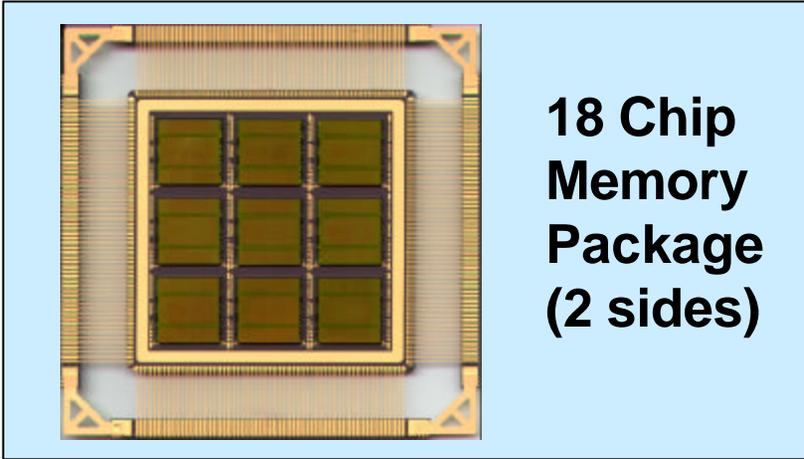
		Cell upset	Multi-bit	Stuck Bit	SEFI
35000 Km, 90% worst case Geo.		1E-9 u/cell-day	5.6E-3 u/device-day	2.4E-13 u/bit-day	6.0E-4 u/device-day
1400 Km, 52 degrees (Hi Leo)		6.1E-11 u/cell-day	7.5E-4 u/device-day	1.4E-14 u/bit-day	1.2E-4 u/device-day
500 Km, 28 degrees (Low Leo)		5.6E-14 u/cell-day	1.2E-4 u/device-day	2.9E-17 u/bit-day	2.4E-5 u/device-day

SDRAM Limited System Availability

Example Case	Array Availability
GEO	0.9748
Hi LEO	0.9996
Low LEO	0.9999

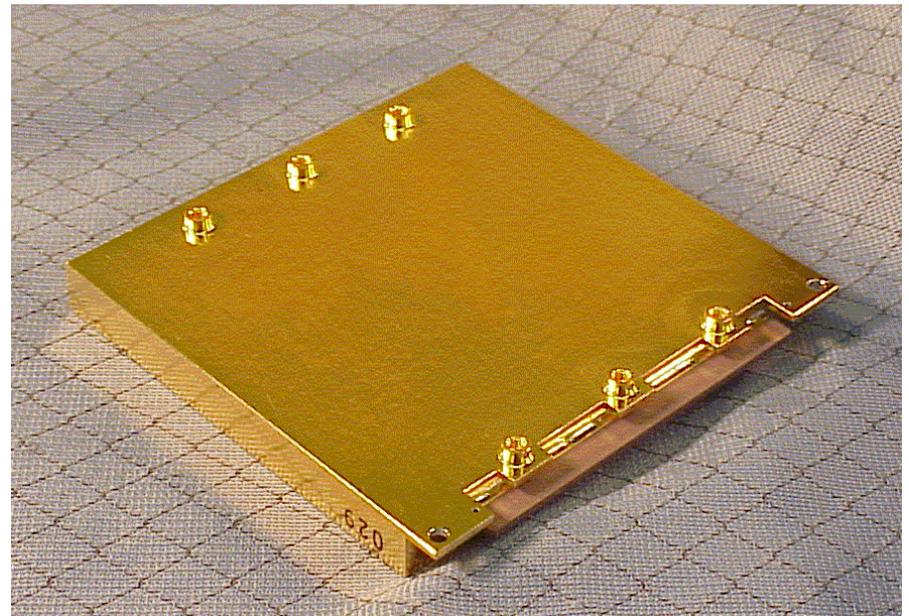
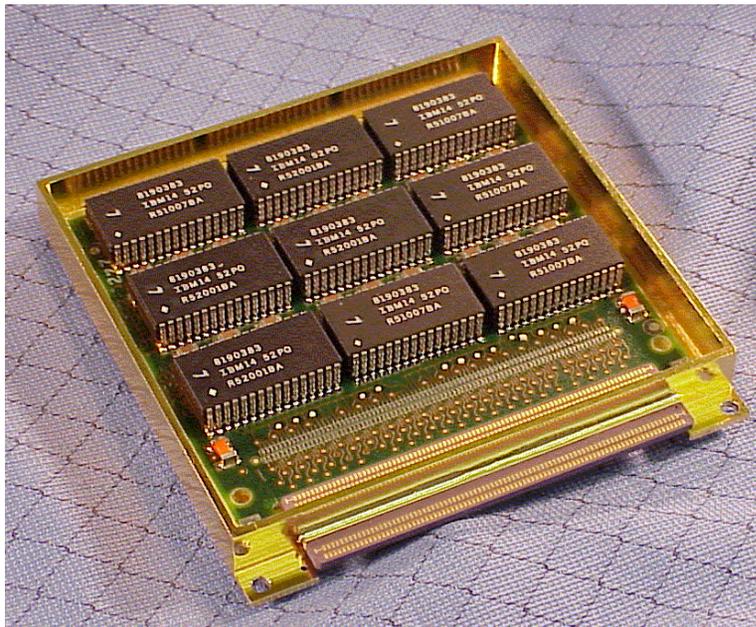
- 10 year mission
- 128 Mbyte array with EDAC
- Scrub array every 24 hours
- Reload Mode register every 12 hours

Multi-Chip Memory Packaging for Space

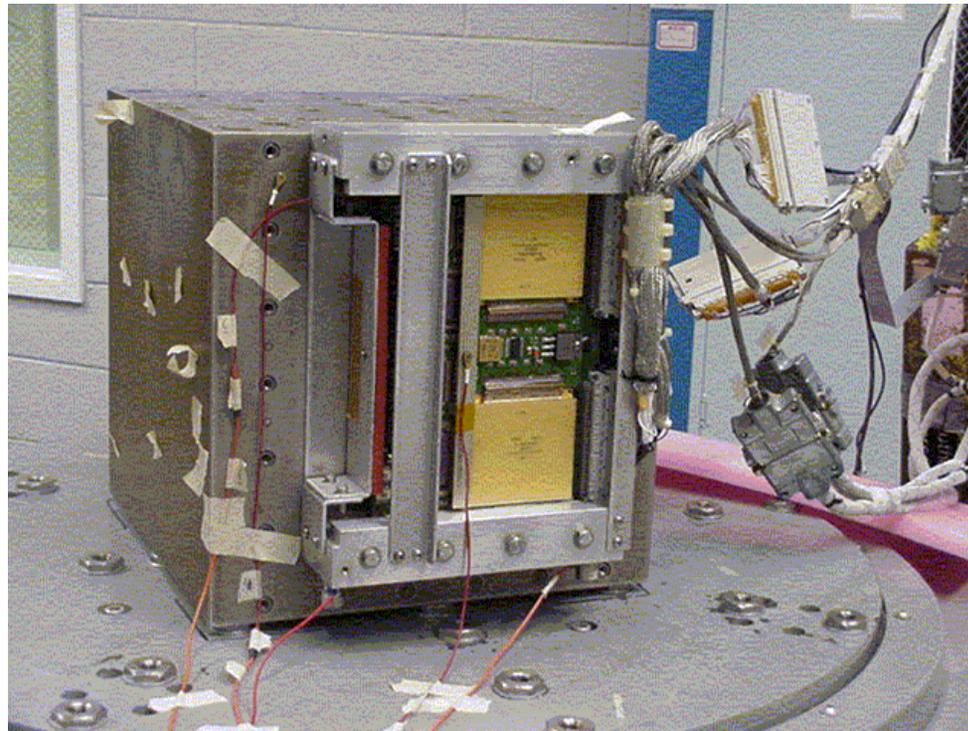


Stacked Memory TSOPs on a Hermetic Memory Card (HMC)

BAE SYSTEMS



Vibration Testing of the HMC



X-axis		Y-axis		Z-axis	
20 to 70 Hz	+6dB/oct	20 to 70 Hz	+6dB/oct	20 to 70 Hz	+6dB/oct
70 to 700 Hz	0.29g ² /Hz	70 to 270 Hz	0.61g ² /Hz	70 to 700 Hz	0.45g ² /Hz
700 to 2000 Hz	-8dB/oct	270 to 400 Hz	-6dB/oct	700 to 2000 Hz	-8dB/oct
		400 to 1000 Hz	0.28g ² /Hz		
		1000 to 2000Hz	-8dB/oct		
Overall	16.9 grms	Overall	21.7 grms	Overall	21.2 grms

C-RAM Phase Change Technology

Currently no one memory technology meets all needs but C-RAM is very attractive

	<i>Speed</i>	<i>Power</i>	<i>Cost</i>	<i>Cycle Life</i>	<i>Non-Volatile</i>
SRAM	Very High	High	High	Very High	No
DRAM	High	Med.	Very Low	Very High	No
FLASH	Low	Very Low	Low	Low	Yes
C-RAM	High	Low	Very Low	High	Yes

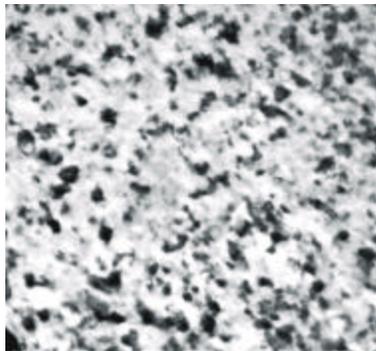
C-RAM Phase Change Technology



- Chalcogenides: alloys with at least one Group VI element
 - C-RAM uses a Ge-Sb-Te alloy
 - Can exist in either of two stable states
 - CD and DVD technology uses reflectance change
 - C-RAM memory uses electrical resistance change
 - Chalcogenide material is radiation immune, devices are as hard as base technology

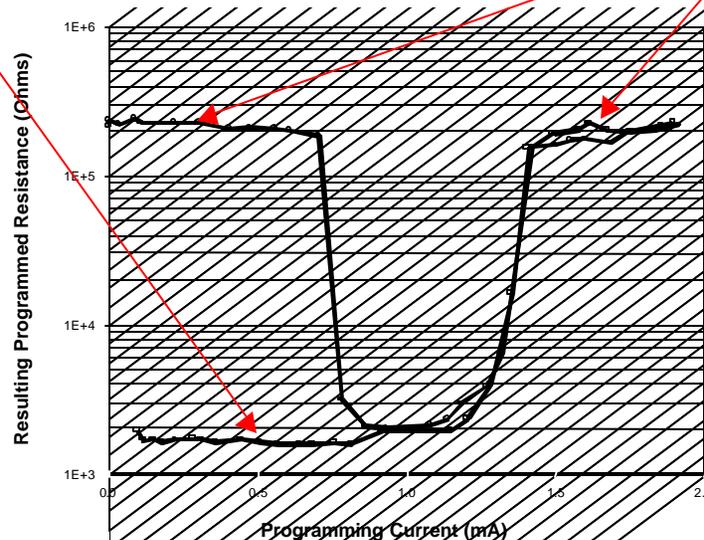
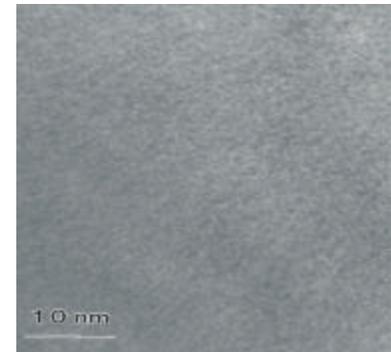
Polycrystalline State

High reflectance & conductance

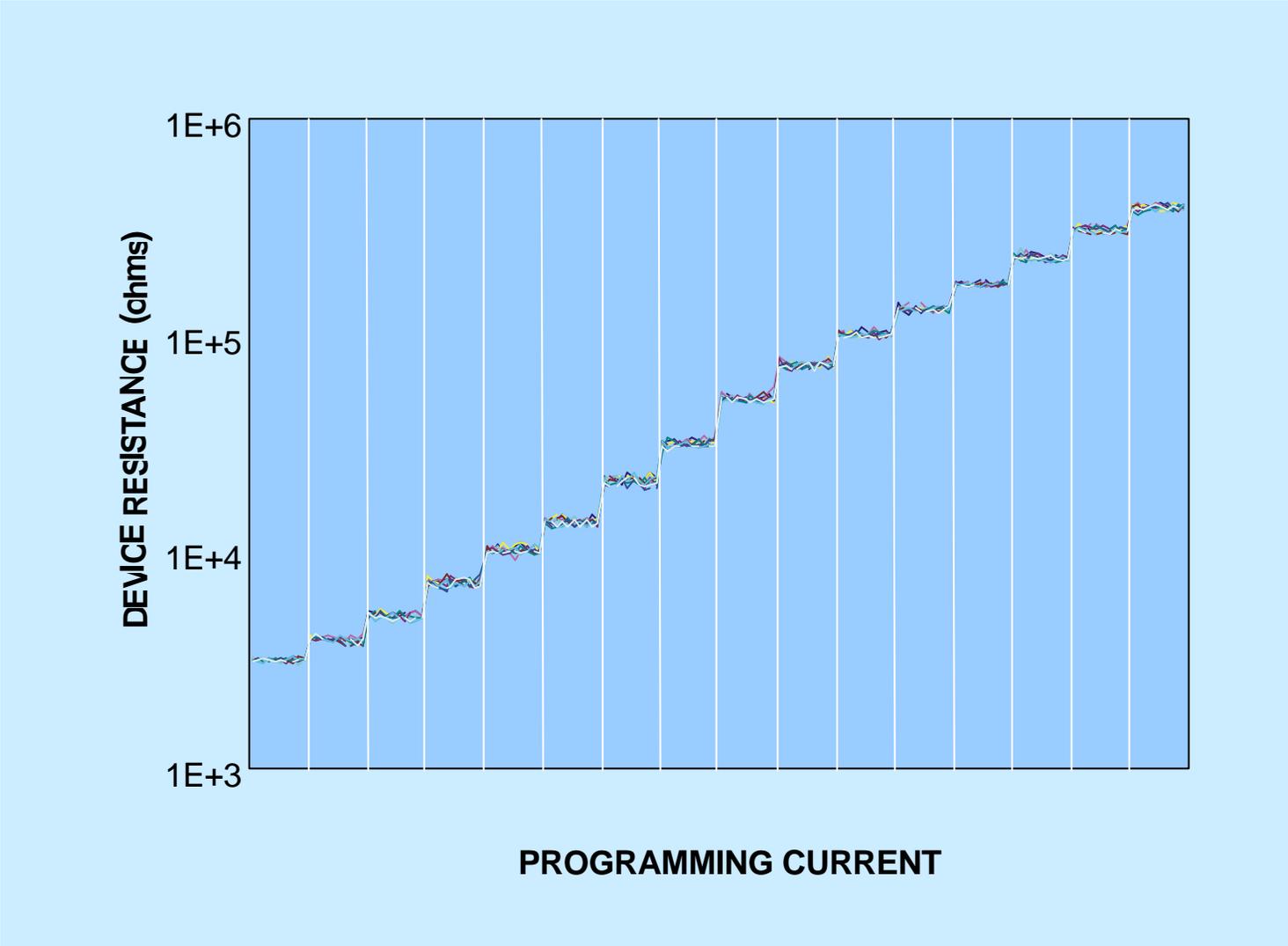


Amorphous State

Low reflectance & conductance

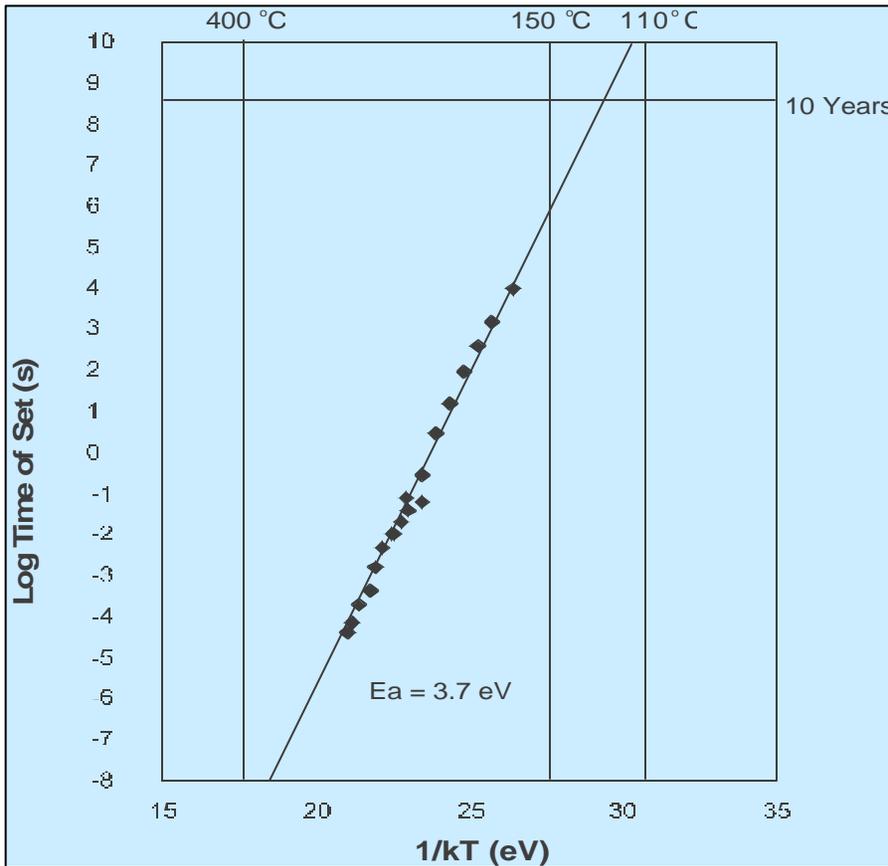


Multiple Storage State Capability of C-RAM Device

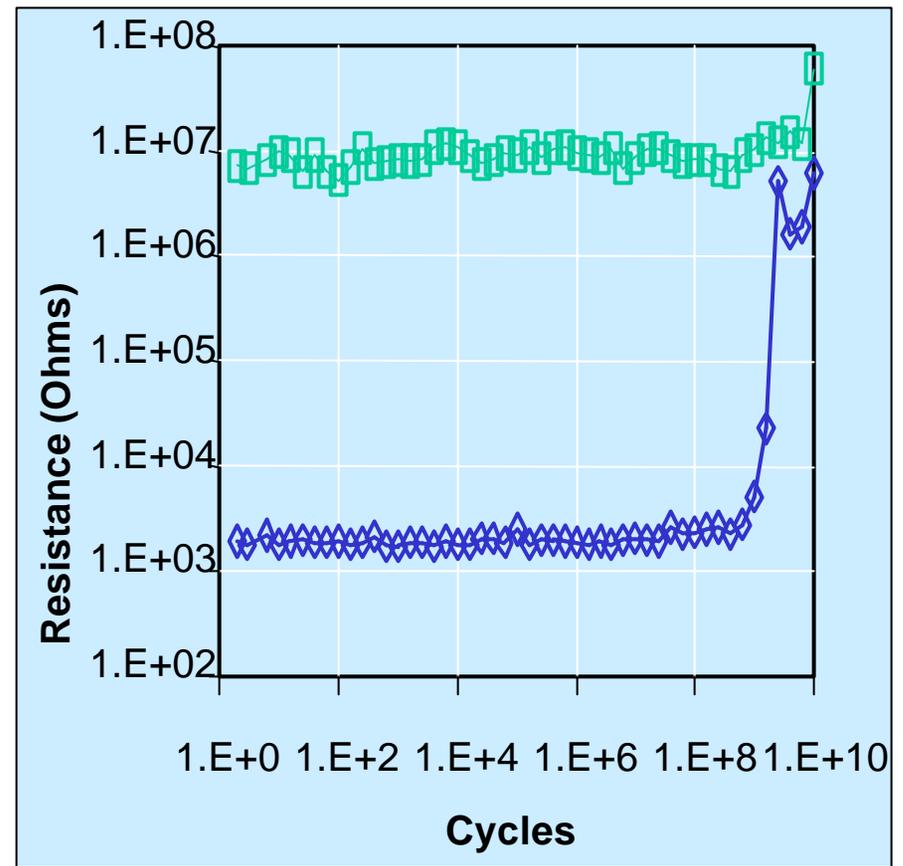


Present Reliability of C-RAM Memories

Data Retention



Cycle Endurance



Status of C-RAM program

- **AFRL sponsored research program with Ovonyx at BAE SYSTEMS, Manassas to develop technology**
 - **Single cell memories have been demonstrated**
 - **Integration into RH CMOS process underway**
 - **Two test chips being designed/fabricated**
 - **Productization phase 2002-2003**
 - **Target 4M-16M NV RAM**
 - **speed near SRAM**
 - **density near DRAM**
 - **endurance better than EEPROM / Flash**
 - **low power**
 - **low cost**

Conclusion

As space system complexity increases the demand for high density, high performance memory grows

Current solutions include QML qualified Rad Hard SRAMs, commercial SRAM and DRAM systems with various screening levels and advanced packaging to improve radiation tolerance and increase board density

SDRAMs offer high density and high performance, but suffer from new failure modes that limit their usefulness in space

A future memory, C-RAM, is coming on-line that will simplify space system designs, and will share the quality, reliability and radiation characteristics of its integrated base technology