Radiation Test Report, Single Event Effects, Virtex-5QV Field Programmable Gate Array, Multi-Gigabit Transceivers

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1. SCOPE

This document describes the execution and results of the investigative effort to characterize the Single Event Effect (SEE) symptoms that are experienced by the multi-gigabit transceivers (MGT) embedded in the Virtex-5QV Xilinx Field Programmable Gate Array (FPGA).

2. REPORT SUMMARY

Device Tested	Viretx-5QV FX-130 Prototype; s/n's A4464, A4438 and A4421.
SEE Test	MGT Characterization, Basic Functions, MGT isolation with Ion Mask
Radiation Type	15, 25-MeV/amu Heavy Ions (TAMU) 16-MeV/nuc Heavy Ions (LBNL)
Test Facilities:	Texas A&M K500 Cyclotron, College Station, TX (TAMU) Lawrence-Berkeley NL 88" Cyclotron, Berkeley, CA (LBNL)
Exploratory Test Dates	November 2009 (TAMU), December 2009 (LBNL), January 2010 (LBNL), March 2010 (TAMU)
Characterization Test Dates	May and August 2010 (TAMU)
Principal Investigator	Roberto Monreal (Southwest Research Institute)
XRTC Participation	S.A. Anderson, M. Coe, P. Rutt, (SEAKR Engineering); D. Lee (Sandia NL), G. Madias (Boeing Space Systems), G. Allen (JPL)

The Single Event Effect (SEE) characterization testing performed on the Multi-Gigabit Transceiver elements of the Xilinx Virtex-5QV Prototype showed a variety of symptoms which have been measured, analyzed and classified. Events were classified into two main types, Bit-Error (BE) and Loss-of-Link (LOL) events. Bit Errors are the events where a corruptive effect with immediate self-recovery occurs on a synchronized MGT channel, resulting in only a handful of corrupted bits of the transmitted data per each event. Loss-of-Link events, on the other hand, are events that require some type of user interaction, typically a channel resynchronization or re-initialization procedure, for the communication channel to resume functionality. The resynchronization and re-initialization process can be sourced periodically or automatically upon detection from either the governing serial-link protocol (i.e. Aurora, Rapid I/O, PCIe) or from a capable custom link monitoring mechanism built into the FPGA design. The investigation also demonstrates that LOL events can simultaneously affect multiple MGT channels found in each MGT tile; and in some cases, also simultaneously affect one or more channels in groups of MGT tiles in the same column of the device. Other much less frequent recovery activities required were GTX Tile Resets, GTX Tile Dynamic Reconfiguration Port (DRP) bit-value scrubbing, and re-initialization of the downstream interface MGT devices. Occurrence rates due to heavy-ions in a Geo-synchronous orbit have been calculated for each of these events, and they are shown in Table 1. First order system analysis shows that with communication protocols that posses data delivery verification capability and basic channel LOL monitoring and recovery schemes, the effects of SEEs on MGTs can be effectively transparent.

Table 1. Event Rate Summary (Source: CRÈME-MC, Geosynchronous Orbit, nominal conditions, with a 0.150" thick Aluminum enclosure).

EVENT TYPE		UNITS	EVENT RATE (/DAY)	DAYS	YEARS
TX BE		/CHANNEL	2.13E-04	4,684	12.8
RX BE		/CHANNEL	5.58E-04	1,790	4.9
TX LOL :	TOTAL	/CHANNEL	6.03E-05	16,581	45.4
	RESYNC	/CHANNEL	5.47E-05	18,297	50.1
	RE-INIT	/CHANNEL	6.21E-06	161,031	441.2
RX LOL :	TOTAL	/CHANNEL	1.19E-04	8,402	23.0
	RESYNC	/CHANNEL	1.14E-04	8,774	24.0
	LONG RESYNC	/CHANNEL	2.77E-06	361,406	990.2
	TOTAL REINIT	/CHANNEL	1.20E-05	83,018	227.4
RX REINIT LOL :	RX BUFFER RESET	/CHANNEL	4.38E-06	228,487	626.0
	RX RESET	/CHANNEL	9.42E-07	1,061,828	2,909.1
	RX CDR RESET	/CHANNEL	8.43E-08	11,862,579	32,500.2
TILE LOL:	GTX TILE RESET	/CHANNEL	2.10E-06	476,349	1,305.1
	DRP SCRUB	/CHANNEL	6.82E-09	146,545,483	401,494.5
MULTIPLE MGT:	SINGLE TX	/TILE	3.69E-05	27,125	74.3
	SINGLE RX	/TILE	1.80E-04	5,548	15.2
	MULTI-ELEMENT	/TILE	2.42E-05	41,346	113.3
	MULTI-TILE	/TILE	2.84E-08	35,221,313	96,496.7

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4. ACRONYMS AND DEFINITIONS

ADC, A/D	Analog-to-Digital Converter.
BiE	Bits in Error; total number of bits in error.
BE	Bit-Error; most benign but also most probable SEE of MGTs.
BER	Bit-Error Rate; ratio of erroneous bits vs. non-corrupted bits.
CCSDS	Consultative Committee for Space Data Systems; space industry packetizing standard.
ConfigMon	Configuration Monitor, part of the generic Xilinx test vehicle.
CDR	Clock-Data-Recovery; MGT technological feature used to extract clock from incoming serial signal.
CML	Current-Mode Logic; digital logic signaling standard
DCM	Digital Clock Manager; FPGA Macro found in Virtex FPGA devices.
DRP	Dynamic Reconfiguration Port, architectural feature of the Virtex FGA MGT and DCM primitives.
FIFO	First-In, First-Out, semiconductor memory device access-type.
FPGA	Field-Programmable Gate Array.
FuncMon	Functional Monitor FPGA, part of the generic Xilinx test vehicle.
FX-1	Viretx-5QV Prototype.
GLUT Mask	Generic Look-Up Table mask
GND	Ground (electrical potential)
GUI	Graphical User Interface.
GTX	Gigabit-Transceiver; name of MGT hardware macro for the Virtex-5QV device.
GTX-Dual	MGT macro designation.
JTAG	Standard test Access port and boundary-scan architecture that is named after the Joint Test Action Group (JTAG) who defined it.
K-SYNC	8B/10B “K” character for synchronization of communication links.
LBNL	Lawrence-Berkeley National Laboratory.
LET	Linear Energy Transfer; always in units of MeV·mg/cm^2 unless otherwise noted.
LOL	Loss-Of Link in serial communication link; the channel is unresponsive until action is taken.
LOS	Loss-of-Synchronization; term used to define when a communication link is not synchronized.
LUT	Look-Up Table; logic function implementation in the FPGA configuration block.
LVU	Link Verification Unit
MEU	Multiple Element Upset
MTU	Multiple Tile Upset

MGT	Multi-Gigabit Transceiver.
MICTOR	Matched-Impedance ConnecTORs.
PCB	Printed Circuit Board.
PLL	Phase-Lock Loop; FPGA Macro found in Virtex devices.
PCI	Peripheral Computer Interface; internal computer parallel standard.
PCIe	Peripheral Computer Interface Express; internal computer communication bus based on MGT-like communication links.
PCS	Physical-Coding Sub-Layer; aspect of the MGT system that exchanges data to and from the PMA and FPGA fabric.
PMA	Physical Media Attachment; the portion of the MGT that interface to the physical media
PPC	Power Processing Computer.
PRBS	Pseudo-Random Bit Sequence; standard test pattern used in the serial-communications applications.
PROG	Re-program pin of the configuration controller in the Virtex FPGA devices.
PROM	Programmable Read-Only Memory.
Rapid I/O	Rapid Input/output; serial communication standard for MGT-like communication links
ReInit	Re-initialization.
ReSync	Resynchronization.
RS-232	Recommended Standard 232, a serial telecommunications standard.
RX	Receiver.
SATA	Serial Advanced Technology Attachment; serial communication standard for MGT-like communication links
SEE	Single-Event Effects.
SEFI	Single Event Functional Interrupt.
SMA	SubMiniature version A) RF co-axial connectors
SMPX	Another name for SubMiniature version B) RF co-axial connectors (SMB)
SRV	Service FPGA
SW	Software.
SwRI	Southwest Research Institute.
SysMon	Internal macro in the Virtex-5 FPGAs used mostly for analog house-keeping functions.
TAMU	Texas A&M University.
Tile	Common reference to Xilinx GTX macro.
TX	Transmitters.
UART	Universal Asynchronous Receiver/Transmitter, telecommunications protocol.
XCLK	Internal MGT clock, used in the PCS.
XRTC	Xilinx Radiation Test Consortium.

5. TECHNICAL BACKGROUND

5.1 Introduction

Multi-Gigabit Transceivers (MGT) are semiconductor integrated circuits embedded in the FPGA that are devised to be high-speed digital data transmitter and receivers (i.e. transceivers); the collection of integrated circuits that constitute the MGT and provide it's functions are referred to as a MGT Tile. MGTs tiles that are embedded in the Xilinx Virtex-5 FPGAs, are referred to as GTX Tiles or Giga-bit transceivers Tiles. MGTs are also found in the previous generations of Xilinx Virtex FPGAs (Virtex-2 Pro and Virtex-4), as well as in FPGAs by other manufacturers (Altera Inc., Lattice Semiconductor). The MGTs studied in this work are the GTX Tiles of the Xilinx Virtex-5QV (V5QV) FPGA, which also feature radiation hardened configuration cells, thus making MGTs available for FPGA designs that are intended for space applications. Figure 5-1 shows a plot of the maximum data rate and the parallel clock frequency that some common communication standards have. For comparisons sake, the 64-bit PCI and 32-bit VME bus parallel standards aggregate data rate are also plotted.

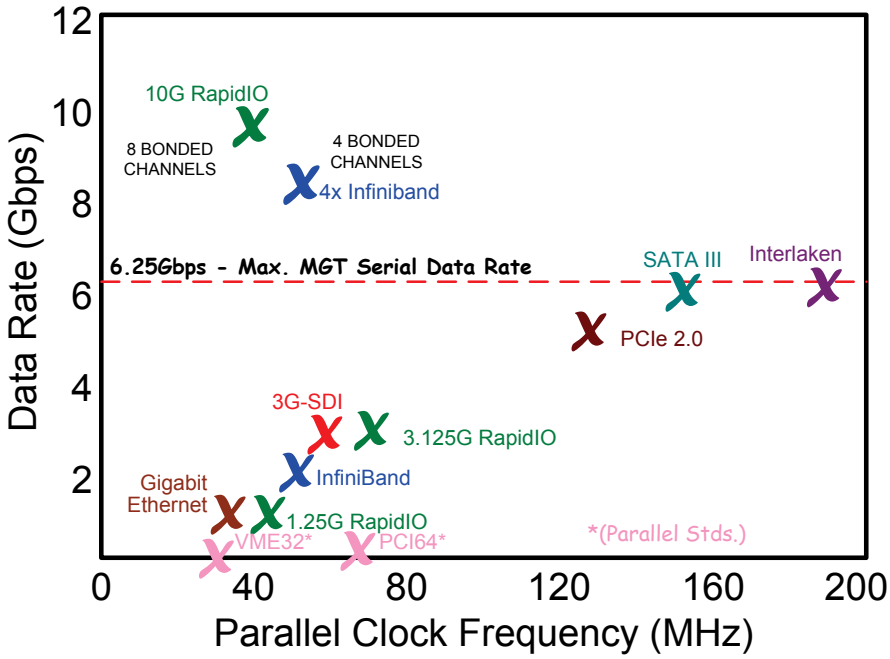

Figure 5-1. Data Rate vs. Parallel Clock Frequency for some of the Serial Communication Standards.

The V5QV GTX MGTs are physically capable of providing high-speed serial interfaces in excess of 6 Giga-bits per second (Gbps) for each individual channel, and 10Gbps or more for bonded channels. This embedded serial interface capability that MGTs provide FPGAs is extremely attractive to systems designers and has been used assiduously in commercial systems. MGTs are the choice physical devices for the implementation of serial communication interfaces for data that must be exchanged between devices, across backplanes, or in between systems. Thus they are used in numerous common communication standards, such as PCI-Express, Fibre-Chanel, Infiniband, 10G and Giga-bit Ethernet, SATA, Aurora, just to a name a few. For space system applications, designers need to understand the effects that the ionizing particles encountered in space by the space-craft will have on their functionality in order to mitigate these negative effects. This alleviation is essential so the system can maintain the highest level of assurance and fidelity, while still offering the high performance of an MGT-driven

communication interface. It is the intention of this research to provide the designer with such characterization details.

5.1.1 MGT Description

Fundamentally, MGTs consist of 1) a transmitting (TX) or serializing element; 2) a receiving (RX) or de-serializing element; and 3), a phase-lock loop (PLL) element that provides the serial rate and sampling digital clock. TX elements are made up of parallel-to-serial circuitry with sophisticated encoding and synchronizing capabilities that feed a current-mode logic (CML) differential driver. The RX element consists of a CML differential receiver which feeds serial-to-parallel conversion circuitry which also provides equally sophisticated decoding and synchronizing capabilities. Figure 5-2 shows a diagram of the MGT primitive instance available in the Xilinx Virtex-5 FPGA GTX Tile, where the three main partitions can be seen, i.e. TX, RX and the shared resources; as well as the dual transceiver (RX and TX) capability, hence the given name 'GTX Dual'.

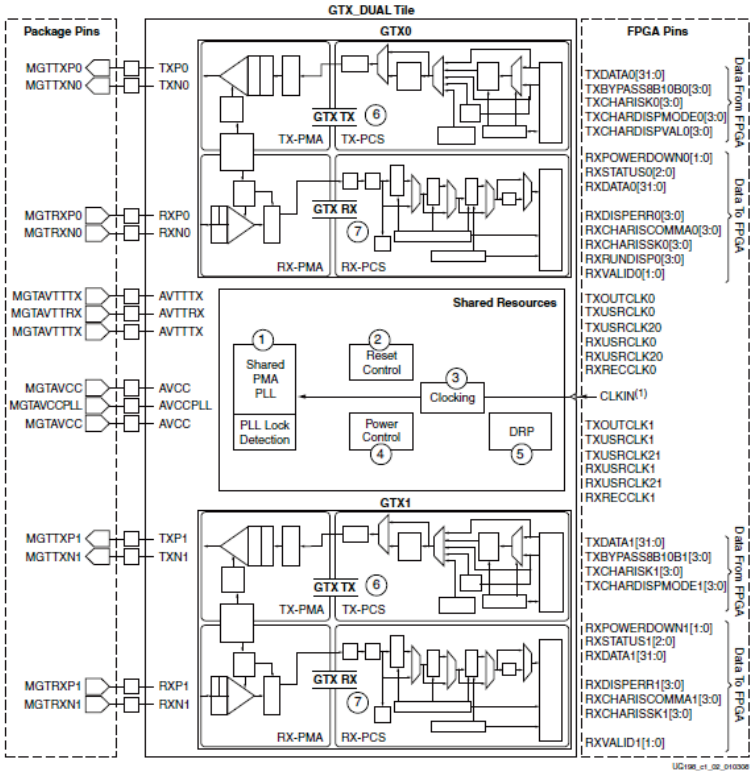

Figure 5-2. Virtex-5 GTX Tile, with shared resources (1-5), TX elements (6) and RX elements (7).

5.1.1.1 MGT Configuration

The MGTs are configured in the FPGA with multiple settings available to the user; some of the settings involve the basic functionality aspects of the MGT, such as analog settings, line rate, internal clock speed, clock source and internal parallel data width; while others are very specific to particular applications, such as control character definitions, self-test capabilities, etc. One of the more advanced features of the MGT implementation in the Virtex-5 FPGA fabric is the availability of a Dynamic Reconfiguration Port (DRP), which allows the user to reconfigure the MGT through a serial port that is built in to the MGT tile. The DRP configuration settings allow the user to dynamically alter the MGT configuration aspects independently of the main device configuration engine. This provides the MGT users with an ability to

completely change the communication specifications, (i.e. communication protocol) without having to reconfigure the device. This DRP port interface is also present in the Digital Clock Managers (DCM) and Phase-Lock Loops (PLL), which are also available in the Virtex-5 FPGA.

5.1.1.2 MGT Power

A very critical aspect of the MGTs is the method of supplying power. The voltage levels required by the MGTs have to be very stable over the range of electrical current they require to operate. Noisy power supplies can be very detrimental to their operation (1), and for this reason the Virtex-5 devices provide separate power inputs for each GTX tile, and for specific aspects of the MGT. Table 2 lists the different supplies, the voltage level, and required tolerance as specified by Xilinx.

Table 2. Virtex-5 GTX Tile Voltage Supplies.

MGT Supply	Description	Voltage (VDC)	Tolerance (%)	Max. Current (mA)
MGTAVCCPLL	Analog supply voltage for the GTX_DUAL shared PLL relative to GND	1.00	5	99.4
MGTAVTTTX	Analog supply voltage for the GTX_DUAL transmitters relative to GND	1.25	5	86.3
MGTAVTTRX	Analog supply voltage for the GTX_DUAL receivers relative to GND	1.25	5	56.5
MGTAVCC	Analog supply voltage for the GTX_DUAL common circuits relative to GND	1.00	5	179.5
MGTAVTTRXC	Analog supply voltage for the resistor calibration circuit of the GTX_DUAL column	1.25	5	0.5

5.1.1.3 MGT Digital Clocking

One of the more important aspects that permit MGT and like devices with the capability to transmit and receive high data band-width volumes reliably is a stable, high-quality, low-jitter clock reference. To achieve this, each of the Virtex-5QV MGT Tiles has been devised with their own clock differential input IO and differential clock buffer, which feeds the internal Phase-lock loop (PLL) of each tile. The PLL clock is used to drive the Gigabit rates of the MGTs. Each tiles MGT clock reference can be forwarded to the FPGA fabric, as well as to adjacent tiles. The MGT tiles can also receive their operative clock reference from a regular fabric clock source, but the performance capabilities are significantly diminished.

5.1.2 MGT Technological Features

To overcome the physical difficulties of transmitting and receiving signals reliably in the GHz frequency domain, MGTs make use of a rich set of analog and digital technological features. MGT TX buffers employ pre-emphasis and de-emphasis to limit high-frequency signal loss and the MGT TX parallel portion can use digital encoding, such as 8B/10B, to provide transition-rich signals. MGT RX functions use receiving amplifier equalization and programmable termination impedance to overcome high-frequency loss and to ensure signal integrity. Digitally speaking, the MGT RX functions use clock data recovery (CDR) to extract a clock that is aligned to the incoming data stream transitions, RX functions can be configured to align the incoming serial pattern to a specified parallel position by making use of alignment characters, and RX functions also have the capability of executing clock-correction operations to overcome clock difference between the CDR extracted clock, and the host FPGA's sampling clock. Multiple MGT tiles can have their TX and RX elements configured in concert to operate in channel bonding mode, where multiple MGT connections create a single higher throughput channel. Special

alignment characters are used by the MGT RX function to de-skew each MGT channel that is bonded. This is one of the more attractive features of the Xilinx MGTs, where common standards such as PCI Express, XAUI and others have been specified to make use of this feature. The band-width power of channel bonding is evident in the scatter plot shown by Figure 5-1 on page 12.

5.1.3 MGT Functional Characteristics

In serial communication links that send and receiving digital data, the receiver elements are required to be synchronized to the transmitter elements periodically and often. This is due because if the receiving side swallows or duplicates a single bit of the serial data stream, all of the following bits from that point on in that stream will be erroneous. With single-channel serial rates specified up to 6.125Gbps (Aurora), where the value of each bit is evaluated in a time window in the order of picoseconds, the probability of sampling bit values incorrectly is very high, even for robust systems operating in benign environments. Thus to implement useful serial communications channels, the link must be able to handle occasional errors with very little interruption. For this reason, serial communications data streams employ framed or packet data, where the actual digital information being communicated is contained within frames, providing opportunities in between the framed data (or packets) of performing synchronization tasks. Other tasks are also performed during the gaps between data frames, which are called the inter-packet-gaps. Common inter-packet-gap tasks are channel de-skewing and clock correction. Packetized data (or frame data) is the essential building block in all digital communications, of high and moderate speeds, allowing for the implementation of error detection capabilities, network addressing capabilities and control functions into the packet or frame structure. Packets have various sizes depending on the application; for example, the Consultative Committee for Space Data Systems (CCSDS) has defined a packetized data standard to use for deep-space communications, with variable “data packet” sizes of up to 64k bytes, made up of fixed 2k byte “frames”, which include a frame header and control information. Data packets are a very important aspect of the nature of MGT communications, since it provides a natural solution to detect data errors and recover from single event effects in space.

5.2 Existing MGT SEE Data

At the time of this report, several groups had provided some data on MGTs prior to this study. The results of their work served to identify the testing parameters and variables for the work described in this report. In 2004 Petrick et.al from NASA-GSFC obtained the first bit-error cross-sections on MGTs of the Virtex-II Pro. In their work they utilized masking techniques to isolate the fabric portion of the design so only the MGTs were exposed to the test ions. (2) In 2006, the author of this report also performed tests with Virtex-II Pro MGTs, were the existence and separation of self-recovered effects and effects requiring re-synchronization were first demonstrated. (3) In 2008, K. Morgan, et al. from Los Alamos tested a customized dual-redundant MGT-Aurora protocol in a commercial Virtex-5 device with alpha-particles, and demonstrated the viability of MGT links for space. Shielding used in this experiment also demonstrated that the actual MGT devices of the Virtex-5 provided a very small portion of the upsets detected in the Aurora system compared to the susceptibility of the fabric logic. (4) And in 2010, Hiemstra, et al. showed that the RapidIO protocol was also viable by exposing a Virtex-5 commercial FPGA to protons. (5)

6. TEST DESCRIPTION

6.1 Methodology

The basic concept of the MGT SEE test undertaken consists primarily in measuring the amount of time the MGT communication channel is in error before correct communications are re-established again, and

what action, if any, is required to do so. The SEE test was also devised to observe the electrical current being consumed by the MGT devices in order to determine if they were susceptible to any type of high-current state caused by SEEs.

Based on the nature of the MGT transmit and receive mechanisms, two distinct basic types of single events can be expected; events with an almost instantaneous effect and sub-sequent self-recovery of the MGT channel; and events that result in the MGT function being upset in a way which requires some sort of user or protocol activity to fully recover the communication channel, which in theory could include any activity, all the way from basic link re-synchronization to a complete device re-configuration. All MGT SEEs can be categorized into these two types; the first type is referred to as a *Bit-Error* Event (BE), and the second type as a *Loss of Link* Event (LOL). It must be noted that in prior SEE testing of MGTs, LOL-like events are referred to as Loss-of-Sync (LOS) events (3); while for these tests, the designation Loss-of-Link (LOL) is utilized. LOL is considered a more accurate designation since LOS events imply that a simple re-synchronization action is simply required to recover the link, while LOL events encompass not only LOS events, but also refer to any other manifestations that require actions beyond re-synchronization to recover the MGT communication link.

6.1.1 MGT Isolation through Ion masking

To differentiate the SEEs incurred by the MGT structures, from the SEEs incurred in the supporting glue-logic instantiated in the FPGA fabric (i.e. CLBs and IO Buffers), a stain-less steel mask was designed and fabricated. XRTC member SEAKR Engineering provided the resources to fabricate the mask. The mask design took advantage of the layout of the MGTs in the device, which are arranged in a single column of GTX tiles on one of the edges of the device die, as is shown in Figure 6-3 on page 17. The stainless-steel mask was designed to only expose one half of the MGTs of the column, the top or bottom, providing shielded MGT transmitters and receivers for moving test data streams into and out of the DUT without ionizing interference during testing. Figure 6-1 illustrates how the masking of the top/bottom of the MGT column, together with interleaving of the MGTs, also provides a very efficient way of separating transmit and receive functions for each test channel. Figure 6-2 shows the mask in palace.

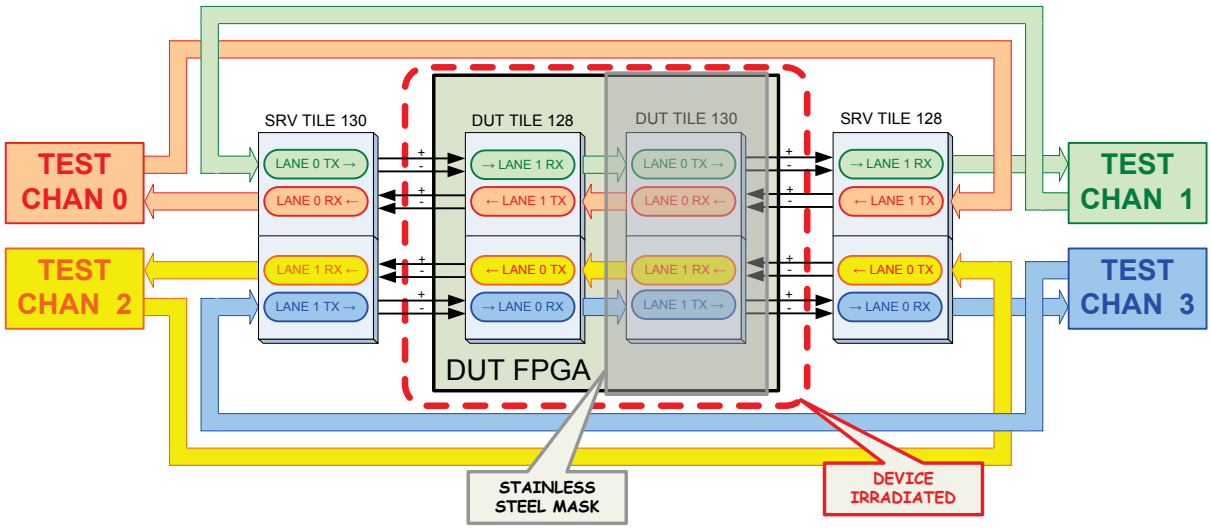

Figure 6-1. Interleaving of 4 Test Channels with stainless-steel mask.

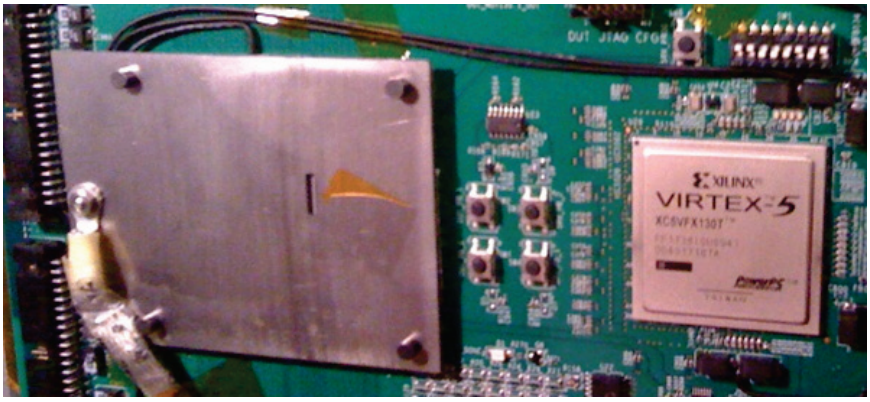

Figure 6-2. Photograph: The ion mask is in place for testing; the Service FPGA is visible on the right, the DUT FPGA is under the mask, where a half of the MGT column is exposed.

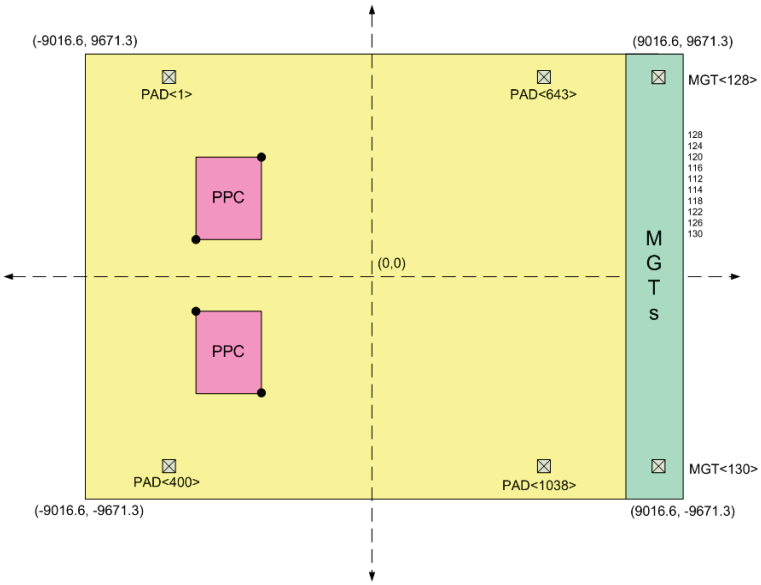

Figure 6-3. Illustration of FX-1 Prototype with MGT Column.

6.1.2 Detecting and differentiating SEE Manifestations

To differentiate between BEs and LOLs, the two types of SEEs expected from the MGTs, error-duration time limits were established. Once the time limit was surpassed by the event, the event is deemed a LOL event and recovery mechanisms were initiated. Events that were fully recovered before the expiration of the time limit were considered BEs. The time limits were extracted from typical lengths of serial communication packets and frames. For example, a common data packet size, such as 2k bytes, would equate to approximately 6.5µs of transmission time in a 3.125Gbps system, so several time limits were extracted from that reference. The thought process being that one or more BEs can exist in a single data packet without affecting more than several bits in error, while a LOL event will negatively affect at a minimum, a large portion of the transmitted packet since activity is required to recover from a LOL. Several BE-LOL time limits were used to separate BEs and LOLs in the test, Table 3 shows the limits used and their characteristics. It must be emphasized that the time limits are implemented to determine the duration of a self-recoverable BE events, not the worst-case duration of a LOL event.

Table 3. Maximum BE duration time limits utilized.

Time Limit	Consecutive 32-bit parallel words in error	No. of Bytes
102 ns	8	32
205 ns	16	64
410 ns	32	128
819 ns	64	256
1.536 µs	128	512
3.277 µs	256	1,024
6.554 µs	512	2,048
13.107 µs	1024	4,096

6.1.3 Test Protocol

A key aspect of the test methodology which facilitates the application of a recovery sequence, as well as the differentiation of self-recoverable BE events and LOL events for each channel, is the use of a custom test protocol. The test protocol permitted any of the given MGT channels to undergo continuous resynchronization attempts while in a LOL state and to transmit test data continuously while in a synchronization state. This was accomplished by synchronizing the test data verification with the test data generation. In summary the protocol's activity consisted of first attempting to synchronize the channel by transmitting synchronization characters. Upon positive verification of synchronization, a test data pattern was then transmitted indefinitely until detection of an LOL event, which initiated the synchronization sequence once again. The test data pattern utilized was a standard 32-bit Pseudo-Random Bit Sequence (PRBS) pattern. The synchronization pattern used is one of the standard "K" or "comma" characters defined by the 8-bit/10-bit encoding standard. The BE/LOL event time limits were measured as consecutive parallel words (See Table 3 on page 18).

The channel was considered synchronized when 256 consecutive 32-bit Sync characters followed by the first 32-bit PRBS data word were verified. Figure 6-4 illustrates the protocol's transmit and verification sequence.

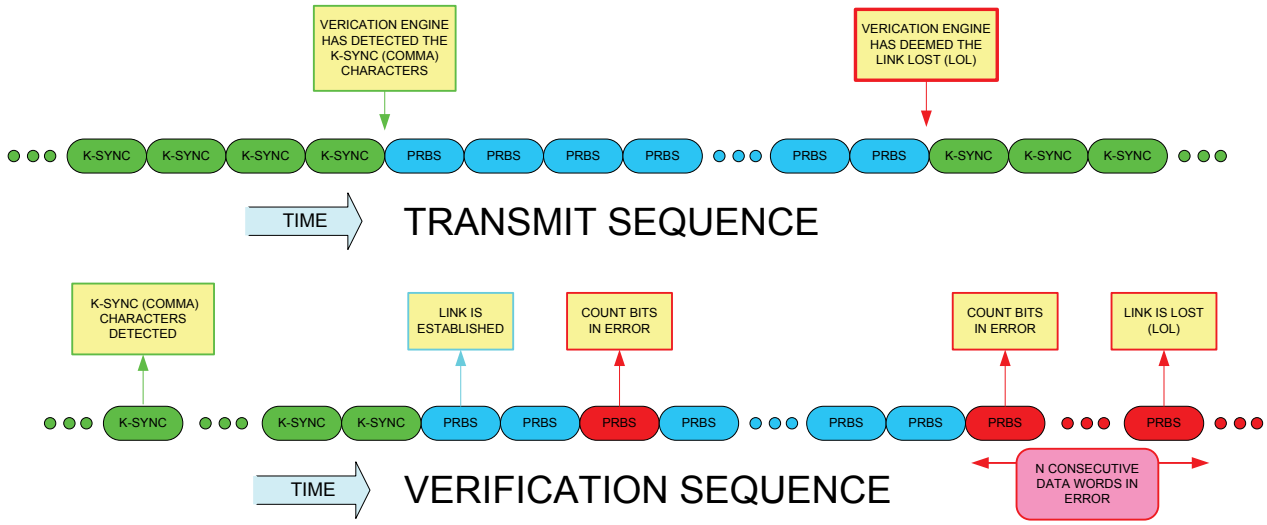

Figure 6-4. SEE Test Protocol Transmit and Verification Sequences.

6.1.4 LOL Event Recovery Sequence

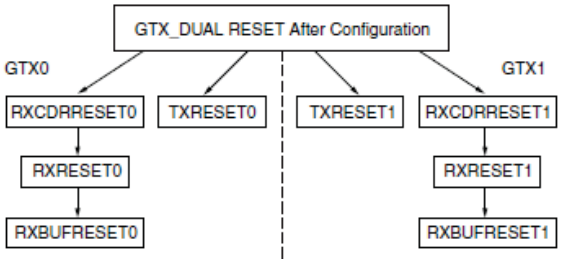

Figure 6-5. Virtex-5QV MGT Primitive (GTX_DUAL) Reset Hierarchy; note the two transceivers in the tile, GTX0 and GTX1.

LOL events are classified by the activity that recovered full functionality of the MGT channel. The results of this classification approach provide the MGT user and designer with a direct evaluation of the impact of the SEE on their system, since activity to recover is necessary. Upon deeming an event a LOL event, that particular channel in error is then commanded to re-synchronize, and after 512ms, if full functionality was not detected, a series of re-initialization commands were then automatically applied one at a time to the particular MGT transmitter or receiver, until the channel recovered full functionality. If after the sequence expired the channel never recovered full functionality, manual interventions were applied to the channel until the functionality is recovered. Manual interventions used are tile-level reset commands, tile power-down commands, and device full-reconfiguration. It must be noted that until the channel is fully recovered, the link is continuously being commanded to re-synchronize. All the automatic recovery sequences employed for the test were obtained from the specific reset signals defined by the MGT primitive, where each of them only affect certain components within the MGT. Figure 6-5 illustrates the hierarchy of resets of the MGT primitive in the Virtex-5QV device, and the description of each is listed in Table 4. Each reset stimuli was applied for 1µs, as is shown in Figure 6-6, which illustrates the chronological order of the event automatic-recovery sequences.

Table 4. MGT primitive resets and description.

Reset Name	Affects	Description
GTX_RESET	Entire tile	This reset systematically resets all subcomponents of the GTX_DUAL tile. This sequence takes about 120µs to complete upon de-assertion. Once asserted, is equivalent to the state of the tile upon configuration of device.
RXCDRRESET<n>	GTX 0 or 1 RX	This reset affects the Clock-Data-Recovery system by temporarily forcing the receiver to give up its current lock and instead lock to the shared PLL Frequency during assertion.
RXRESET<n>	GTX 0 or 1 RX	Resets all aspects of the digital portion of the receiver, or the Physical Coding Sub layer (PCS).
RXBUFRESET<n>	GTX 0 or 1 RX	Only resets the Receiver's elastic buffer
TXRESET<n>	GTX 0 or 1 TX	Resets all aspects of the digital portion of the transmitter, or the Physical Coding Sub layer (PCS).

The available recovery mechanisms that were implemented manually during the test are:

- GTX Tile Reset
- GTX Tile Power Down
- Dynamic Reconfiguration Port (DRP) Scrub
- Device Reconfiguration

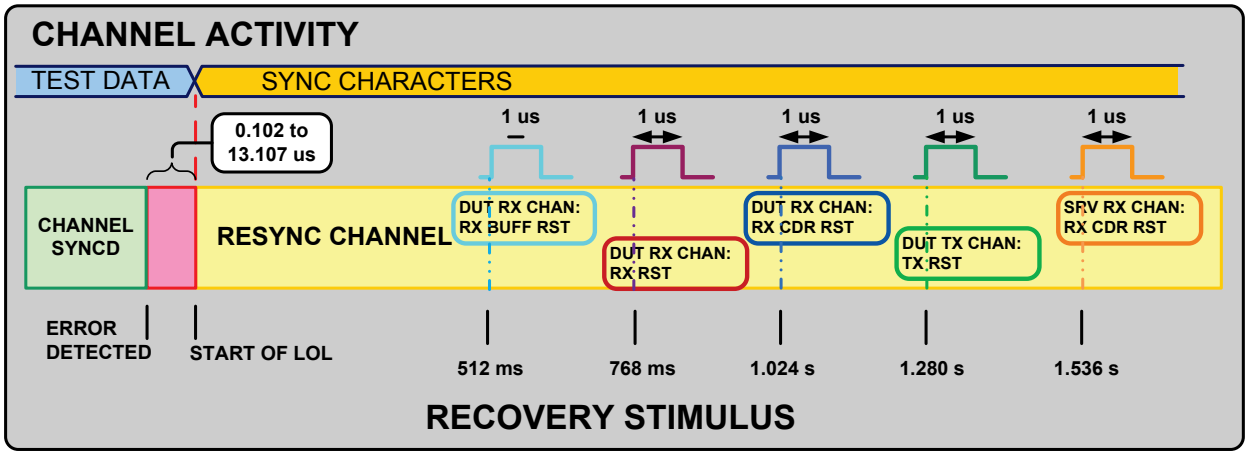

Figure 6-6. MGT Channel Automatic Recovery Stimulus; beyond the last automatic recovery stimulus (> 1.792s), manual mechanisms were applied to the MGT Channel.

6.2 Instrumentation

6.2.1 Physical Interface to MGTs under Test

To interface to the MGTs of the Virtex-5 DUT FPGA, a second Virtex-5 FPGA is employed, referred to as Service FPGA. Each of the MGT channels available in the DUT FPGA is coupled to the MGT channels of the Service FPGA, offering a simple way of providing and retrieving MGT test data from the DUT MGTs. By utilizing the masking technique described in 6.1.1, each MGT test channel is subject to the SEEs incurred by only the RX or TX element of the MGT tile (reference Figure 6-1 on page 16). The Service FPGA also provides the physical paths for the stimulus control to the MGTs under test, and all the test data generation and verification capabilities, as well as the state machines that trigger the auto-recovery mechanisms.

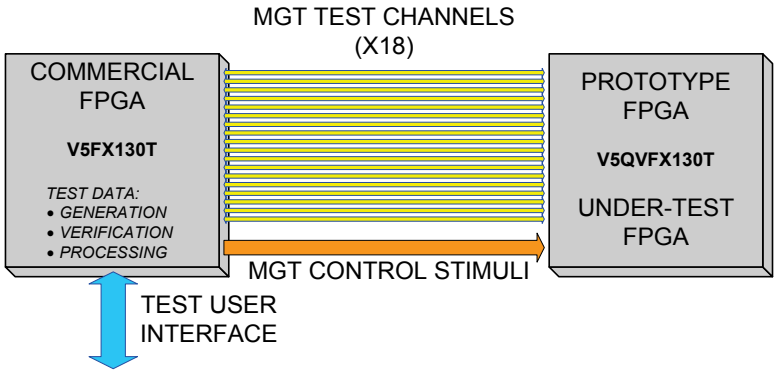

Figure 6-7. MGT Interface illustration for MGT Test Channels in DUT FPGA (right) and Service FPGA (left).

Table 5. Data Products.

Data Product	Description	No. of Chan.	Output Interface
Bit Error (BE) Event Counts	16-bit count of events for each test channel that *did not exceed* the BE/LOL time-limit setting (reference Table 3 on page 18); duplicated for the beam on and beam off states.	20	SRV UART
Bits in Error (BiE) Counts	32-bit count of bits in error accumulated *for each test channel* while *not* in the LOL state, which in essence is the BiE of the BE events; duplicated for the beam on and beam off states.	20	SRV UART
Loss-of-Link (LOL) Event Counts	16-bit count of events for each test channel that *did* exceed the BE/LOL time-limit setting (reference Table 3 on page 18); duplicated for the beam on and beam off states.	20	SRV UART
Channel Synchronization Time	32-bit Word indicating the amount of time the each MGT test channel *was not* in a LOL state. The time granularity used in this measurement is 409.6ns. This provided a method to correct for the particle fluence used in the experiment per test channel; duplicated for the beam on and beam off states.	20	SRV UART
LOL State	1-bit Status indicating LOL status of each channel.	20	SRV UART
Tile Power On/Off State	1-bit Status indicating whether the Service or DUT FPGA MGT Tile is powered or not.	18	SRV UART
Received Data	32-bit Word received by the verification system at the start of the LOL event.	18	FM BrainBox
Expected Data	32-bit Word expected by the verification system at the start of the LOL event.	18	FM BrainBox
LOL Start Time	40-bit Word indicating the exact time the LOL event was detected. The LOL event start time is synchronous across all MGT channels, with a granularity of 12.8ns (parallel clock period).	18	FM BrainBox
LOL Event Duration	40-bit Word indicating the exact time the MGT channel recovered full functionality from the LOL event. The actual LOL event duration must include the BE/LOL time-limit	18	FM BrainBox

	setting (see Table 3 on page 18). The duration granularity used is 12.8ns (parallel clock period).		

6.2.2 MGT Test Data Monitoring

Summarizing, the primary function of the MGT SEE test system consisted of measuring the duration of the error condition on each MGT channel. This duration is used to qualify each event as either a BE or LOL event, as well as triggering a series of recovery stimulus. Real-time data verification was required to be performed on each MGT channel tested. The data products were captured for each MGT test channel are shown in Table 5.

6.2.3 MGT Current Monitoring

The current consumption of the MGTs under test was also monitored to determine if any high current conditions are induced due to ionized-particle interactions. The presence of high current conditions is a good indication that a parasitic latch has been inadvertently instantiated in the device, as a result of the residual ionization track created by the incident particle. To monitor the MGT currents, current-sense resistors were inserted in between the power supply and the device input for each specific MGT power input. The voltage-drop of the sense resistor, which corresponds to the current consumption, is then fed into the analog-to-digital (A/D) converter device that is available in the Service FPGA, referred to as the System Monitor. This embedded feature is only available in the commercial version of the Virtex-5. The Service FPGA System Monitor also provides a 16-to-1 analog multiplexing device, providing the system with 16 channels or the capability to monitor 16 individual currents. An operational amplifier circuit was used to condition the analog sense signal to range the current monitoring system and to meet the input specifications of the System Monitor. Table 6 lists all of the currents being monitored by the system. The I/O supply on channel 16 was instrumented for future tests that would use the same PCB.

Table 6. Current monitoring channel assignments.

A/D Chan.	Supply Monitored	Component	Current Range
1	MGTAVCC	GTX Tile 114	0 to 2 A
2	MGTAVCC	GTX Tile 118	0 to 2 A
3	MGTAVCC	GTX Tile 122	0 to 2 A
4	MGTAVCC	GTX Tile 126	0 to 2 A
5	MGTAVCC	GTX Tile 130	0 to 2 A
6	MGTAVTTTX	GTX Tile 114	0 to 2 A
7	MGTAVTTTX	GTX Tile 118	0 to 2 A
8	MGTAVTTTX	GTX Tile 122	0 to 2 A
9	MGTAVTTTX	GTX Tile 126	0 to 2 A
10	MGTAVTTTX	GTX Tile 130	0 to 2 A
11	MGTAVCCPLL	GTX Tile 114	0 to 2 A
12	MGTAVCCPLL	GTX Tile 118	0 to 2 A
13	MGTAVCCPLL	GTX Tile 122	0 to 2 A
14	MGTAVCCPLL	GTX Tile 126	0 to 2 A
15	MGTAVCCPLL	GTX Tile 130	0 to 2 A
16	VCC-IO	IO Banks 12, 18, 20 and 26	0 to 5 A

6.3 Devices Tested

Xilinx Inc. provided Virtex-5QV "FX-1" prototypes for these experiments. Three different units were used in the all the characterization and exploratory campaigns. Each of them had previously undergone processing to reduce the thickness of the substrate. Since the Xilinx Virtex series of FPGAs use flip-chip architecture, the accelerator's energetic ions must travel the thickness of the back-substrate to reach the sensitive integrated circuits. The thickness of the substrate was reduced by JPL to allow particles with lower energy to make it through to the sensitive area. Table 7 lists the three devices used in these experiments, the thickness of their substrate, and the PCB they were mounted on. Figure 6-8 shows a photograph of one of the DUTs utilized.

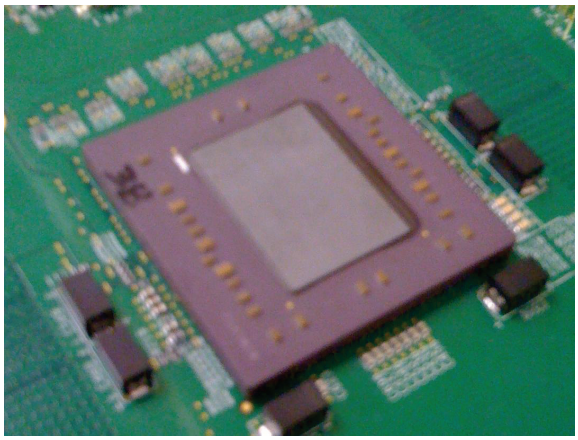

Figure 6-8. Photograph: Processed FX-1 device with exposed substrate mounted directly on to test PCB.

Table 7. Devices tested and processing characteristics.

DUT Device	Substrate Thickness	PCB Serial No
FX-1, SN A4438	200µm	Rev. B 0928-010
FX-1, SN A4421	126µm	Rev. B 0928-008
FX-1, SN A4464	85µm	Rev. B 0928-009

6.4 Test Setup

6.4.1 Test System Hardware

The test system devised for these experiments was based on the XRTCs test platform, which has been employed by Xilinx Inc. and their customers for several generations of Xilinx FPGAs.

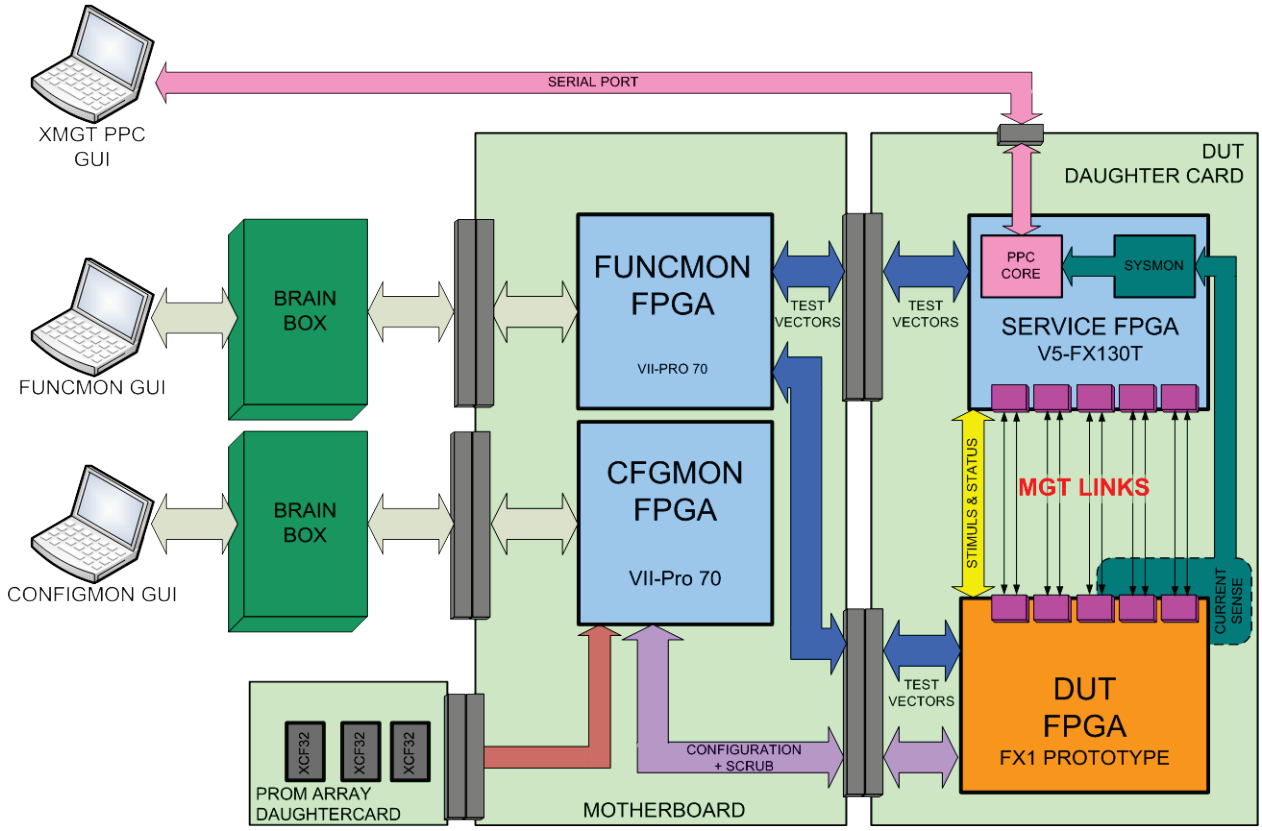

Figure 6-9. Test System top-level diagram.

6.4.1.1 XRTC Motherboard

The principal building-block of the XRTC test platform is the XRTC Motherboard, which has been upgraded through the years to the current design, in use since 2005. The XRTC motherboard hosts a Functional Monitor FPGA (FuncMon), a Configuration Monitor FPGA (ConfigMon), and a multitude of interfaces. The primary interfaces are: to a DUT daughter-card, to host-computers for control and data logging of the FuncMon and ConfigMon FPGAs, to a PROM array daughter-card, and to power supplies. The XRTC ConfigMon and FuncMon external interfaces employ hardware modules commonly known as "Brain Boxes", which format the data being read into log files to be stored in a corresponding laptop; each Brain Box also provides user interface commands to the ConfigMon and FuncMon FPGAs from the host laptops. The PROM array daughter card hosts 12 Xilinx XCF32 Flash-PROM devices that allow the ConfigMon FPGA to access a collection of DUT FPGA designs to be uploaded to the DUT very efficiently while testing. The diagram shown in Figure 6-9 displays the system, also showing the interface to the specific MGT DUT daughter-card devised for these experiments. Typically, the XRTC DUT daughter card architectures do not provide a second FPGA.

As each of the motherboard's FPGA names imply, the FuncMon and ConfigMon FPGAs are used to monitor the particular functionality being tested in the DUT FPGA, and used to monitor the configuration

of the DUT FPGA. Thus for each different experiment, a new FuncMon design is generated, while the ConfigMon FPGA design is shared from experiment to experiment within the XRTC. The ConfigMon code is maintained and kept by Xilinx Inc. Both of the FuncMon and ConfigMon FPGAs are implemented in Virtex-II Pro FPGAs, which meant that for this MGT test, which has to interface to Virtex-5 MGTs, a Virtex-5-based functional monitor FPGA is needed. This issue was resolved by providing a commercial-grade Virtex-5 FPGA (Service FPGA) in the DUT daughter-card. Thus to carry out the test, hardware designs were generated for a MGT daughter card PCB, a Service FPGA, a FuncMon FPGA and a DUT FPGA.

6.4.1.2 MGT Test PCB Daughter-card

A custom test daughter-card was devised for these tests, which interface to the XRTC motherboard as is shown in Figure 6-9. An illustration of the daughter-card's aspect is shown in Figure 6-10

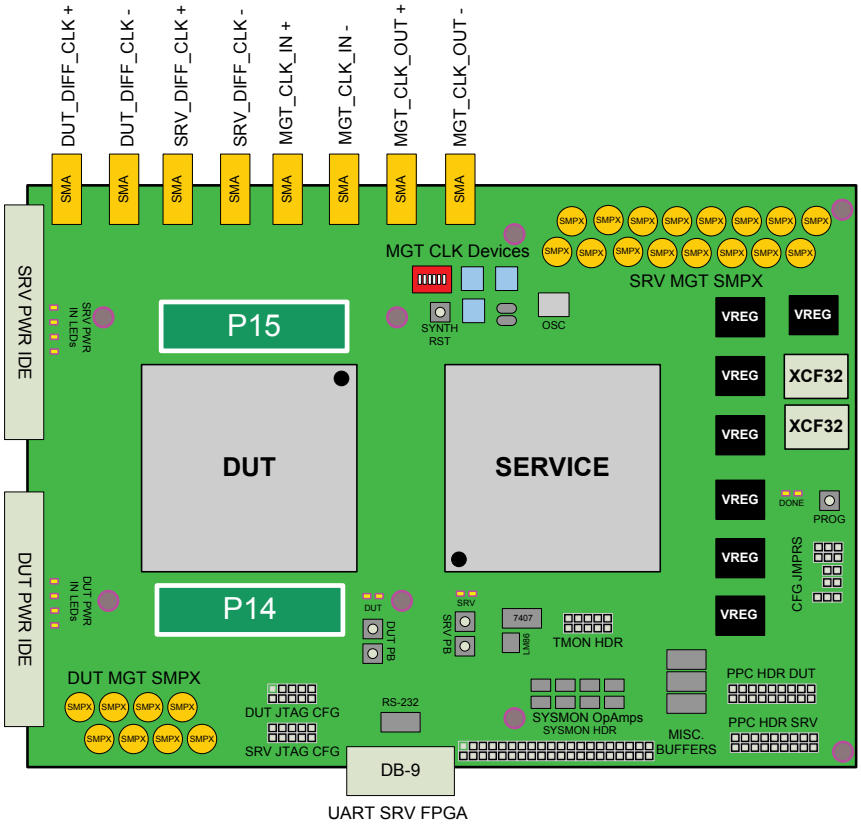

Figure 6-10. MGT Test daughter-card diagram.

The daughter-card interfaces to the motherboard in a mezzanine fashion via two matched-impedance connectors (a.k.a. MICTORs), labeled P14 and P15 on the Figure 6-10 illustration. These connectors are common to all of the DUT daughter-cards employed by the XRTC. For ease of illustration, Figure 6-9 depicts this interface with the connectors in horizontal fashion. The MICTORs provide the test and data vector physical paths for the FuncMon FPGA to interface to the Service and DUT FPGAs. They also provide the SMAP interface that allows the DUT FPGA configuration to be driven by the ConfigMon FPGA. The principal features of the MGT daughter-card are:

- Precision clocking provisions for the Service and DUT MGTs.

- Access to Xilinx XCF32 Flash-PROMs to configure the Service FPGA
- JTAG access to the Service and DUT FPGAs configuration engines.
- External interface SMA connectors for Service and DUT differential clock inputs
- SMA connectors for an externally driven MGT clock source reference.
- SMA connectors to output the MGT reference clock to external test equipment.
- Amplifier circuitry for DUT MGT current monitoring signals.
- Linear regulators for DUT and Service MGT power.
- Service and DUT FPGA temperature monitoring capability via National LM86 temperature monitoring IC.
- Special interface to power adaptor PCB for stand-alone operation.
- Service and DUT FPGA PPC debug headers.
- MGT channel SMPX connectors for external access and monitoring.
- RS-232 transceivers and D-sub connector for a serial UART interface to Service FPGA.

6.4.1.3 FPGA Designs

As stated earlier, three unique FPGA designs were generated for these tests; a DUT, a Service and a FuncMon FPGA were implemented.

Clock Rates

The MGT daughter card provided a clock synthesizer that sourced MGT reference clocks to the MGT Tiles 118 and 120 in both DUT and Service FPGAs. The frequency of the MGT reference clock is 156.25MHz, which was forwarded to the adjacent tiles by tiles 118 and 120. In the configuration utilized, this frequency resulted in a 78.125MHz parallel clock rate, a 156.25MHz internal MGT clock-rate, and a 3.125Mbps line rate. The Service FPGA employed a 100MHz oscillator also provided on the daughter card as a reference clock for all internal operations, and a 33MHz reference clock from the FuncMon for the FIFO data coupling.

6.4.1.3.1 DUT FPGA

The DUT FPGA houses the MGTs under-test. Each of the MGTs RX data output was looped-back into their corresponding top or bottom side MGTs TX data input, so serial data received by an MGT on the "top" side of the column was looped back out through a MGT on the "bottom" side of the column, and vice-versa. In this way, the interleaving concept illustrated in Figure 6-1 on page 16 was possible. Illustrated by Figure 6-11 is the loopback concept for all of the available MGT tiles of the DUT FPGA. Also shown here are the tiles that only have one transceiver available, Tile 124 and Tile 126. The tiles shaded in red receive their clock from highlighted MGT Tile 120, while the tiles shaded in blue receive their clock from the highlighted Tile 118. For the test, the blue tiles were hidden from the ionized particles by the ion mask. The test channels through tiles 112 and 114 were not monitored to avoid any uncertainty issues with what the exact area the ion mask shielded. The resulting arrangement could provide a total of 14 test channels, 7 TX channels and 7 RX channels. The iso-synchronous clock domain cross-over for the parallel data moving between the "red" and the "blue" (or top and bottom) tiles, was accomplished by using shallow asynchronous FIFOs, as illustrated in Figure 6-12. Also shown here is the usage of the DCMs to achieve low latency and skew distribution of the clocks needed by the FIFOs and MGTs. The status outputs of the DCMs were monitored to ensure that they were locked and generating a valid clock signal. The test user was also provided with the ability to

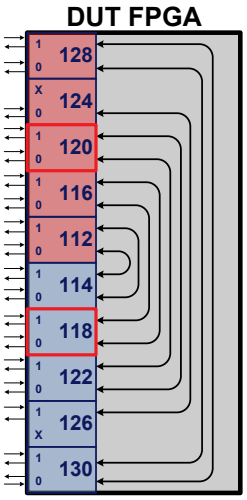

Figure 6-11. DUT FPGA Test Channel top/bottom Loop-back concept.

reset the DCMs at any time. The ion mask shielded all logic, including the FIFO's and DCMs.

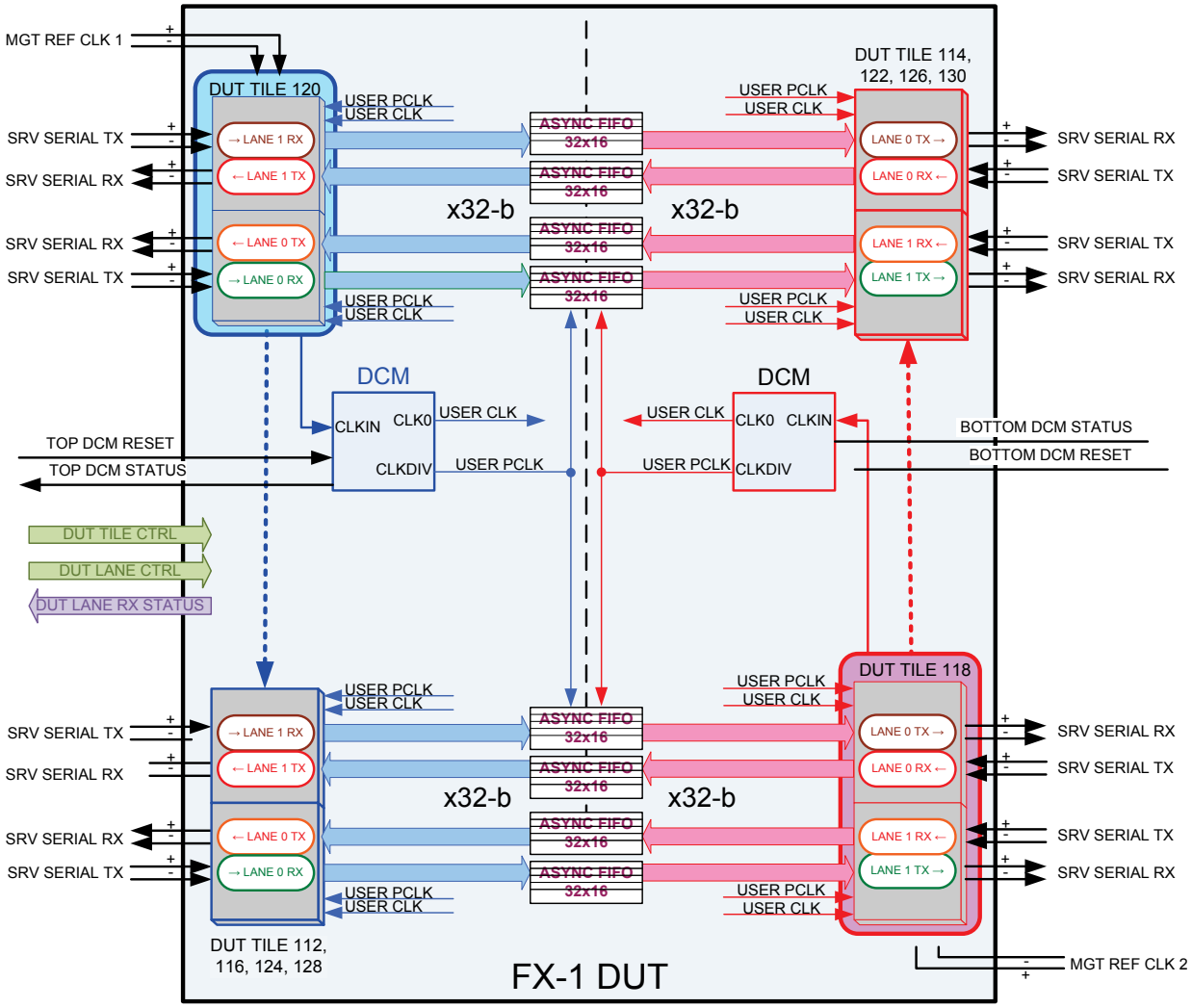

Figure 6-12. Detailed block diagram of DUT FPGA design.

6.4.1.3.2 Service FPGA

The Service FPGA provided all test data generation, verification, and real-time processing for each MGT test channel, as well as the A/D converter and required control mechanisms to relay the DUT MGT current measurements to the appropriate interface hosts. The Service FPGA provided the UART interface to forward the current measurements and the test data counts for each test channel listed in Table 5 on page 21. The Service FPGA also provided a FIFO asynchronous interface to the FuncMon FPGA to forward the LOL event details also listed in Table 5. User access to all Service FPGA test settings and user commands were provided by a command bus interface through the FuncMon FPGA.

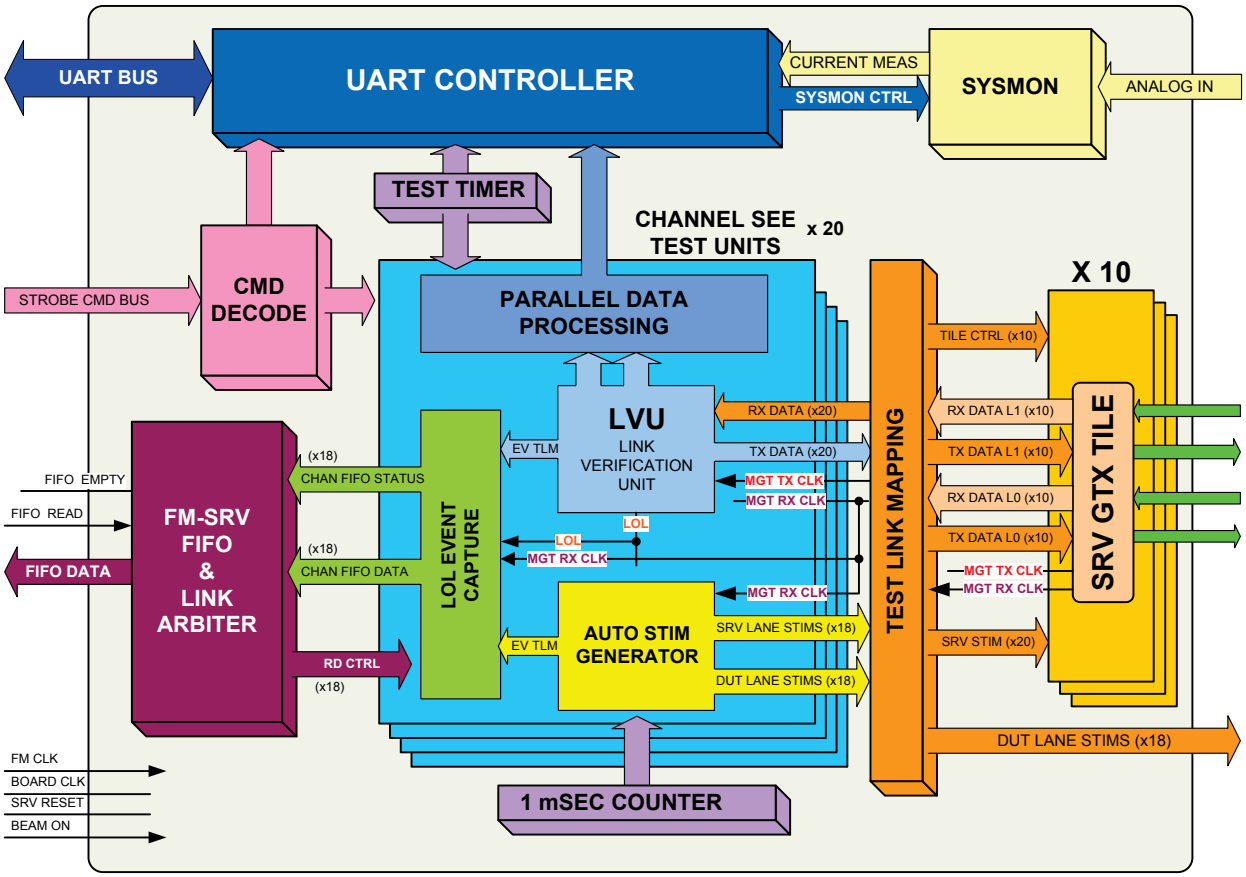

Figure 6-13. Service FPGA Design Block Diagram.

Figure 6-13 illustrates the block diagram of the Service FPGA with all of its functionality. The main element of the service FPGA is the *Channel SEE Test Unit*, which is replicated for each test channel. The test system could have a maximum of 18 test channels, the number of MGT channels available in the DUT Virtex-5QV, but the commercial Virtetx-5 Service has 20 MGT channels, so the extra 2 channels of the Service FPGA are implemented in "internal loopback" mode for functional verification purposes of the Service MGT. Each of the blocks of the Service FPGA design is summarized below:

1) *Channel SEE Test Unit* – Block iterated for each test channel implemented; provides all of the data generation, verification and test data processing capabilities. Made up of the following sub-blocks:
    a. *Link Verification Unit (LVU)* – Main engine of the test channel, providing the test protocol governance of the data generation and verification. The LVU provides the LOL state, the BiE counts, and the Expected and Received data words. Synchronous to the appropriate TX and RX clocks.
    b. *Auto-Stim Generator* – Contains the state-machines that step through the DUT MGT stimulus discussed in Section 6.1.4. This block outputs the discrete signals for the Service FPGA and DUT FPGA MGT stimulus, and is synchronous to the appropriate RX clock. Not implemented for the two Service channels in internal loopback.
    c. *LOL Event Capture* – Contains two 128-bit wide FIFOs, one for the Start of LOL events and one for the Stop of LOL events. It also provides the logic to capture of the LOL

event information; and is synchronous to the appropriate RX clock. Not implemented for the two Service channels in internal loopback.

d. *Parallel Data Processing* – Generates the second order counts that are discussed in section 6.2.2 for each channel, providing separate counts for the beam-on and beam-off scenarios. It also provides the synchronization of the count data to the UART controller block, which is synchronous to the Service FPGA system clock.

2) *Command Decode* – accepts a 6-bit parallel bus and a strobe signal from the FuncMon FPGA and outputs 64 discrete commands. Inputs are synchronous to FuncMon generated clock and outputs are synchronous to the Service FPGA system clock.

3) *UART Controller* – Controls the SysMon block, in order to read out the measured currents, and it also prepares the UART data packets to be transmitted to the host laptop. This block receives its commands from the Command Decoder block. This block employs an embedded PPC, allowing for the SysMon control and UART packet generation to be altered by software. The ratio of transmission of channel test data packets vs. current measurement packets is approximately a 1-to-100 ratio, to maximize current measurement granularity. In this fashion, the system can provide a current reading every ~ 990µs, and a test counts reading every ~ 96ms. This block is synchronized to the Service FPGA system clock.

4) *FuncMon-Service FIFO and Link Arbiter* – This block monitors the status of each test channel's SEE Test Unit and reads data from each of them accordingly, multiplexing each channel's LOL data into a single dual-port asynchronous FIFO that is 128-bits wide. When this FIFO contains data, the FuncMon FPGA will request the data. Inputs are synchronous to the Service FPGA system clock, and the outputs are synchronous to a FuncMon generated clock. T

5) *Test Timer* – Provides the test time value to the UART Controller block and the Channel SEE Unit blocks. The Test Timer block is synchronous to the Service FPGA system clock.

6) *1msec Counter* – Provides all of the Channel SEE Test Units with millisecond pulses for the automatic stimulus generation, also synchronous to the Service FPGA system clock.

7) *System Monitor (SysMon)* – Provides the A/D functions for current monitoring; synchronous to the Service FPGA system clock.

8) *Test Link Mapping* – Maps each of the Channel SEE Test Units input and output data to the appropriate MGT tiles of the Service FPGA, allowing for the top/bottom loopback concept illustrated by Figure 6-11. It also maps the stimulus signals to the DUT FPGA MGTs, and which MGT user clocks generated by the GTX tiles are to be used as RX or TX clocks for each of the Channel SEE Test Units. The use of this block provides a single source of HDL that completely defines the MGT path of each test channel, allowing for efficient loopback concept changes. This block is completely asynchronous.

9) *SRV GTX Tile* – This block represents the Virtex-5 MGT primitive, as shown in Figure 5-2 on page 13. Ten instances of the GTX tile were employed by the design. As with the DUT FPGA, 5 tiles share a "top" side clock and, 5 tiles share a "bottom" side MGT reference clock.

6.4.1.3.3 Functional Monitor (FuncMon) FPGA

The FuncMon FPGA is used by all the experiments that employ the XRTC Motherboard, and a defined design template exists where experimenters can insert their particular test cores with ease. Figure 6-14 shows a block diagram of the FuncMon template, with the external Motherboard and DUT interfaces, while Figure 6-15 illustrates the FuncMon Test Core used in the MGT testing.

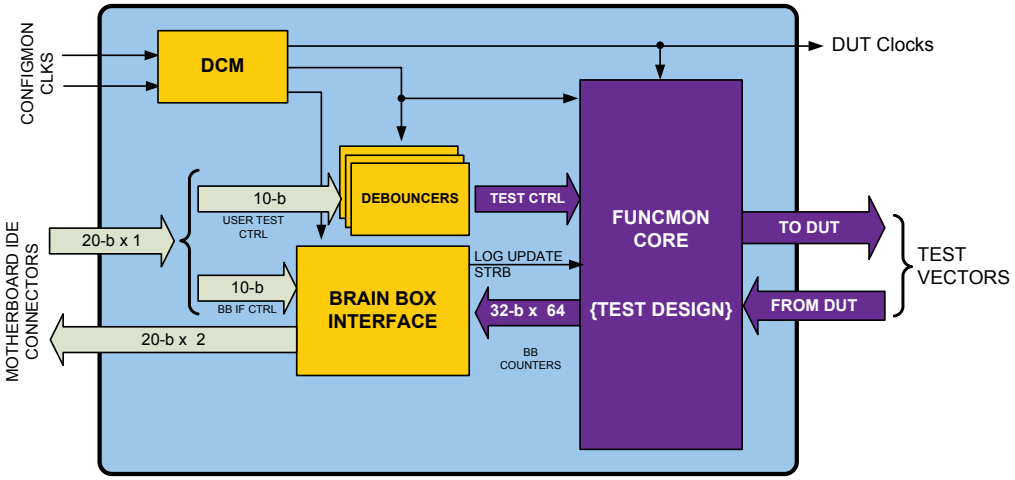

Figure 6-14. XRTC FuncMon FPGA Design Template.

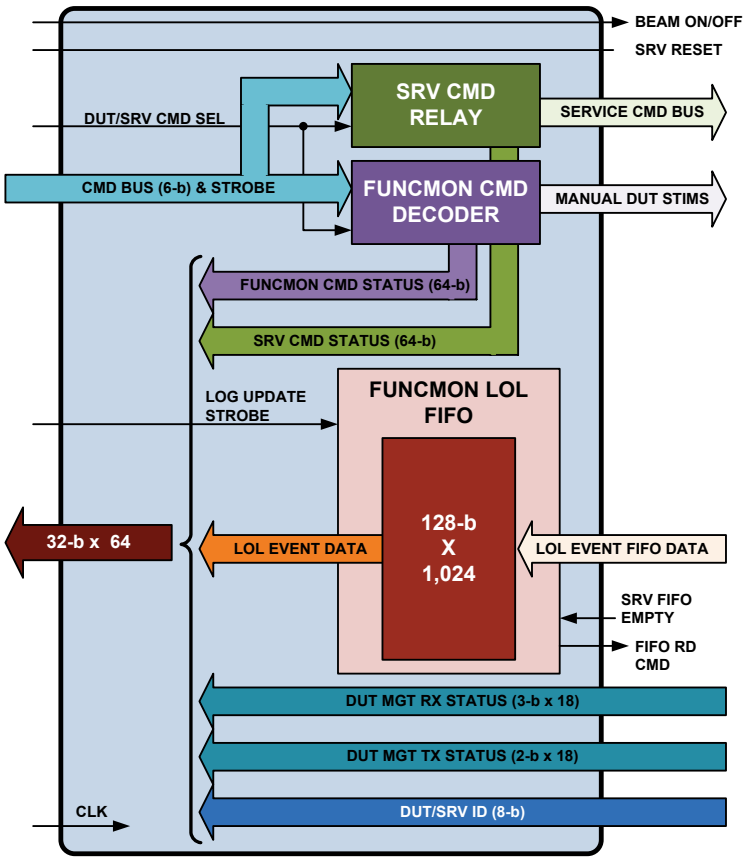

Figure 6-15. FuncMon Test Core used in MGT Testing.

The FuncMon test core consists primarily of a Service-FuncMon FIFO and interface, a FuncMon Command Decoder, and it assigns the LOL Event FIFO data, DUT MGT RX and TX Status, and other house-keeping information to the Brain-Box counter array for data logging, which is made up of 64, 32-bit counters. The user can select one of two command decoders that decode the 6-bit command bus; the FuncMon Command Decoder, which decodes commands that go directly into the DUT FPGA, such as the

manual stimulus commands, and the Service FPGA decoder, which if selected, forwards the command bus to the Service FPGA for the actual decoding to be done in situ.

6.4.2 Test GUIs

As is shown in Figure 6-9, three different test interfaces (GUIs) were used in this test, the Service UART interface, a FuncMon Brain-box interface and a ConfigMon brain-box interface.

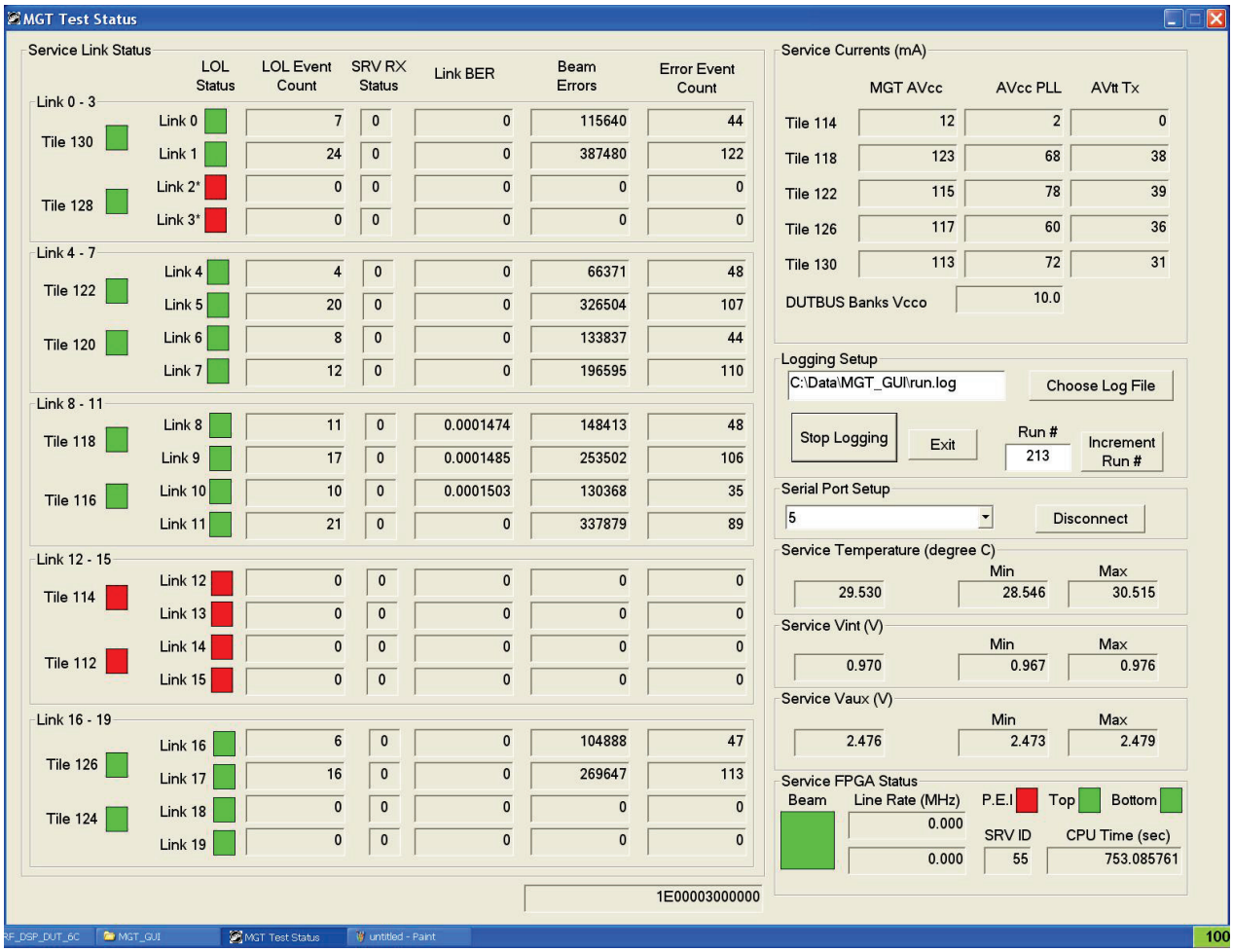

Figure 6-16. Service FPGA Test GUI.

6.4.2.1 Service UART User Interface

This interface was developed specifically for these tests, and only provides monitoring and logging capabilities. Figure 6-16 shows a snapshot of the GUI, and summarizing, it contains the tile and channel status and event counts on the left side of the GUI, and on the right side from top to bottom, the current measurements, log file settings, Service FPGA temperature and voltage information, beam status, line rate status, and DUT DCM top and bottom status. The Service Command status is shown in the bottom side of the GUI. Each channel's Link BER status displays the BER accumulated while the beam is off. All other test channel counts are accumulated only while the beam is on. A log file was scribed by this GUI with about 1,040 entries per second.

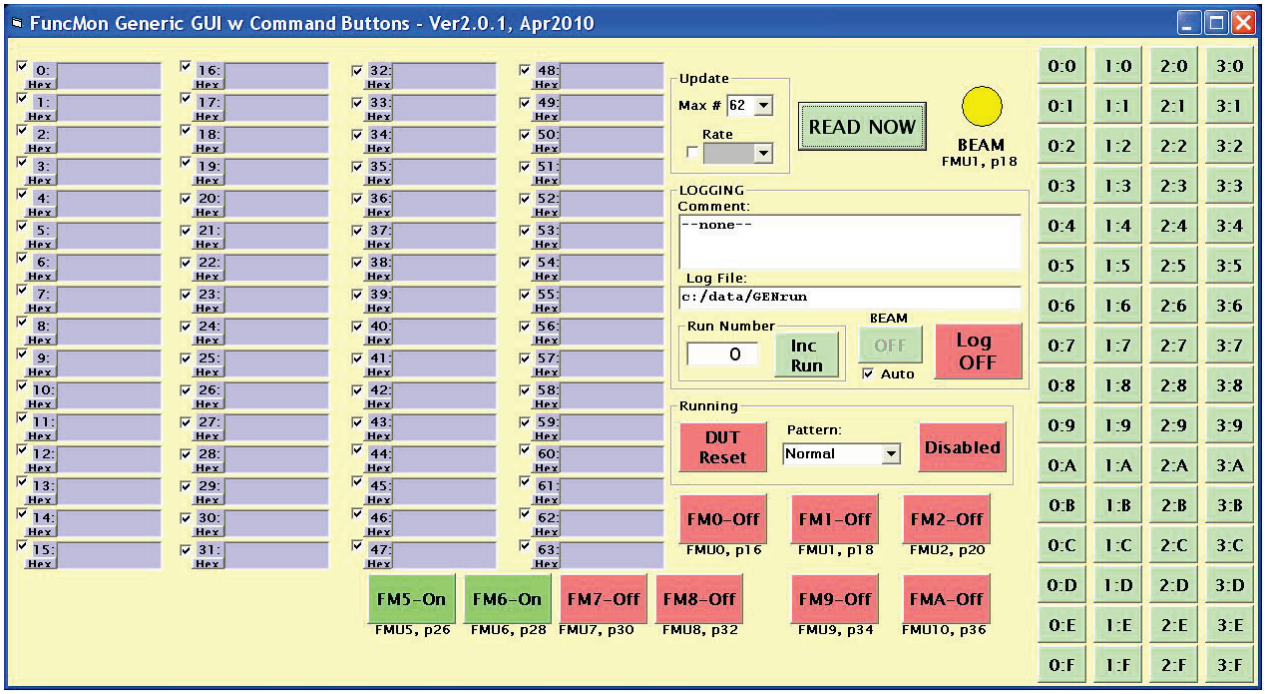

Figure 6-17. Functional Monitor Brain-box GUI.

6.4.2.2 FuncMon User Interface

The FuncMon user interface was based on the generic FuncMon GUI employed by the XRTC, with two unique additions for these experiments. To implement the 6-bit and strobe command bus, 64 distinct command buttons were added, labeled with the Hexadecimal designation. To forward the Beam on/off signal supplied the beam facility; the GUI had to forward the signal via one of the user command signals to the FuncMon. The test status information discussed in section 6.4.1.3.3, was displayed in an array of counters. Figure 6-17 shows the FuncMon GUI utilized for the tests, with the 64, 32-bit counters arranged on the left side, and the 64 command buttons laid out on the right side. In between them, common discrete commands such as DUT Reset and Enable/Disable are shown, as well as the log file settings and the beam on/off indicator.

6.4.2.3 ConfigMon User Interface

The Configuration Monitor GUI is shown in Figure 6-18, and is the same one exercised by all the XRTC experiments. In summary, through this GUI, the test user was able to select different configuration monitoring modes, such as read-back only, scrub only, or read-back/scrub alterations, the user can instantiate a GLUT mask in the DUT FPGA Configuration engine, which masks LUT RAM bits and SRL16 bits from the read-back. Also, through the ConfigMon GUI, the user can select different DUT and FuncMon configuration files, different DUT design mask files, and implement non-essential bit-stream bit masks on top of those. A detailed description of the Configuration Monitor functionality is beyond the scope of this document

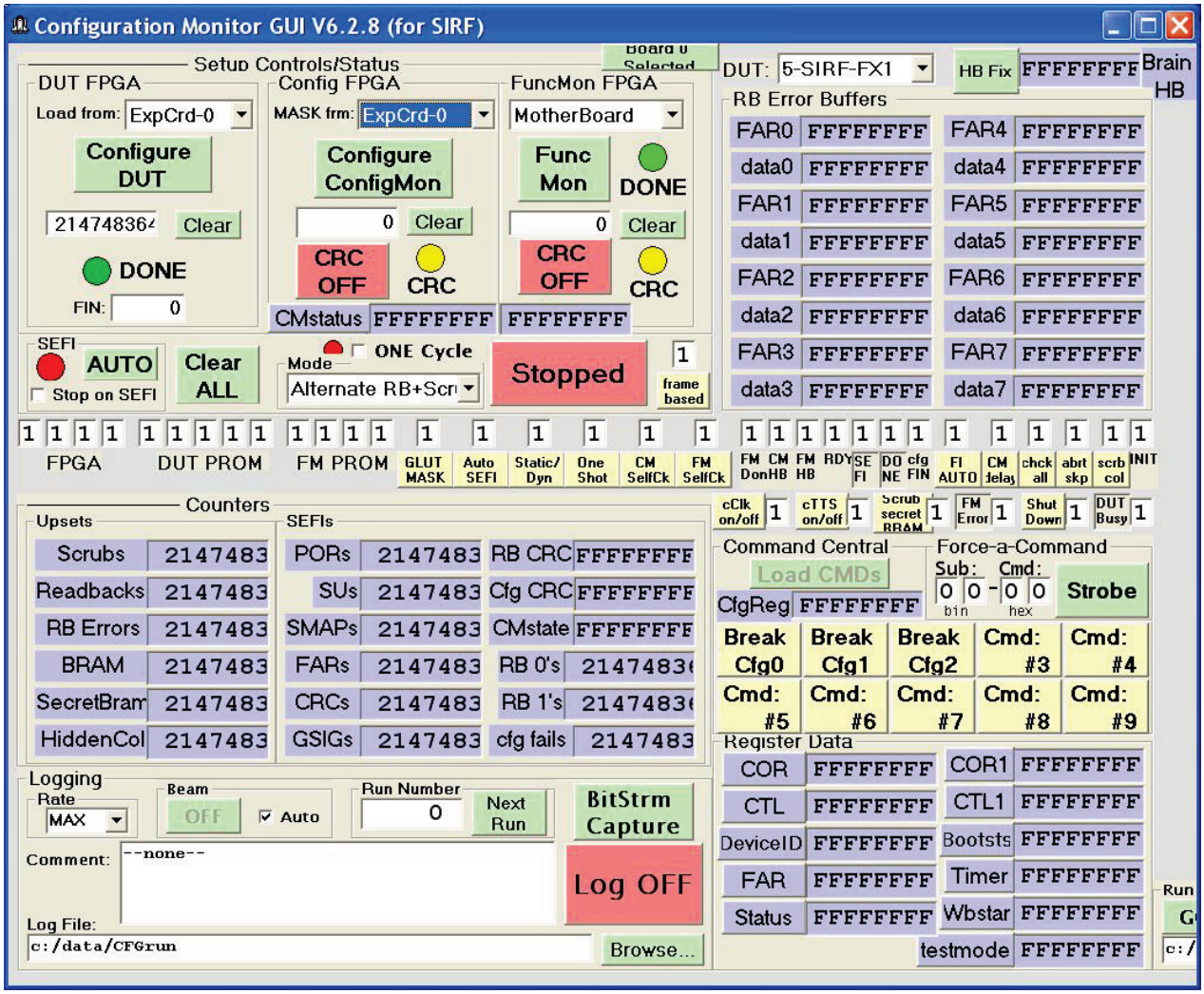

Figure 6-18. Configuration Monitor Brain-box GUI.

6.4.3 DUT Configuration

The DUT FPGA design was being verified for configuration integrity during the irradiation runs. A full-design configuration read-back cycle was performed and followed by a full-design scrub cycle. The read-back and scrub cycles were driven by the ConfigMon FPGA. Each scrub cycle was broken up into individual frames, where the ConfigMon would verify the status of the DUT FPGA's configuration engine before proceeding to scrub the next frame of the design. If the DUT FPGA configuration engine status was unexpected, or failed to respond, the ConfigMon would initiate a reconfiguration process of the DUT FPGA. These configuration engine events are referred to as SEFIs, and have received much attention by the industry (6). The ConfigMon functionality also allows for particular masking of the read-back bit-stream, for instance, the state of the LUT register bit values, the state of the DRP configuration bits can all be read-back and scrubbed. During the testing, a mask was implemented that masked these bits from being scrutinized in the read-back. By removing the mask temporarily, the ConfigMon was able then to scrub the DRP bits.

It must be noted that due to the utilization of an ion mask, where only one half of the MGT column was exposed to heavy ions during the testing, very few configuration errors, and no SEFIs were detected. Configuration errors were not possible to be counted because of a hardware bug existing in the interactions of the MGT DUT PCB and the ConfigMon FPGA. However, since MGT DRP configuration bits were upset and corrected, it served as evidence that regular configuration bits were more than likely also upset; and due to the continuous read-back/scrub cycle operations, these were corrected immediately.

6.5 Test Procedure

The testing was carried out in several beam sessions and at two cyclotrons, at Texas A&M University and at the Lawrence-Berkeley National Laboratories. In the inaugural beam sessions, which were of an exploratory nature, the test procedure was still being fined tuned, but for the later test sessions, which served to do the detailed SEE characterization, the procedure was well defined. Figure 6-19 illustrates with a flow chart the test procedure used for the characterization. It must be noted that each test channel was being verified independently, as discussed in Section 6.4.1.3.2, which includes the individual auto-stimulus activation. The manual stimulus, however, were applied at a tile or device level, which when applied affected at least all 4 of the test channels that were driven through the particular tile, affect the tile sharing the reference clock, or in the case of device-level stimulus, all test channels.

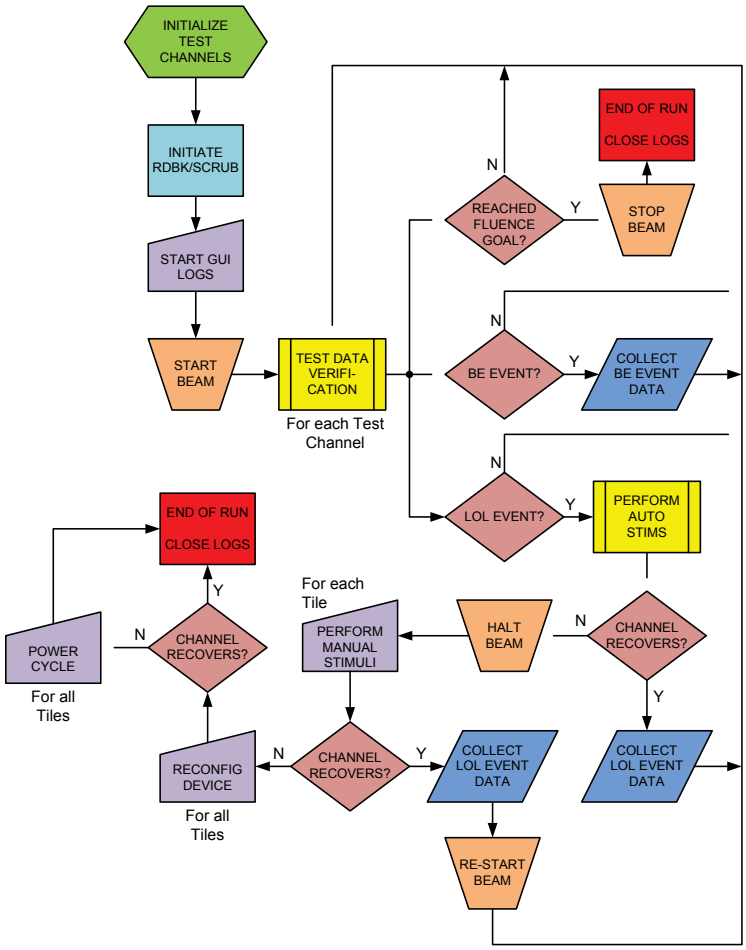

Figure 6-19. Test Procedure Flow-chart.

The manual stimuli employed in the sequence also utilized the GTX tile power-down feature, which removed voltage from the tile. Below is the sequence list of actions:

1) DUT exposed-tile, GTX Reset
2) SRV exposed-tile, GTX Reset
3) DUT masked-tile, GTX Reset
4) SRV masked-tile, GTX Reset
5) DUT exposed-tile power-cycle
6) SRV exposed-tile power-cycle
7) DUT masked-tile power-cycle
8) SRV masked-tile power-cycle
9) DUT device read-back and scrub with GLUT mask disabled (i.e. DRP bits are corrected)
10) DUT exposed-tile, GTX Reset
11) DUT masked-tile, GTX Reset
12) DUT device reconfiguration (i.e. PROG-pin is pulled down)
13) DUT device Power-cycle

The "masked" and "exposed" tiles of each affected channel's depend on the TX or RX function of each test channel. Table 8 shows the TX and RX tile assignments. The tiles shaded in grey are the "masked" tiles. So, for example, if channel 6 needed manual stimuli, DUT Tile 120 is the exposed DUT tile, and Tile 122 is the masked tile; while SRV Tile 122 interfaces to the "exposed" DUT tile, and SRV Tile 120 interfaces to the "masked" DUT tile. The channels with no tile assignments were not monitored.

Table 8. Tile assignment table with masked (in gray) and exposed DUT tiles.

CHAN	DUT		SRV	
	RX TILE	TX TILE	RX TILE	TX TILE
0	130	128	130	128
1	128	130	128	130
2	-	-	-	-
3	-	-	-	-
16	126	124	126	124
17	124	126	124	126
18	-	-	-	-
19	-	-	-	-
4	122	120	122	120
5	120	122	120	122
6	122	120	122	120
7	120	122	120	122
8	118	116	118	116
9	116	118	116	118
10	118	116	118	116
11	116	118	116	118
12	-	-	-	-
13	-	-	-	-
14	-	-	-	-
15	-	-	-	-

7. TEST RESULTS

The testing of the MGTs took place in six test sessions; the first four were of an exploratory nature, in which the methodology, the instrumentation and data verification hardware was established. The latter two test sessions provided the characterization data.

7.1 Exploratory Campaigns

7.1.1 Texas A&M University, November 2009

During this test, a single MGT Tile and one test channel was implemented that transmitted continuous synchronization characters. For verification, the dedicated outputs that signify that a sync/comma character were being monitored. GTX_DUAL outputs RXCHARISCOMMA<n>[3:0] and RXCHARSISK<n>[3:0] were observed and monitored (Reference Figure 5-2 on page 13). Hardware bugs in the DUT PCB at the time did not allow for the DUT design to be scrubbed, thus the testing scope was limited. No masking was utilized in the irradiation. As expected, the synchronization pattern demonstrated both self-recovered and reset-recovered events and a count of the self-recovered error duration events were obtained. Only two runs at one LET value were performed in this session. Table 9 shows the log table and Figure 7-1 shows the cross-section of the duration bins of the self-recovered events, which effectively are BE events and LOL Re-Synchronization events.

Table 9. Experiment Log November 2009 TAMU Experiments.

			ENERGY				EFF RANGE	DEGRDR		RUN	FLUX	FLUENCE	Bad Histogram						RESET
Run	SN	Test	(Mev/u)	Ion	LET	Eff. LET	(um)	#@Deg	Angle	TIME (S)	(p/cm²/s)	(p/cm²)	1.00E-02	1.00E-03	1.00E-04	1.00E-05	1.00E-06	1.00E-07	EVENTS
155	A4438	SYNC	24.8	Ar	15.0	15.0	250.0	3@57	0	378.9	1.07E+05	4.07E+07	4	4	10	15	16	16	4
156	A4438	SYNC	24.8	Ar	15.0	15.0	250.0	3@57	0	160.767	7.72E+04	1.24E+07	2	2	3	4	6	7	1

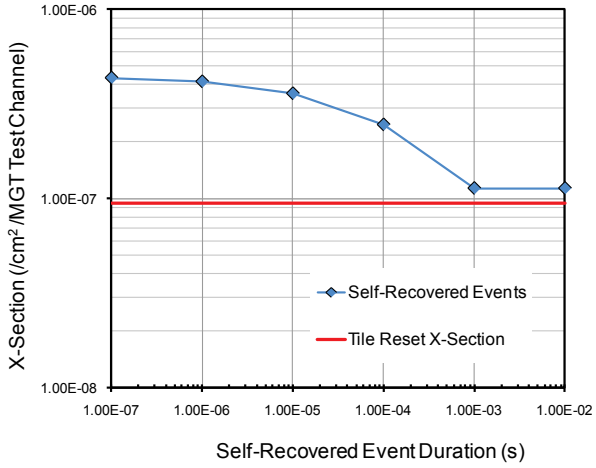

Figure 7-1. Cross-Sections from November 2009 TAMU Experiments.

7.1.2 Lawrence-Berkeley National Labs, December 2009

During this test, two MGT Tiles were implemented, providing 4 MGT test channels, which were arranged in the interleaving fashion illustrated in Figure 6-1 on page 16. The setup did not include the automatic stimulus activation, but all the stimuli to the test DUT MGT Tiles was available to the user for manual implementation. Configuration scrubbing was implemented in this test, and the top/bottom tile masking discussed in Section 6.1.1 was introduced, however data demonstrating its applicability was not obtained. The test protocol methodology presented in Section 6.1.3 was also implemented, but bugs in the channel verification units did not allow for accurate counts on BE events or for self-recovered LOL event counts to be collected. A first look at the cross-section of all LOL events and main recovery mechanisms were

obtained. The counts obtained are shown in Table 10 and a cross-section of all events observed by the MGT tiles is shown in Figure 7-2.

Table 10. Experiment Log December 2009 LBNL Experiments.

RUN	DUT SN	ION	LET	MASK	FLUENCE (p/cm²)	TOTAL EVENTS	DUT RECONFIG	DUT GTX RESET	RX BUF RESET	RX CDR RESET	SRV GTX RESET
21	A4438	Kr	30.86	NO	2.92E+06	4	4				
22	A4438	Kr	30.86	NO	5.00E+07	8	8				
29	A4438	O	2.19	NO	5.00E+07	0					
30	A4438	O	2.19	NO	1.00E+08	0					
32	A4438	O	2.19	NO	1.45E+08	5	4			1	
35	A4438	O	2.19	NO	2.00E+08	2					2
36	A4438	O	2.19	NO	7.86E+07	4	4				
37	A4438	O	2.19	NO	5.44E+07	6	4	2			
38	A4438	O	2.19	NO	2.00E+08	8	4	4			
39	A4438	O	2.19	NO	2.00E+08	5	4		1		
40	A4438	O	2.19	NO	2.00E+08	5	4		1		
41	A4438	O	2.19	NO	2.00E+08	4		4			
43	A4438	O	2.19	NO	2.00E+08	12	12				
44	A4438	Ar	9.74	NO	2.00E+06	0					
45	A4438	Ne	3.49	NO	2.07E+06	0					
46	A4438	Ne	3.49	NO	5.06E+07	0					
47	A4438	Ne	3.49	NO	2.00E+08	4	4				
48	A4438	Ne	3.49	NO	2.00E+08	2		2			
49	A4438	Ne	3.49	YES	2.00E+08	0					
50	A4438	Ne	3.49	YES	2.00E+08	0					
51	A4438	Ne	3.49	YES	2.00E+08	0					
52	A4438	Ne	3.49	YES	2.00E+08	0					

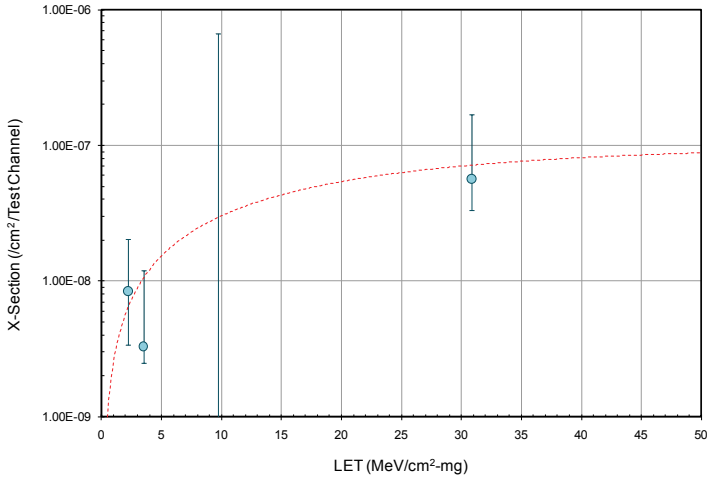

Figure 7-2. Cross-Sections from December 2009 LBNL Experiments.

7.1.3 Lawrence-Berkeley National Labs, January 2010

In the January 2010 tests at LBNL, two test tiles were implemented in the DUT providing 8 test channels, the DUT design shown in Figure 6-12 was implemented, the first Service FPGA current measurements were taken and the mask was implemented in the majority of the runs with confidence. It was also observed that using the mask shielded the DUT FPGA DCMs, which proved to be more sensitive than the MGTs and required continuous DCM reset activity in the runs where the mask was not in place. Separation of TX and RX effects was demonstrated in this test, and the current measurements demonstrated no significant current increases in the test tiles. In this test, were an embedded processor was providing the current measurements from the Service FPGA out to the host laptop, large increases in the temperature of the Service FPGA in the vacuum environment were observed that would cause the Service FPGA to cease working, preventing continuous operation in vacuum. Midway through the testing the embedded processor was removed from the Service FPGA. The bugs were still present in the

test channel data verification which added uncertainty in the LOL event duration and BE, LOL and BiE counts, and thus accurate counts were still not available. No DUT reconfiguration events were observed, leading to the conclusion that the DUT reconfiguration events of the December tests were due to the DCM needing reset and the setup not having that capability. In this test, the capability of resetting the DUT was available. Data obtained from this experiment along with data from the TAMU March 2010 test was presented at the SEE Symposium in April 2010 (7). Table 11 shows the experimental table and Figure 7-3 the cross-section of the data.

Table 11. Experiment Log January 2010 LBNL Experiments.

RUN	SN	MASK	ENERGY (Mev/u)	ION	EFF LET	ANGLE	RUN TIME	FLUX (p/cm^2/s)	FLUENCE (p/cm^2)	RX BUFF RESET	TX RESET	TILE RESET
65	A4421	YES	16	Kr	25	0	73.22	2.01E+04	1.47E+06	1		
66	A4421	YES	16	Kr	25	0	37.03	2.04E+05	7.55E+06	1		
67	A4421	YES	16	Kr	25	0	19.28	1.76E+05	3.39E+06	1		
68	A4421	YES	16	Kr	25	0	113.14	1.88E+04	2.13E+06	1		
69	A4421	YES	16	Kr	25	0	76.56	1.92E+04	1.47E+06	1		
70	A4421	YES	16	Kr	25	0	57.82	1.92E+04	1.11E+06	2		
71	A4421	YES	16	Kr	25	0	157.93	1.91E+04	3.02E+06	1		
72	A4421	YES	16	Kr	25	0	56.6	1.98E+04	1.12E+06	0		
73	A4421	YES	16	Kr	25	0	114.06	2.04E+04	2.33E+06	0		1
74	A4421	YES	16	Ar	7.27	0	40.84	7.96E+04	3.25E+06	1		
75	A4421	YES	16	Ar	7.27	0	74.78	7.80E+04	5.83E+06	1		
76	A4421	YES	16	Ar	7.27	0	11.49	7.82E+04	8.98E+05	1		
77	A4421	YES	16	Ar	7.27	0	89.69	7.72E+04	6.92E+06	1		1
78	A4421	YES	16	Ar	7.27	0	391.67	7.40E+04	2.90E+07	11		
79	A4421	YES	16	Cu	16.5	0	295.74	1.98E+04	5.87E+06	7	1	
80	A4421	YES	16	Si	4.35	0	64.48	3.24E+02	2.09E+04	0		
81	A4421	YES	16	Si	4.35	0	144.59	1.65E+05	2.39E+07	6		1
82	A4421	YES	16	Si	4.35	0	142.42	1.61E+05	2.29E+07	5	1	
83	A4421	YES	16	Ne	2.39	0	11.05	8.87E+05	9.80E+06	2		
84	A4421	YES	16	Ne	2.39	0	78.62	4.48E+05	3.52E+07	3		
85	A4421	YES	16	Ne	2.39	0	158.18	4.38E+05	6.93E+07	6		
86	A4421	YES	16	O	1.54	0	208.74	8.81E+05	1.84E+08	10		
87	A4421	YES	16	N	1.16	0	80.67	1.08E+06	8.68E+07	5		
88	A4421	YES	16	N	1.16	0	21.12	1.14E+06	2.40E+07	4		
89	A4421	YES	16	N	1.16	0	106.68	1.14E+06	1.22E+08	11		

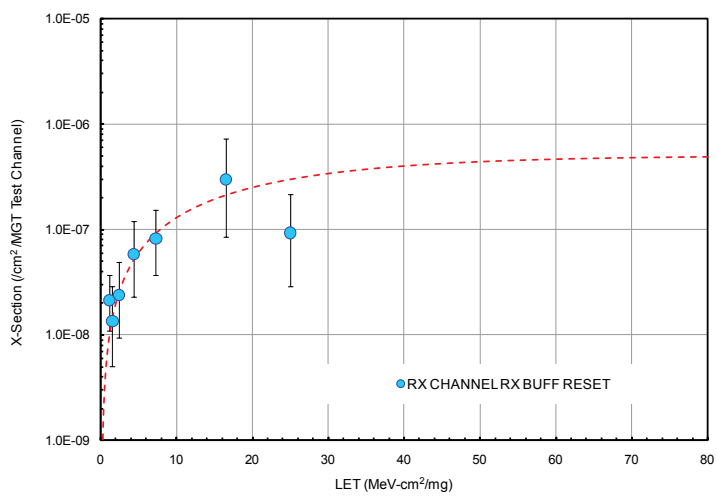

Figure 7-3. Cross-Sections from January 2010 LBNL Experiments.

7.1.4 Texas A&M University, March 2010

For the March TAMU tests, the Service FPGA was advanced to now make 12 test channels available. Issues in the integration of the multiple test channels into the Service FPGA didn't allow for the new data verification units to be implemented in time for this test, so BiE, and BE counts and LOL-event data were still not accurately collected. The integration setbacks also prevented the automatic stimulus recovery mechanism to be implemented, so they had to be done manually, and also limited the number of effective

test channels available to 8. LOL counts were obtained and separation of re-synchronization LOL events and LOL events that required stimulus was possible. Current measurements were obtained and were considered valid. This data, and together with the data from the January 2010 LBNL tests, was presented at the SEE Symposium conference in La Jolla, California (7). It must be noted that events manifested as a "burst of events" were observed during these tests; these interesting events were also observed in DSP element testing that the authors were also undertaken in parallel (8). "Burst" events are characterized by occurring at a rate at least 100 times quicker than what are considered "normal" events, which never exceed a rate of 1 event every 100ms during the testing, while "burst" events, generate hundreds or thousands of events for every 100ms. Test channels that suffered this effect were removed from the data set. Figure 7-4 and Table 12 show the cross-sections obtained and the experimental log table.

Table 12. Experiment Log March 2010 Texas A&M Experiments.

RUN	SN	ENERGY (Mev/u)	ION	LET	EFF LET	EFF RANGE (um)	DEGRDR (#@angle)	ANGLE	RUN TIME (s)	FLUX (p/cm²/s)	FLUENCE (p/cm²)	TEST CHANNEL	CHANNEL TYPE	SYNC TIME (S)	ACTUAL FLUENCE (p/cm²)	TOTAL LOL COUNTS	AUTOSTIM LOL	RESYNC LOL
128	A4421	24.8	Xe	49.0	49.0	140.3	none	0	122.7	3.293E+04	4.039E+06	8	TX	55.75	1.836E+06	117	102	15
128	A4421	24.8	Xe	49.0	49.0	140.3	none	0	122.7	3.293E+04	4.039E+06	9	RX	114.36	3.766E+06	103	11	92
128	A4421	24.8	Xe	49.0	49.0	140.3	none	0	122.7	3.293E+04	4.039E+06	10	TX	121.77	4.011E+06	103	11	92
128	A4421	24.8	Xe	49.0	49.0	140.3	none	0	122.7	3.293E+04	4.039E+06	11	RX	105.64	3.479E+06	96	16	80
202	A4421	40.0	Ar	10.0	10.0	123.1	5@55.813	0	268.9	1.441E+05	3.877E+07	8	TX	264.64	3.818E+07	117	28	89
202	A4421	40.0	Ar	10.0	10.0	123.1	5@55.813	0	268.9	1.441E+05	3.877E+07	9	RX	263.13	3.796E+07	103	15	88
202	A4421	40.0	Ar	10.0	10.0	123.1	5@55.813	0	268.9	1.441E+05	3.877E+07	10	TX	263.37	3.800E+07	103	15	88
202	A4421	40.0	Ar	10.0	10.0	123.1	5@55.813	0	268.9	1.441E+05	3.877E+07	11	RX	262.10	3.782E+07	96	16	80
209	A4421	40.0	Ar	4.1	4.1	933.3	none	0	141.4	4.301E+04	6.080E+06	8	TX	139.18	5.985E+06	18	1	17
209	A4421	40.0	Ar	4.1	4.1	933.3	none	0	141.4	4.301E+04	6.080E+06	9	RX	121.86	5.240E+06	16	2	14
209	A4421	40.0	Ar	4.1	4.1	933.3	none	0	141.4	4.301E+04	6.080E+06	10	TX	139.18	5.985E+06	21	1	20
209	A4421	40.0	Ar	4.1	4.1	933.3	none	0	141.4	4.301E+04	6.080E+06	11	RX	123.37	5.305E+06	14	2	12
214	A4421	40.0	Ne	1.2	1.2	1510.0	none	0	602.8	1.905E+05	1.148E+08	8	TX	599.24	1.143E+08	43	2	41
214	A4421	40.0	Ne	1.2	1.2	1510.0	none	0	602.8	1.905E+05	1.148E+08	9	RX	599.24	1.143E+08	44	5	39
214	A4421	40.0	Ne	1.2	1.2	1510.0	none	0	602.8	1.905E+05	1.148E+08	10	TX	599.24	1.143E+08	49	2	47
214	A4421	40.0	Ne	1.2	1.2	1510.0	none	0	602.8	1.905E+05	1.148E+08	11	RX	596.38	1.138E+08	42	7	35
228	A4421	40.0	N	0.6	0.6	2177.0	none	0	273.7	6.340E+05	1.736E+08	8	TX	272.96	1.736E+08	14	1	13
228	A4421	40.0	N	0.6	0.6	2177.0	none	0	273.7	6.340E+05	1.736E+08	9	RX	272.96	1.736E+08	13	1	12
228	A4421	40.0	N	0.6	0.6	2177.0	none	0	273.7	6.340E+05	1.736E+08	10	TX	272.18	1.731E+08	14	2	12
228	A4421	40.0	N	0.6	0.6	2177.0	none	0	273.7	6.340E+05	1.736E+08	11	RX	272.96	1.736E+08	12	1	11
228	A4421	40.0	N	0.6	0.6	2177.0	none	0	273.7	6.340E+05	1.736E+08	12	TX	272.96	1.736E+08	13	-	-
228	A4421	40.0	N	0.6	0.6	2177.0	none	0	273.7	6.340E+05	1.736E+08	14	TX	272.96	1.736E+08	12	-	-

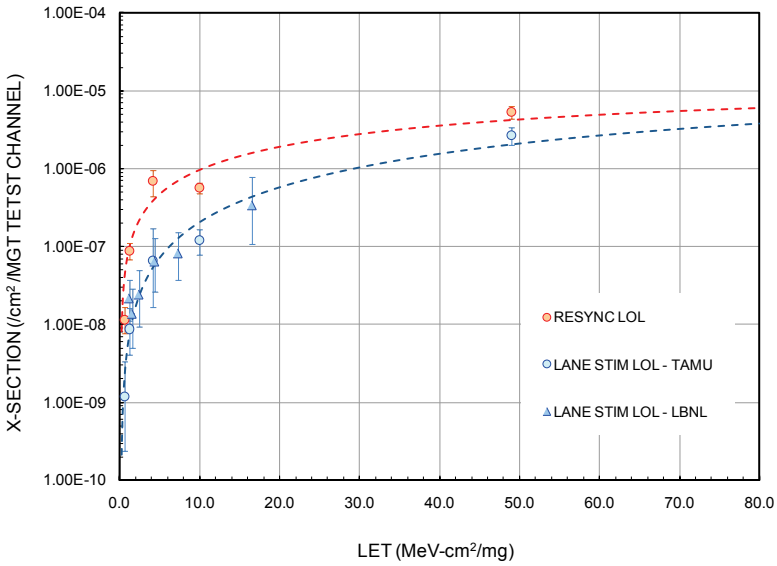

Figure 7-4. Cross-Section from March 2010 TAMU Experiments.

7.2 Characterization Tests

For the final characterization tests, 12 MGT test channels were implemented effectively. The test provided the full detailed LOL event data, and the complete set of automatic recovery mechanisms. The

characterization tests were done over two sessions at Texas A&M during May and August of 2010. Tables A-1 and A-2 in Appendix A show the experimental log for each run and each test channel. The automatic stimulus event column headers are highlighted in light gray, while the manual stimulus events are hihglighted in dark gray. Blank entries in the tables signify zero or no counts. Some of the test-channels had to be discarded due to the presence of oscillatory events which corrupted the LOL, BiE and BE counts, as well as the LOL Event words. Other notes on any acquisition difficulties for each run are also listed in tables A-1 and A-2. The curve parameters for all the Weibul fits are listed in Section 8.6, and the details of the cross-section data and error calculation as a function of LET are shown in Appendix C.

7.2.1 Bit Error Events

Bit Error event counts were accumulated for each test channel 32-bit word with at least one bit in error. They were accumulated in the Service FPGA and logged via the Service UART interface; only counts during the "beam on" state were considered. The counts for each run and channel had to be corrected for the Bit Error events caused by an eventual LOL event. The plot in Figure 7-5 shows the BE cross-section vs. LET for TX and RX channels, and the manually fitted Weibul curve.

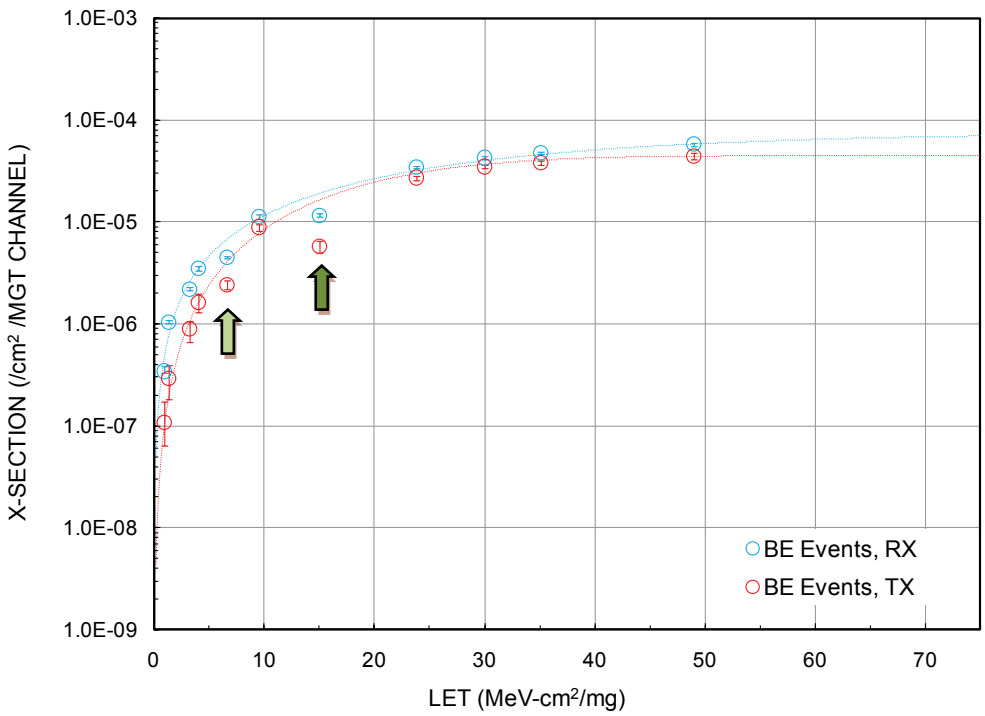

Figure 7-5. BE Event Cross-Section vs. LET.

It must be noted that the average effective penetration range for all LET runs was approximately 400µm, while the estimated penetration range for the runs with LETs of 6.6 and 15.0, is 33.9 and 40.2µm respectively. The small margin provided by these runs with respect to the other runs, questions whether the stack-up of tolerances required by the dosimetry calculations was violated, and perhaps leading to both LET and Fluence calculation errors. The cross-section data points for the LETs in question were not considered for the Weibul fit; the points are indicated by arrows in Figure 7-5.

7.2.2 Loss-of-Link Events

Loss-of-link event counts were captured for all TX and RX channels. They were accumulated in the Service FPGA, and dispensed through the Service UART. LOL event counts were also extracted by the number of LOL event words through the FuncMon GUI Logs. In a few runs the number of counts disagreed between the direct counts and the LOL event counts. This was seen in the runs where oscillatory events occurred on any of the channels, which would flood the 12 channel event-capture bandwidth, resulting in a few events in each of most of the channels to not be extracted in time and become overwritten. This can be seen in Tables A-1and A-2. The LOL event counts from the Service UART Log had to be corrected for the LOL events incurred while the beam was off, specifically while intrusive manual tile recovery activity was taking place.

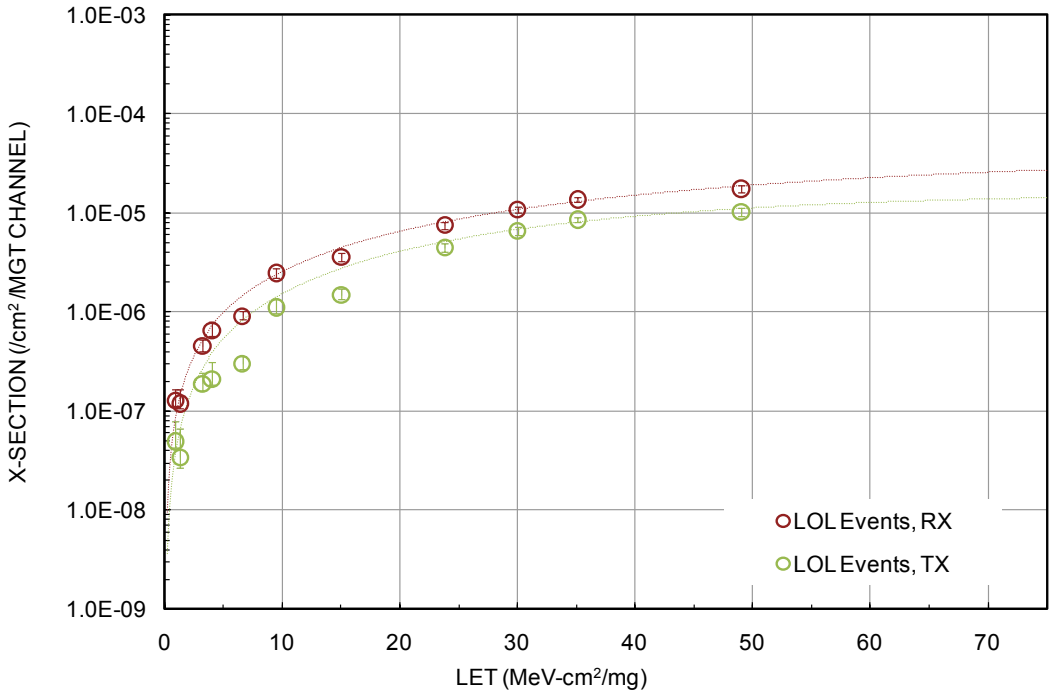

Figure 7-6. LOL Event Cross-Section vs. LET.

The data points at LETs of 6.6 and 15.0 were also omitted from the Weibul fit, since they also appear to have LET/Fluence errors, as discussed in 7.2.1. In this case however, the wide knee of the data set obscures the visual effect a bit more.

7.2.2.1 TX Channel LOL Events

The large majority of LOL events observed on the TX channels were recovered by the channels resynchronization activity. All TX channel LOL events requiring re-initialization were recovered by the test channel's respective Service FPGA RX Channel's CDR Reset. This is the downstream MGT RX element of the affected TX channel. Figure 7-7 shows the cross-sections of the LOL events for the TX that were recovered by resynchronization and that were recovered by the down-stream RX CDR reset. Both of these cross-sections are plotted against the Weibul-fit for the overall LOL counts of the TX channels. LOL events were so few that their cross-section is barely discernible from the Poisson zero-event statistical noise.

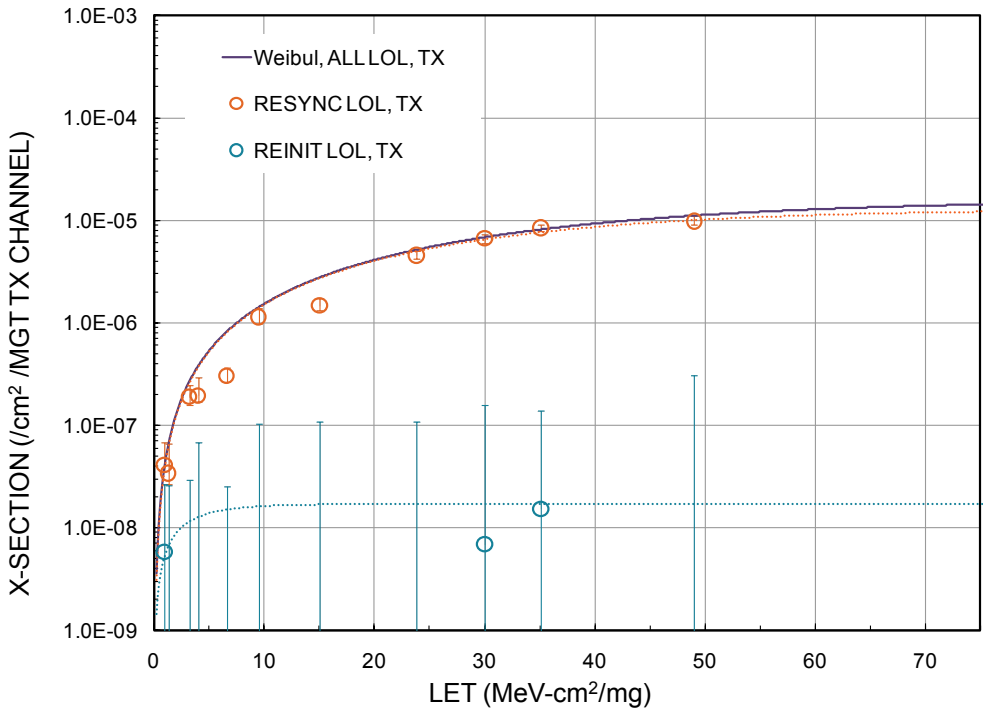

Figure 7-7. TX LOL Events Cross-Section vs. LET.

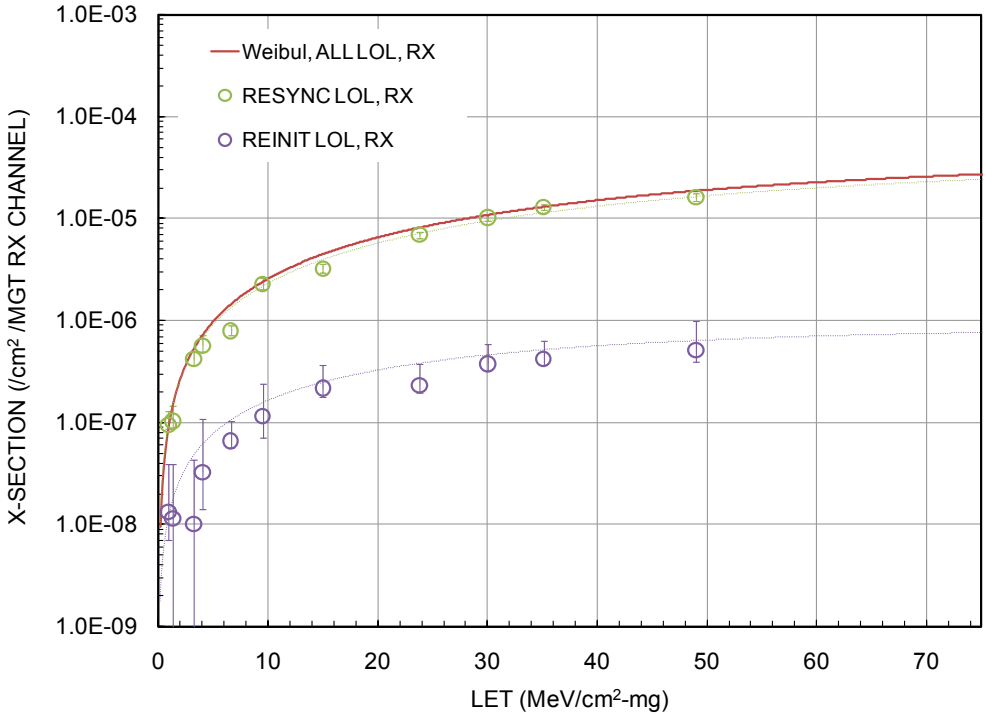

Figure 7-8. RX LOL Events Cross-Section vs. LET.

7.2.2.2 RX Channel LOL Events

As is the case with the TX channels, the large majority of LOL events observed on the RX channels were recovered with the resynchronization activity. However, many LOL events were observed that needed the test channel's automated resets/recoveries. Figure 7-8 shows the cross-sections of the LOL events for the RX channels that were recovered by resynchronization and the ones that were recovered by the automated resets, these latter ones rare eferred to as Re-Initialization or ReInit LOL events, since lane-level resets are actuated by most protocols when reinitializing a channel. In Figure 7-8, both of these cross-sections are plotted against the Weibul-fit for the overall LOL counts of the RX channels. The ReInit LOL event cross-section for the MGT RX functions is almost two orders of magnitude higher than for the TX channels.

The cross-sections of the different RX MGT lane resets are shown in Figure 7-9. The RX Buffer Reset's cross section dominates the RX Reset and RX CDR Reset's cross-sections. Also shown in Figure 7-9 is the Weibul-fit for all the RX ReInit LOL events. The larger threshold of Clock-Data Recovery (CDR) Resets should also be noted.

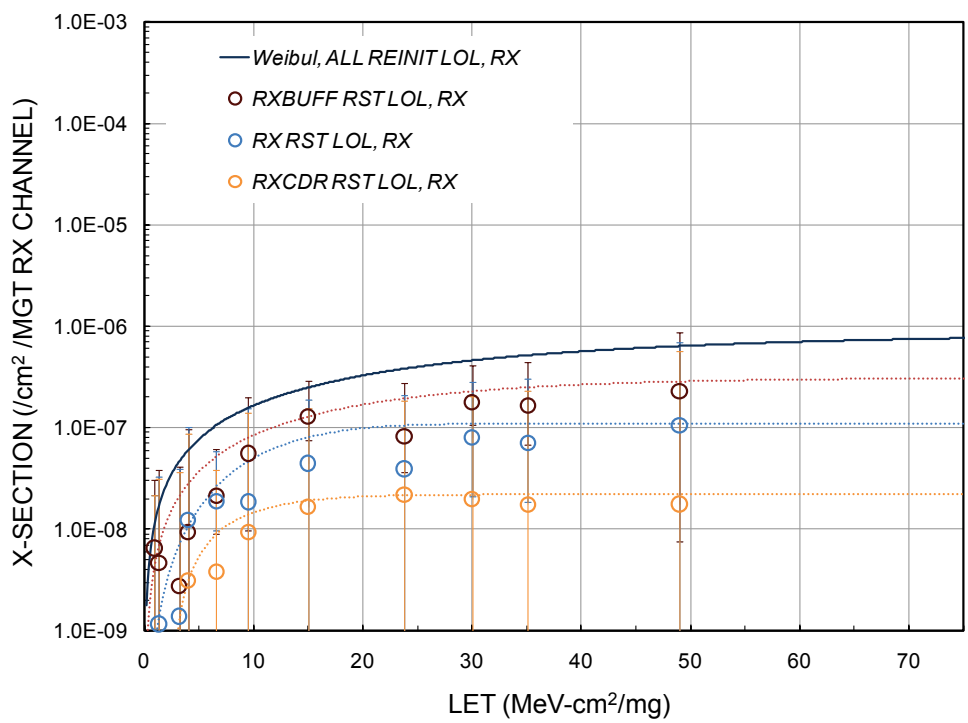

Figure 7-9. RX Re-Initialization LOL Events Cross-Sections vs. LET.

7.2.2.3 GTX Tile Reset LOL Events

GTX tile resets were implemented manually whenever LOL events were observed by the experimenters to not recover within 3 or 4 seconds after the automated stimulus was complete. Of all the characterization tests, only one GTX reset event was observed to be required on a TX channel; the TX to RX channel event ratio being 1/166. Cross-section per test channel is shown in Figure 7-10 on page 44. Even though the cross-section is calculated per channel, it must be noted that the GTX reset activation affects all channels of the tile.

7.2.2.4 MGT Dynamic Reconfiguration Upset Events

Figure 7-10 on page 44 also shows the cross-section measured of LOL events that were recovered by scrubbing the DUT FPGA configuration with the GLUT mask removed. The GLUT mask disables scrubbing of certain bits of the configuration, specifically the configuration bits that can be reconfigured via the Dynamic Reconfiguration Port (DRP). An overall description of the different types configuration bits and the different levels of masking implemented by the ConfigMon FPGA were presented in Section 6.4.3. Very few events were counted that qualified as DRP Scrub events, a total of 22 in all of the characterization testing. The cross-section of these events is thus relatively low, and the onset threshold is in line with the general configuration cell upset onset threshold of the Virtex-5QV device.

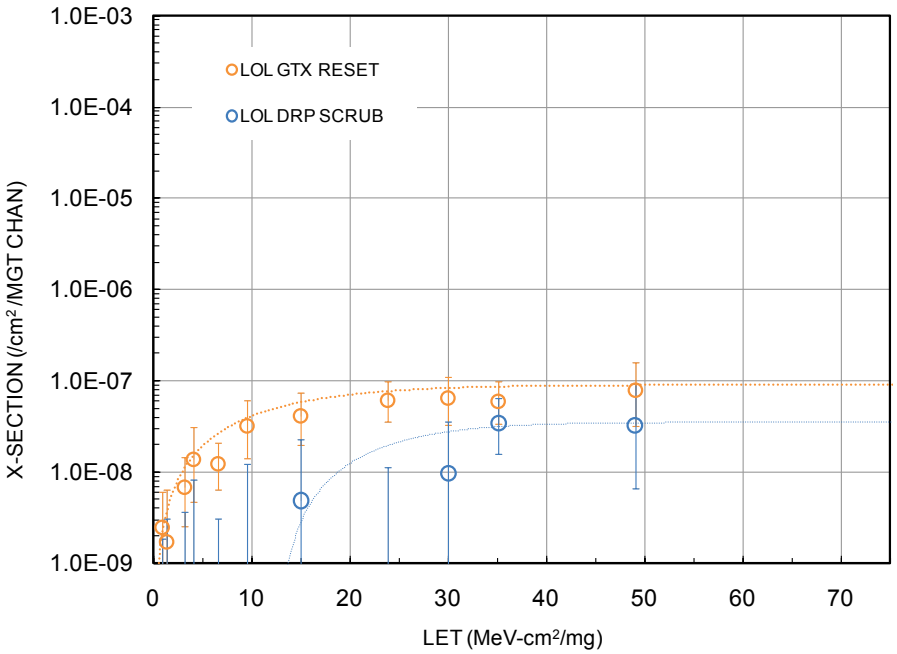

Figure 7-10. GTX Tile Reset and DRP Scrub LOL Events Cross-Sections vs. LET.

8. DATA ANALYSIS

8.1 Bit-Error Duration

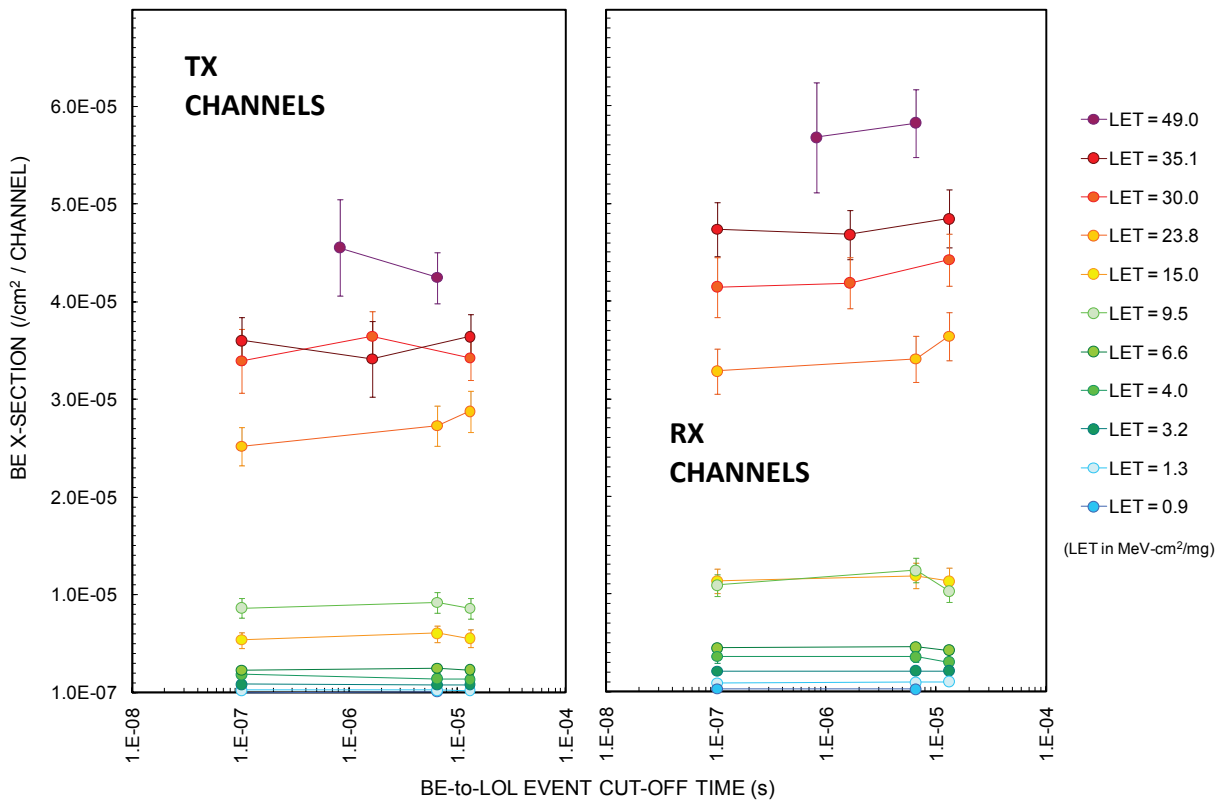

Figure 8-1. BE X-Sections vs. BE-LOL Cutoff Time for each LET.

Several runs were done with different LOL time qualification settings under the same LET, in order to verify that BE events are of a relatively very short duration. Since BE events are completely self-recovering, they are in a different category of precautions to the MGT user and designer. The run parameters used can be seen in Tables A-1 and A-2, where the LOL event time-qualifier ranges from 100ns to 13.1µs (or 8 to 1,024 contiguous 32-bit words in error); the values available for this test variable were shown in Table 3 on page 18. Figure 8-1 shows a plot of the cross-sections vs. LOL-limit for each LET tested with, where it can be seen that the BE cross-section remains relatively constant whether the LOL limits employed were 100ns or 13µs, and across all LETs used. Note that the cross-section vertical axis is in a linear scale, while the LOL-level is in a log scale, in order to visually augment the cross-sectional differences.

This plot is intended to illustrate if any significant changes in the BE event count are taking place. In all cases, the difference in cross-sections between the various LOL levels utilized is never more than ~15% above or below the cross-section at 100ns. This demonstrates that the event cross-section is strongly dominated by BEs with less than 100ns in duration. For RX channels there appears to be a consistent increase in BE cross-section with increasing LOL-level time and at LETs of 15 MeV·cm^2/mg and higher; no such pattern is observed for TX channels. This demonstrates that high LETs can cause completely self-recovering events that can be as long as, or longer than 10µs, only feasible in the RX mechanisms of the MGTs. From a user perspective, these are effectively LOL events, since MGTs employing periodic

resynchronization will be doing so in periodically every several micro-seconds or tens of microseconds, trumping the "self-recovery effect" of these long BEs by initiating resynchronization.

This analysis also supports the hypothesis used in the test approach; the MGT user has to deal with two main types of SEUs, short, less than 100ns, bit-error events that are fully transparent to the transmission mechanisms of the MGTs, and events that are non-transparent to the MGT transmission mechanisms, the LOL events.

8.2 Bits-in-Error per Bit Error Event

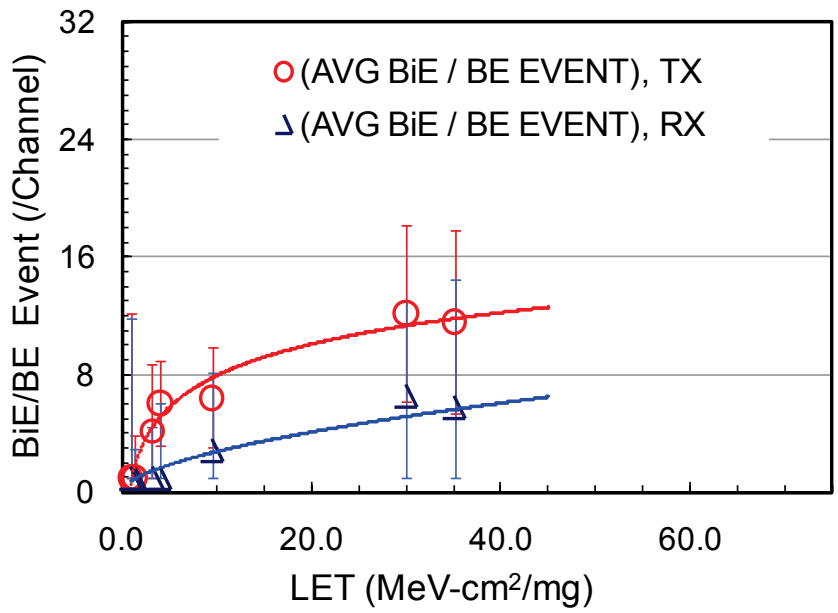

Figure 8-2. Average BiE per BE event vs. LET.

To fully understand the impact of BE events in a system, the average BiE per BE event vs. LET was extracted. Bits-in-Error were accumulated for each test channel and run, and were accumulated while the channel was not in a LOL state. The actual counts of BiE had to be corrected since the accumulation of BiEs was also taking place while contiguous errors from an eventual LOL event were being counted. To do this correction, the BiEs accumulated during LOL determination had to be subtracted. By making use of the expected and received data words captured for each LOL event, the number of bits in error for each LOL event was calculated and then averaged for each run. The 32-bit expected and received data words were actually latched at the instant the erroneous event was deemed a LOL event. By multiplying the number of LOL events for each run, by the number of contiguous words us in the LOL level, and by the average BiE for each LOL event, the number of BiEs due to LOL events is estimated. Only runs with LOL qualification levels of 8 contiguous words (100ns duration) were considered and corrected, since they provide the smallest uncertainty; standard deviation errors were transferred from calculation of the average BiE to the final BiE/BE event average. The formula below shows the final calculation.

$$\frac{BiE}{BE\ event} = \frac{BiE_{raw\ count} - \left(LOL\ Level \times LOL_{count} \times \left\{BiE_{LOL,avg} \pm \sigma\right\}\right)}{BE_{count}} \quad \textbf{(1)}$$

The resulting plot is shown in Figure 8-2, where the BiE per event is shown to be more significant for the TX aspect than for the RX aspect of the MGTs. At lower LETs, a BE event on TX channels will not

cause more than a byte to be in error, while for the RX channels the BiE average is not more than a nibble (4-bits) until LETs of at least 20 MeV·cm^2/mg are reached. For TX channels, at LETs higher than 10 MeV·cm^2/mg, the BiE per event average increases to over a byte, but then appears to reach saturation with LET at a value just under 16-bits. The BiE average value per event for RX channels appears to saturate with increasing LET at less than a byte.
This data verifies the relatively short duration of BE events, causing only a fraction of the parallel word to be in error. It is believed that the BiE average will have some dependency on the line rate of the MGT channel, but since they are events that are transparent to the MGT transmission mechanisms, in a theoretical worst case scenario an increase in line rate would probably only result in an increase in the BiE average. In order to take this into account, during analysis one can deem all 32 bits in error for a BE event, which is an 100% derating factor of the BiE average of a MGT line rate operating at 3.125Gbps.

8.3 Events affecting Multiple MGT Channels

The start time of each LOL event was captured for each channel; analysis of the LOL start times recorded demonstrated several types of simultaneous manifestations on different groups of MGT channels. The maximum envelope for considering shared times was 10us, but in all cases, all channels involved in the simultaneous LOL events never demonstrated start time deltas of more than 320ns. The test setup provided observation on two full tiles and two ½ tiles (i.e. only one lane of the tile was monitored). A multitude of events with simultaneous start times were observed on groups of channels within a single tile, while only five events were observed that involved channels from multiple tiles. For individual tiles, simultaneous channel LOLs were observed in various fashions, on two, three or all four of the MGT channels of the tile, more specifically:

a) The TX and RX elements of one MGT lane of the tile, either Lane 0 or Lane 1.
b) The RX elements in both Lanes 0 and 1.
c) The TX elements in both Lanes 0 and 1.
d) The combination of type a), with either a TX or RX element of the other lane.
e) All four of the channels of the tile.

Manifestations on multiple tiles were grouped separately. For individual tiles, counts were kept for each of the manifestations described above; simultaneous manifestations on 3 and 4 channels were counted together in the same group (items d and e above) for a total of 5 groups. A sixth group tracking the counts of all multiple element manifestations of all types was also extracted.

8.3.1 Multiple-Channel LOLs in a Single Tile.

To understand the impact of simultaneous LOLs on multiple elements on a tile, three more count-groups were created, one to keep track of the counts of the multiple element LOLs of any combination, a second to track single channel RX LOL events, and a third to track single channel TX LOL events. The cross-section per tile is shown in the plot of Figure 8-3 on page 48. Here it can be seen that single RX channel LOL events are the most probable LOL event that will be experienced by an MGT tile. It can also be seen that simultaneous LOLs across multiple channels and lanes in a tile are just as probable as LOLs on a single TX channel of the tile. Figure 8-4 on page 48 shows the cross-sections with the different types of simultaneous manifestations. The more probable manifestation is for all 4 channels of the tile to be affected simultaneously, followed by LOLs where only both of the RX channels in each lane are affected. Also measured, but much less probable, are LOL events where both the RX and TX channels of a single lane are affected, and when both TX channel of the tile are affected. For convenience, these types of simultaneous LOL events will be referred to as a Multiple-Element Upset, or MEU LOL events.

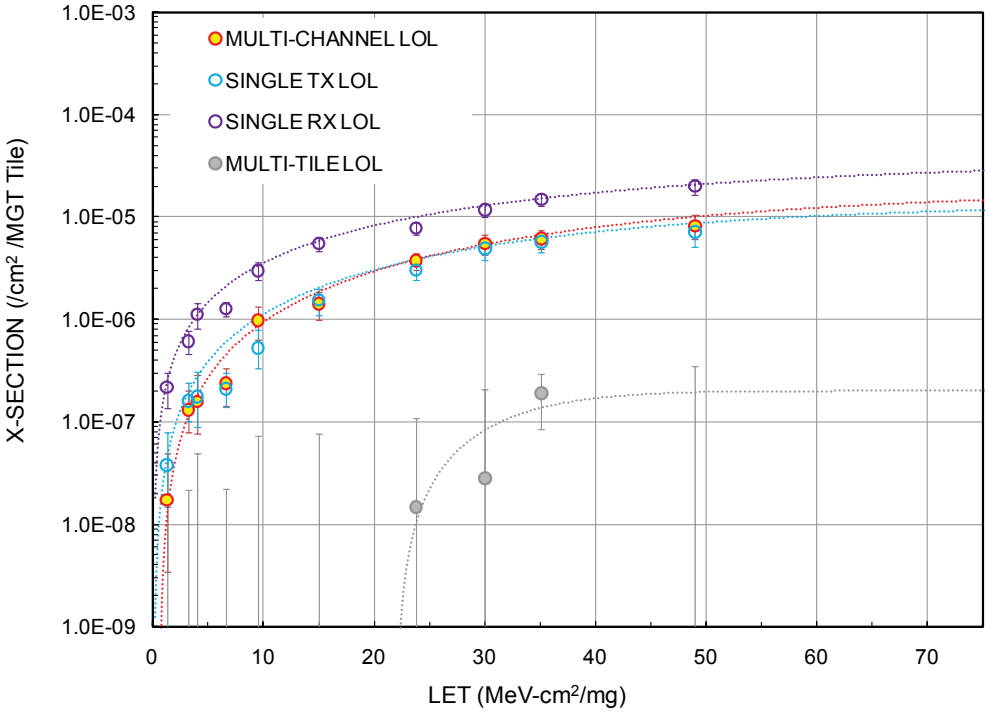

Figure 8-3. Cross-Section vs. LET for Multiple Channel, Single TX and RX, and Multiple Tile LOL Events observed on a single MGT tile.

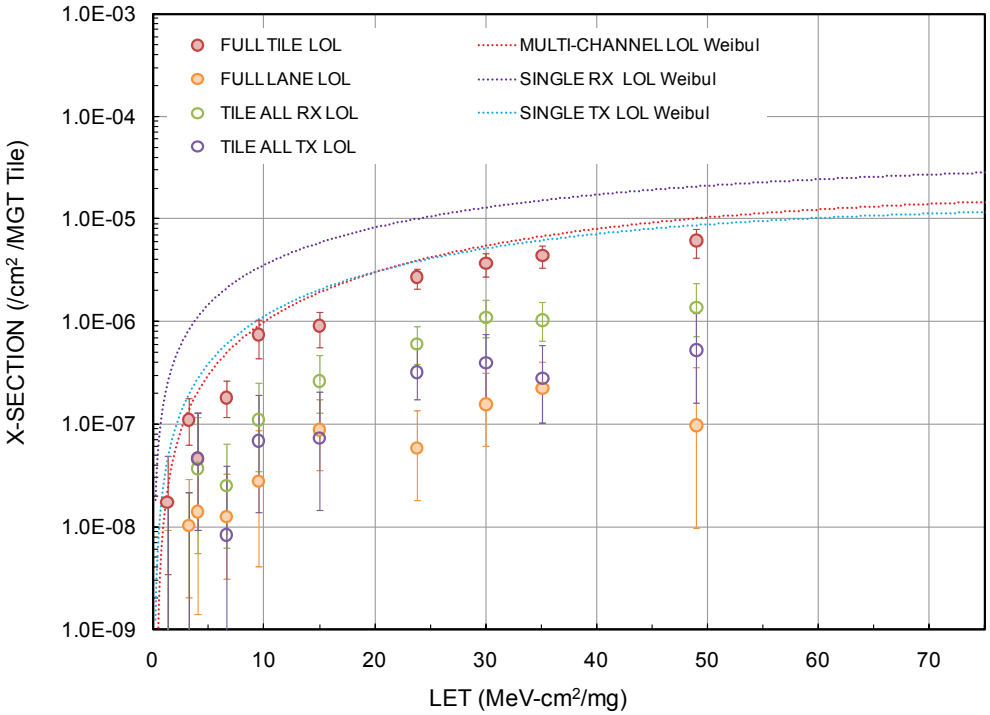

Figure 8-4. Cross-sections vs. LET for the vairous multiple-channel LOL manifestations.

The recovery mechanisms required for the channels involved in MEU LOLs were varied; a large proportion of the events recovered with resynchronization, but in many occasions, some of the MEU channels required a particular re-initialization resets, and some even required full tile resets. The duration of the LOL events in MEUs will be discussed in more detail in Section 0. The distribution of the recovery mechanisms across the channels involved in the MEU is mostly dominated by events where all of the involved channels recover with resynchronizations, as is shown in the illustrations of Figure 8-5. Here, a sample of the shorter MEU manifestations observed is illustrated by diagrams of MGT tiles suffering MEUs, where all channels shown recover with resynchronization unless indicated. The bars are scaled and represent the duration of each channel's LOL event in the MEU. Channels with no LOL bar, where not affected by the MEU. Note the start delay of the RX channel LOLs for each MEU; the delay is due to the latency in the interleaving system, where corrupted data on the RX channel physically needs to loop-back through the DUT FPGA before being verified at the Service FPGA. The variations in RX channel start latency, in the range of 170ns to 320ns, indicates that the RX channel can be impacted by the event causing the MEU at different points of the MGT RX circuitry chain, which can include the PMA, the PCS and the fabric interface of the macro (for an MGT tile diagram, reference Figure 5-2 on page 13). No cross-sections were calculated with respect to the recovery mechanisms of MEU LOLs, since all LOL events are included in the cross-sections of Section 7.2.2.

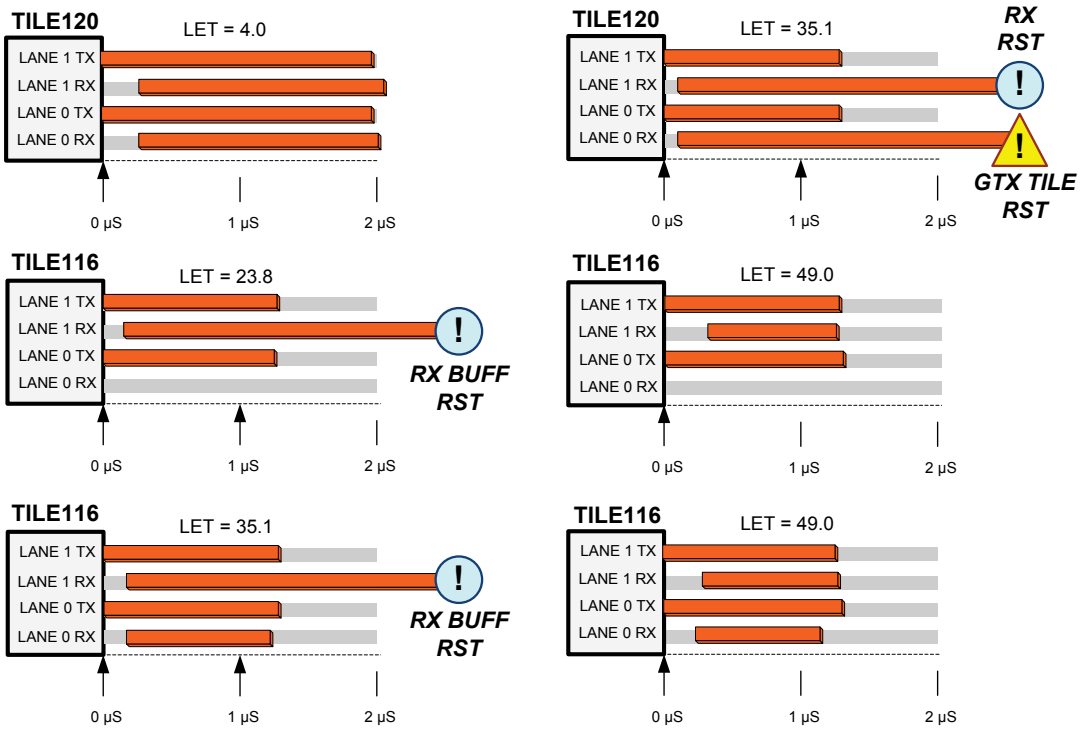

Figure 8-5. Illustration of several MGT Tiles suffering Multiple Element Upset (MEU) events; bars are used to represent the LOL event on each channel.

8.3.2 Multiple-Channel LOLs in Multiple Tiles.

A total of seven LOL manifestations were seen that involved multiple channels across different tiles throughout the course of the testing. The cross-sections obtained were shown in the plot of Figure 8-3 on page 48. As the plot shows, multi-tile MEUs demonstrated a high LET threshold and low saturation cross-section, (note that the cross-sections of ~2E-7/cm^2 is per tile). Figure 8-6. Diagram illustrating MEU events with LOLs on channels of multiple tiles.Figure 8-6 on page 50, illustrates three of the multi-

tile MEUs observed, whose duration was relatively short, and with all channels recovered by resynchronization. The dashed traces are used to represent channels that weren't being monitored, or whose data was corrupted by oscillatory-events and discarded. Tile 120 is highlighted in blue to indicate that it's the tile providing the reference clock to the other MGT tiles shown.

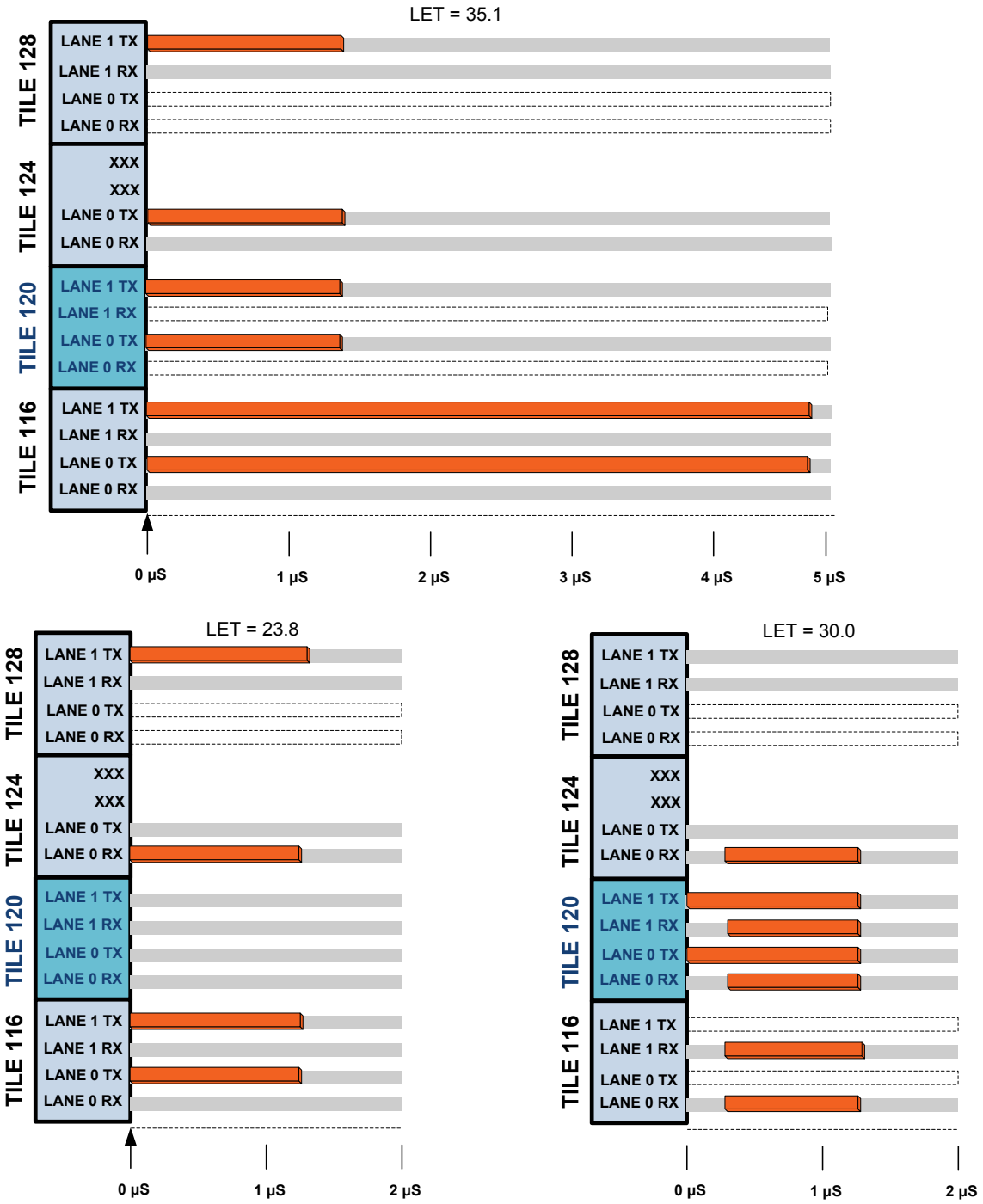

Figure 8-6. Diagram illustrating MEU events with LOLs on channels of multiple tiles.

Of much interest is the event depicted in the bottom right diagram of Figure 8-6, giving the impression that the channels suffering LOL have the MGT clock reference Tile 120 as their SEE epicenter. Also of note here are the long RX latency delays, indicating that the MEU LOL event affected the RX channels at or very near the PMA portion, since the RX detection delay length is one of the longest observed. This is also not that surprising since at the MGT PMA is where SET-like corruptions of the source clock might be more persuasive.

Another type of multi-tile MEU, not illustrated in Figure 8-6, also showed full recovery with resynchronization. This MEU event was actually observed 3 times in a single run, each event lasting 608, 646 and 629 milliseconds, and affecting every RX channel monitored (Run 74, March-2009). These events, with such peculiar RX manifestation, and all occurring within a single run, appear to be an artifact of a bit-upset in one of the DRP analog settings of the source clock tile, where a tolerance threshold is in the brink of violation. Scrubbing of DRP bits was only executed when channels went down indefinitely. The final event, also not illustrated, brought down all 12 test channels and required a manually induced DUT DCM reset command to recover them. This situation is believed to be created by an event on the MGT reference clock distributed by Tile 120, which a DCM also uses as a reference. The DCM-MGT interaction is shown by the diagram in Figure 6-12 on page 27. Such an event is believed to be caused by corruption of either the reference clock signal directly, or since multi-tile MEUs have such a high LET threshold, the temporary corruption of a particular configuration setting that is not protected by the ion mask, and that defines the reference-clock output to the DCM on the fabric. Whatever the source, it caused the DCM, which is behind the ion mask, to lose lock to its reference clock indefinitely.

8.4 LOL Event Duration Spectrum

For each MGT channel monitored, the time of duration was captured for each LOL event. The spectrum of the LOL event durations from 0 to 20 seconds can be seen in Figure 8-7 on page 52, where each event for TX channels, RX channels, and the channels involved in a tile-MEU LOL, are binned by milliseconds. Each LOL event had to be corrected for the LOL level used in the test, and for the minimum number of comma characters required to deem a LOL channel in sync. During the testing, events that did not recover before 8 or 9 seconds were deemed non-self-recoverable, irradiation was halted, and the manual stimulus procedure applied; all the events that auto-recovered (either by resynchronization or re-initialization stimulus) were observed to have done so by at least 10 seconds. In Figure 8-7, the period of the auto-stimulus (0.512 to 1.536 seconds) applications is highlighted; events in this region were counted in the respective recovery stimulus count. This is indicated by the arrows labeled a, b, c, d and e in Figure 8-8, which shows the distribution of LOL events from 0 to 2 seconds. Here, the plot illustrates how the different reset stimuli recover the affected channels. Table 13 shows the stimulus list, and time of application.

Table 13. Channel-Level automatic stimuli.

Label	Reset Stimuli	Time of application
A	DUT RX Buffer Reset	512 ms
B	DUT RX Reset	766 ms
C	DUT RX CDR Reset	1,024 ms
D	DUT TX Reset	1,280 ms
E	Service RX CDR Reset	1,536 ms

Resynchronization-recovered events, were either short (< 1 ms), or “long-lasting” events, which for all but a couple of cases, were only observed on RX test channels. And, while these long-lasting RX resynchronization events are random in duration, they appear consistently, with durations starting at

around 100ms and lasting 8, 9 or 10 seconds; beginning to dwindle in numbers after approximately 6 or 7 seconds. After 8 seconds, the count of this type of events may have been corrupted by manual-reset events. The cross-section of these events was extracted and is shown in Figure 8-9 on page 53. As can be seen in Figure 8-8, the random duration, RX channel re-sync LOLs were also present during the stimulus recovery period.

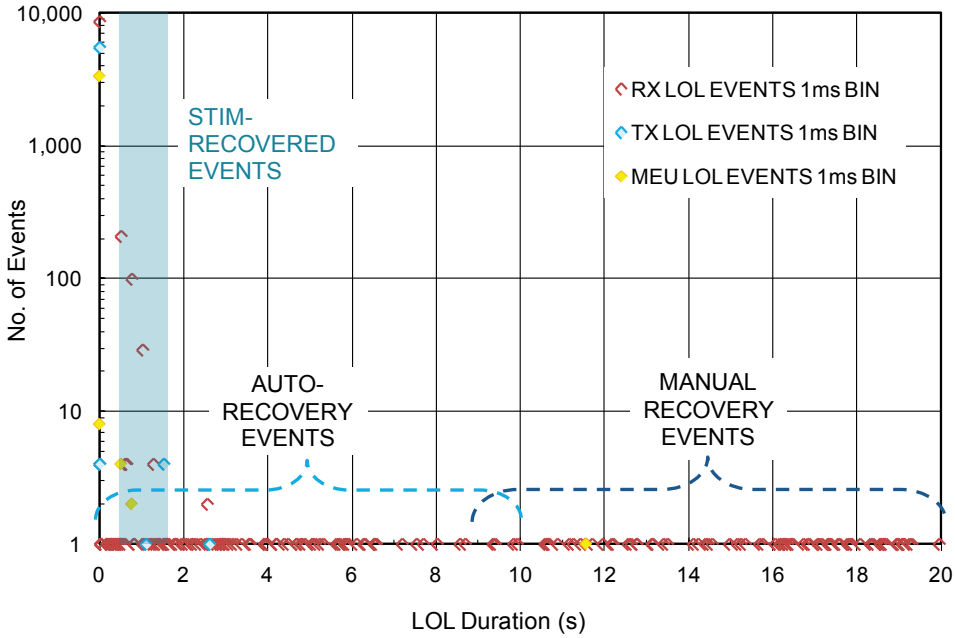

Figure 8-7. LOL duration spectrum, first 20 seconds.

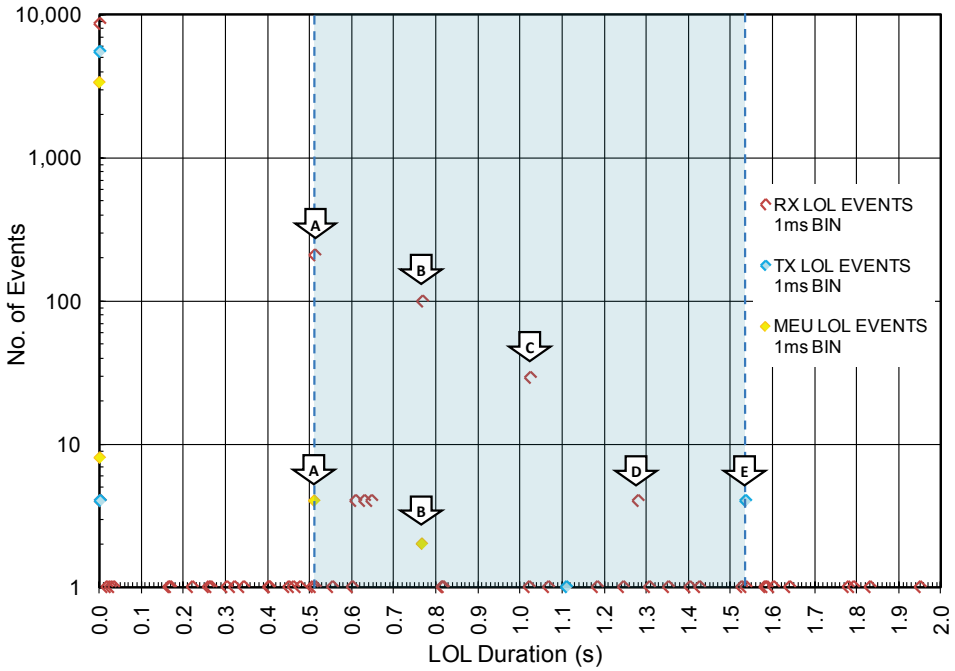

Figure 8-8. LOL duration spectrum, first 2.0 seconds.

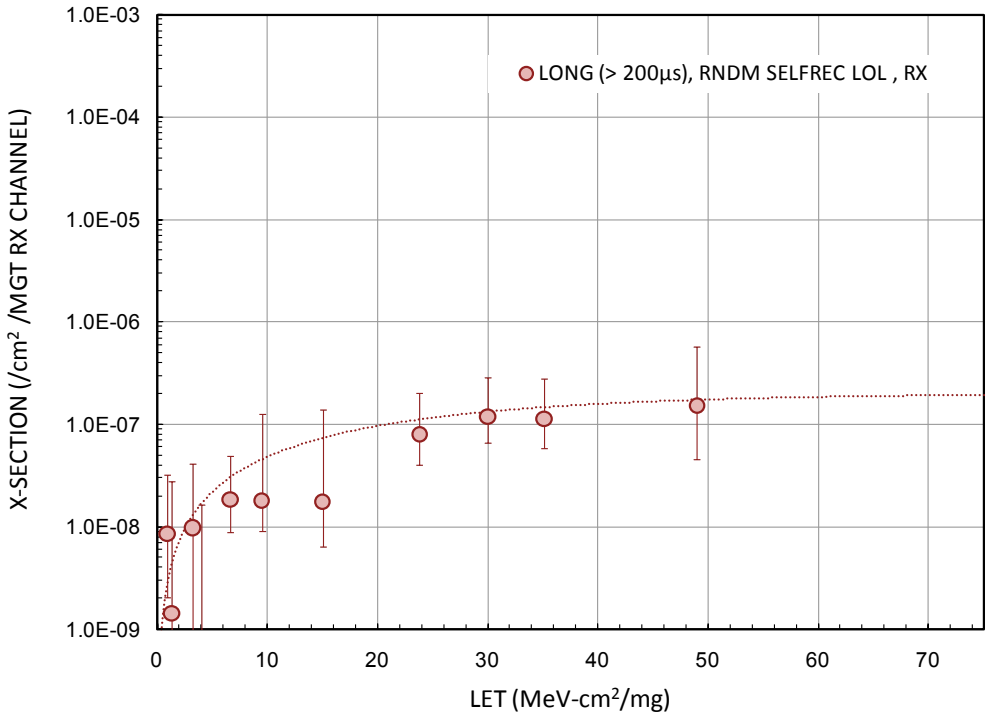

Figure 8-9. Cross-section vs. LET for Long-lasting, > 1.5 seconds, LOL events on MGT RX channels.

In a handful of occasions, RX channel LOL events were recovered by resetting the TX MGT of the loopback path, which is hidden by the ion mask. This can be seen by the arrow labeled D in Figure 8-8; indicating that there are events that corrupt the RX MGT parallel outputs in such a way that the downstream element needed resetting. This is appears to be an artifact of the particular test design used, which could potentially also be found in other designs. Also of interest are the repeatable events observed in Figure 8-8, where in between 600 and 650ms four events were observed, in the same millisecond, three times. This is the multi-tile event described in Section 8.3.2.

Figure 8-10 on page 54 shows the spectrums for 10ns and 10µs bins, over the first 10µs (A), 100µs (B), and 500µs (C) of the LOL event. For RX and TX channels alike, the more repeatable, and thus most probable LOL event to be experienced, is a relatively short event, lasting somewhere in between 1.10 and 2.19µs, and statistically peaking at 1.26µs, as can be seen in plot (A) of the figure. The repeatability of events longer than 2.19µs decreases significantly, from the thousands to the hundreds, regardless of duration signature. In the spectrum plot of Figure 8-10 (B), RX channel event durations are seen to decrease in repeatability up to 60us, while for TX channels no repeatable event durations were observed beyond 25µs. In Figure 8-10 (C) illustrates another very well defined event duration signature, lasting in between 140 and 170us for TX channels, and between 170 and 200µs for RX channels. In all of the plots of Figure 8-10, the MEU event count appears plausible on all event duration centers for RX and TX channels. Beyond the 200µs LOL event duration, the only events with repetition that were observed, were the events corrected by the auto-stimulus, as can be seen in Figure 8-8 and Figure 8-7.

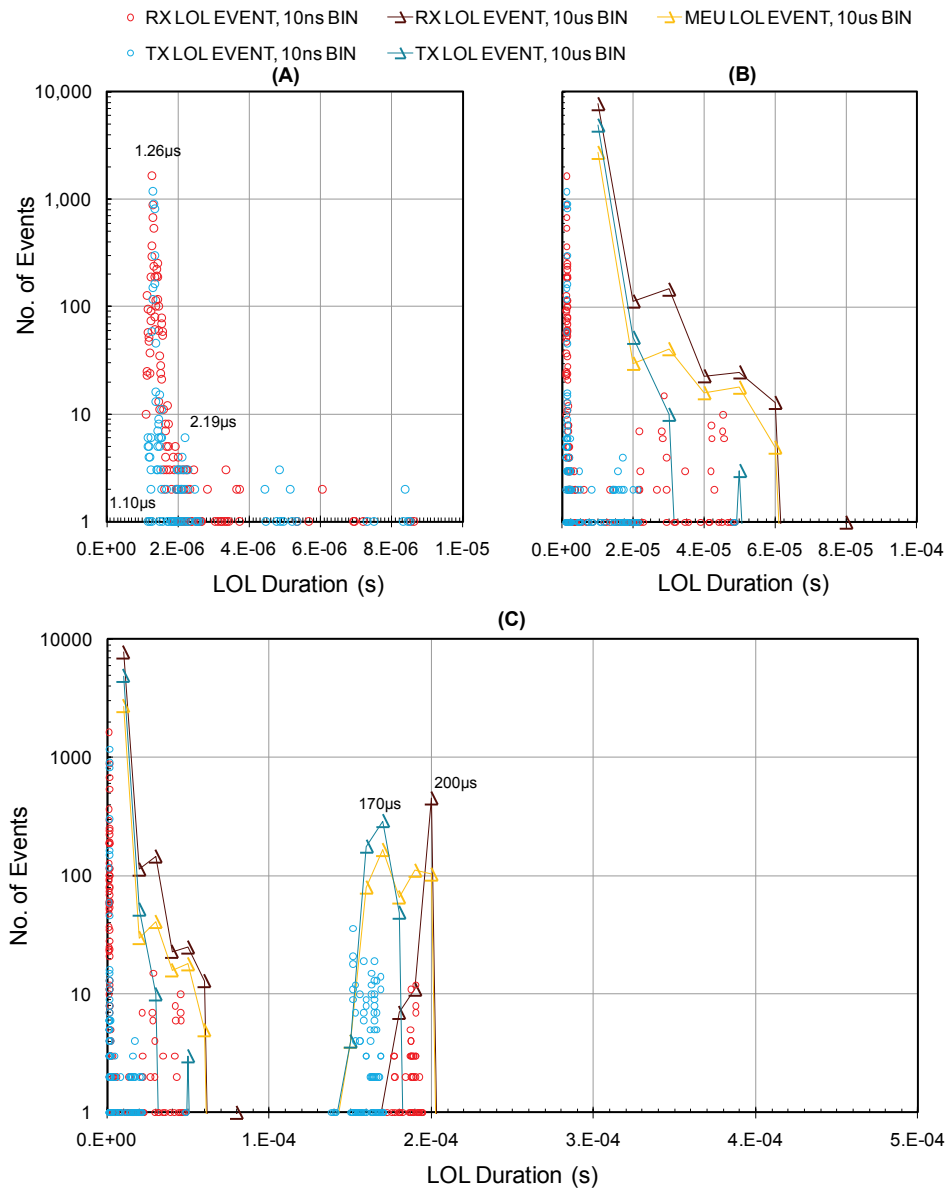

Figure 8-10. LOL duration spectrums for durations up to 10µs (A), up to 100µs (B), and up to 500 µs (C).

8.5 MGT Current Measurements

Current measurements were obtained for each tile in the fashion described in Section 6.2.3 during the March 2010 TAMU experiments. The current level consumed by MGTAVCC, MGTAVCCPLL and MGTVTTTX for tiles 130, 126, 122 and 118, captured every 990µs during each run. Each current level was analyzed for significant changes, and none were observed at LETs of 10MeV·cm^2/mg; at LETs of 49.0MeV·cm^2/mg, actual changes in the current levels were seen, but were still insignificant. Figure 8-11 on page 55, shows the MGTAVCC and MGTAVCCPLL current consumption for Tile 118 through an irradiation run, superimposed on the current chart are the LOL status of the channels of the tile, as well as

an indicator for when the irradiation beam was active and inactive. As it can be seen, no current changes were observed even though individual channels and the entire tile were suffering LOL events, some even requiring a tile reset.

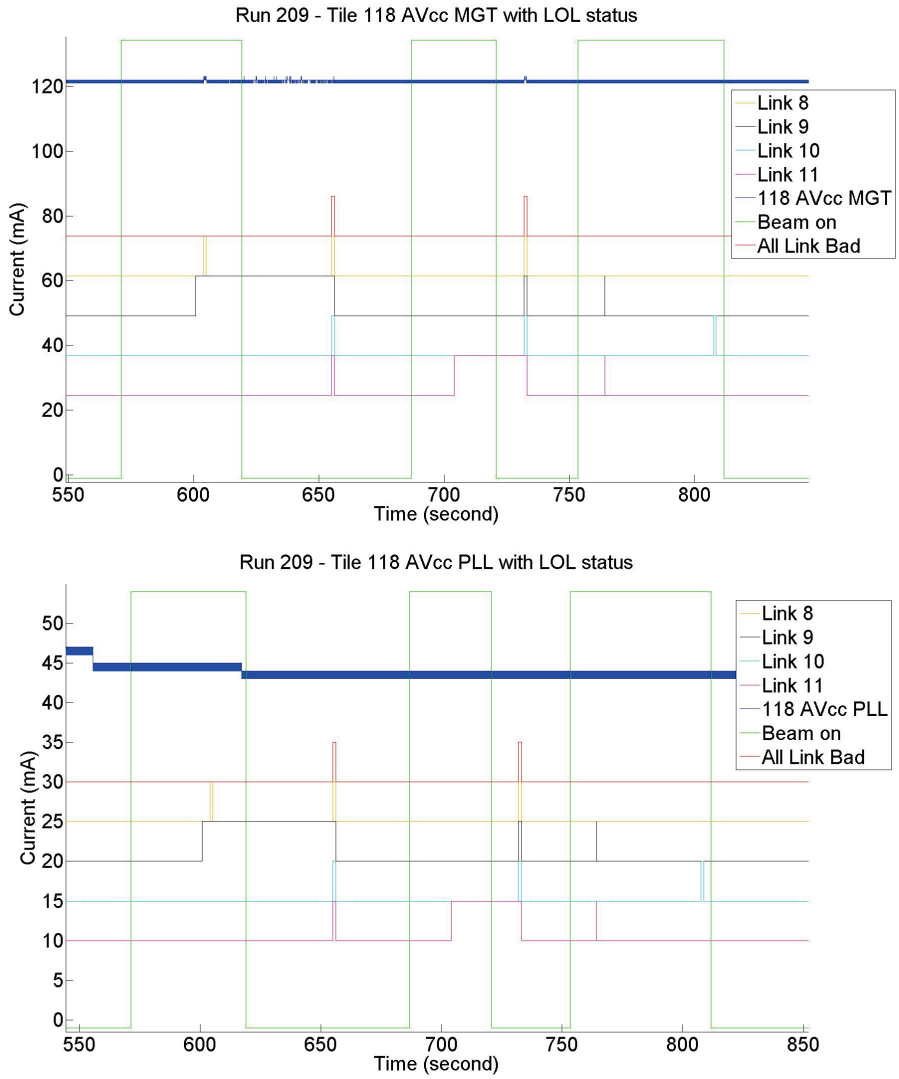

Figure 8-11. AVCCMGT (top) current and AVCC-PLL (bottom) current consumption and channel LOL status strip charts for Tile 118. (LET = 10.0MeV·cm^2/mg, Ion = Ar, Flux = 1.44E+5·p·s/cm^2).

In Figure 8-12 on page 56, the LET is increased and more interesting behavior can be observed on the MGT AVCC and AVCCPLL currents. Very short duration current drops are observed in the AVCC, and a jump in current is observed in the AVCCPLL current. The jump in the AVCCPLL current is more than likely due to a particle-induced DRP configuration change, inconsequential to the design functionality and thus unnoticeable, but not being scrubbed during the test. The short, down-ward spikes in the AVCC current, are well within the MGT specification, and are believed to be due to artifacts of the interaction mechanisms of the incident particle causing LOLs and BEs in the channels and tile. In one instance a LOL on channels 10 and 11 coincides with a 35mA down-ward spike on the current.

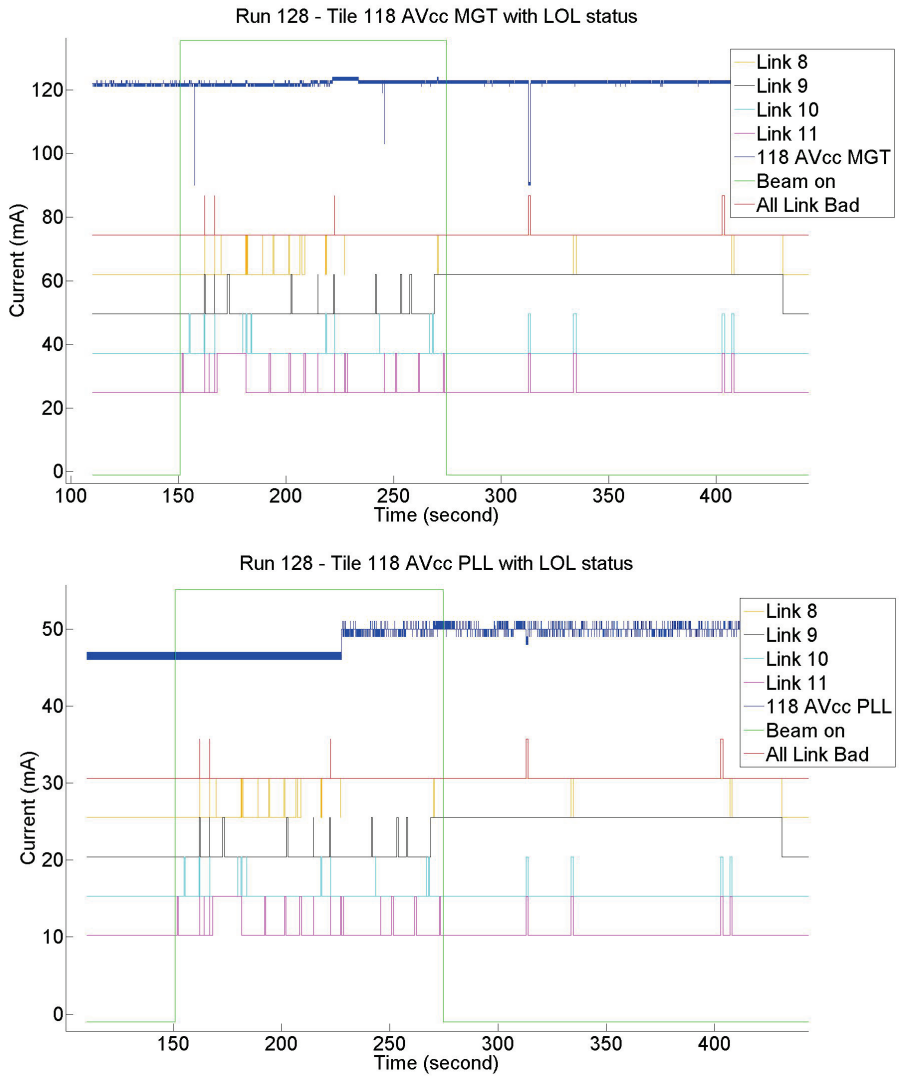

Figure 8-12. AVCCMGT (top) current and AVCC-PLL (bottom) current consumption and channel LOL status strip charts for Tile 118. (LET = 49.0MeV·cm^2/mg, Ion = Xe, Flux = 1.44E+5·s/cm^2).

8.6 On-orbit Rate Estimates

Each event's cross-section that has been characterized by this test is listed in Table 14 on page 57. The worst-case environment to analyze heavy-ion upset rates is in the orbits outside of the Earth's magnetosphere, such as interplanetary space and geo-synchronous orbits. The proton belts that make up the magnetosphere shield the Earth and any spacecraft from many of the energetic heavy ion particles which are generated by galactic cosmic rays, solar-flares and other deep-space sources. CRÈME-MC was used to generate the rates, and the parameters used are listed in Appendix B. All events are shown to not occur more than once a decade. The most susceptible event being RX channel and TX channel Bit-Errors (one event every 4.9 and 12.8 years respectively). Missions that intended to use MGTs in proton-rich environments, can use the resources found in (9) and (10) to estimate the impact of protons on the orbit upset estimates, particularly for SEE types with an LET threshold less than 15 MeV/cm^2·mg.

Table 14. Events Characterized, their Weibul parameters, and the on-orbit rates generated by CREME-MC.

EVENT TYPE		UNITS	WEIBUL PARAMETERS					EVENT RATE (/DAY)	DAYS	YEARS
			LET_{th} (MeV-cm²/mg)	W (MeV-cm²/mg)	S	SAT X-SEC (/cm²)	SAT X-SEC (/µm²)			
TX BE		/CHANNEL	0.01	23	1.93	4.46E-05	4460	2.13E-04	4,684	12.8
RX BE		/CHANNEL	0.01	36	1.39	7.42E-05	7420	5.58E-04	1,790	4.9
TX LOL :	TOTAL	/CHANNEL	0.01	43	1.56	1.57E-05	1570	6.03E-05	16,581	45.4
	RESYNC	/CHANNEL	0.01	37	1.58	1.27E-05	1270	5.47E-05	18,297	50.1
	RE-INIT	/CHANNEL	0.01	2.8	0.9	1.70E-08	1.7	6.21E-06	161,031	441.2
RX LOL :	TOTAL	/CHANNEL	0.01	66	1.42	3.90E-05	3900	1.19E-04	8,402	23.0
	RESYNC	/CHANNEL	0.01	74	1.38	3.80E-05	3800	1.14E-04	8,774	24.0
	LONG RESYNC	/CHANNEL	0.01	28	1.25	2.00E-07	20	2.77E-06	361,406	990.2
	TOTAL REINIT	/CHANNEL	0.01	37	1.17	8.50E-07	85	1.20E-05	83,018	227.4
RX REINIT LOL :	RX BUFFER RESET	/CHANNEL	0.01	24	1.31	3.10E-07	31	4.38E-06	228,487	626.0
	RX RESET	/CHANNEL	0.01	13	1.92	1.10E-07	11	9.42E-07	1,061,828	2,909.1
	RX CDR RESET	/CHANNEL	2.5	7	1.22	2.20E-08	2.2	8.43E-08	11,862,579	32,500.2
TILE LOL:	GTX TILE RESET	/CHANNEL	0.01	14.5	1.33	9.00E-08	9.0	2.10E-06	476,349	1,305.1
	DRP SCRUB	/CHANNEL	12.5	13	1.5	3.50E-08	3.5	6.82E-09	146,545,483	401,494.5
MULTIPLE MGT:	SINGLE TX	/TILE	0.08	48	1.55	1.30E-05	1300	3.69E-05	27,125	74.3
	SINGLE RX	/TILE	0.03	58	1.31	3.75E-05	3750	1.80E-04	5,548	15.2
	MULTI-ELEMENT	/TILE	0.6	55	1.66	1.81E-05	1810	2.42E-05	41,346	113.3
	MULTI-TILE	/TILE	22	12	1.56	2.00E-07	20	2.84E-08	35,221,313	96,496.7

9. SYSTEM IMPACT

The impact of SEEs on the MGT communication system is directly proportional to the duration of the negative effect. The amount of corruption that the negative effect causes on the MGT function is strongly dependant on the line rate, the FPGA interface width, the MGT configuration profile, the number of susceptible devices peripheral to the MGTs, and most importantly of all, the serial communications protocol. The configuration profile of the MGT includes the configuration of the DRP system, and susceptible peripheral devices include any DCMs, PLLs, clock buffers and trees in the FPGA; and clock-sources and MGT power regulators outside of the FPGA. Communication protocols were presented in detail in Section 5.1. For the system utilized for the testing, the line rate used was 3.125Gbps, the FPGA interface 32 bits, and it employed a DCM to divide the MGT-driven XCLK to obtain the parallel clock. The GTX tile instantiation code is shown in Appendix D. The protocol utilized for the test is described in detail in Section 6.1.

9.1 MGT Configuration SEEs

The impact of MGT configuration bit upsets on the system, fabric or DRP, is dependent on the design instantiation. Test-bench and SW tools like fault-injection should be used to identify the configuration susceptibility profile of each design.

For this test, the impact of the configuration bit upsets on the MGTs is included by the results of the characterization. This was achieved by periodic and continuous read-back and frame-based scrubbing cycles taking place. Any configuration upset that would negatively affect the test design was demonstrated to be, 1) recoverable with the methods shown here, and 2), to posses upset characteristics that can be categorized within the intrinsic SEE manifestations. Some of the extremely rare events observed, like long ReSync manifestations on multiple-tiles, and the one or two randomly long MEU or single TX channel events, are more than likely induced by a configuration related upset. The configuration profile difference in between a MGT-based FPGA design and the MGT test described here is not expected to be very significant when only looking at the MGT tiles themselves. Major differences are expected when comparing the overall design since that comparison would include all the glue logic, which for this test design is minimal.

9.2 MGT SEEs

9.2.1 Bit Errors

Bit Errors (BE) have been observed on RX channels and TX channels, the number of bits affected by the SEE is always less than 16-bits at a worst-case. The impact of the BE on the communication system depends on where in the data packet sequence the event took place. A BE could occur while the channel is transmitting:

- Packet user-data, resulting in corrupted bits in the payload data,
- Packet control-data, at the packet's head or tail, resulting in lost or scrambled packets, or
- Inactive idle characters, in the periods in between packets or frames, with no impact.

If there's an under/over-laying protocol, the particular section of that packet sequence could also be affected in the same fashion as described above.

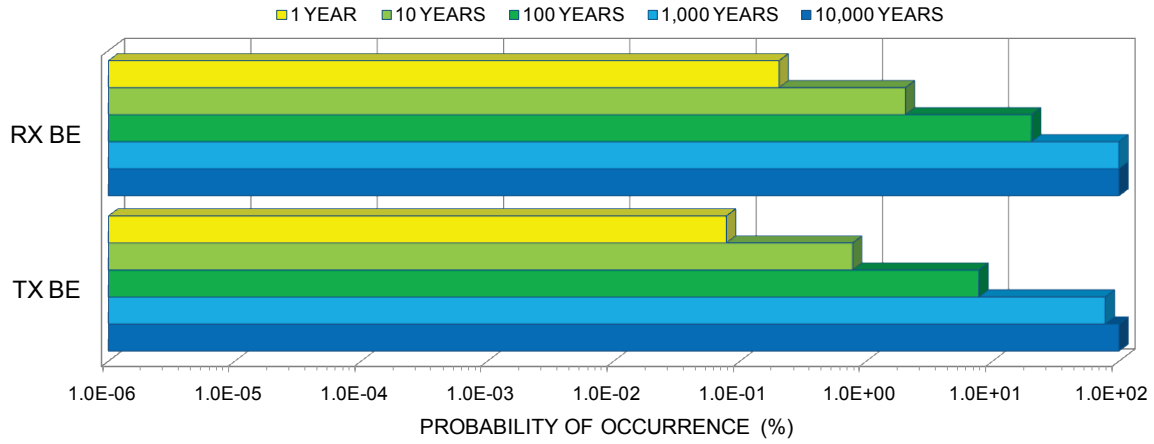

Figure 9-1. Probability of occurrence of Bit Error Events.

MGT protocols employing guaranteed TX and RX delivery verification will resend any lost or corrupted data packets, with virtually no impact to the system's band-width. MGT systems with no such-verification will lose the entire data of the lost packets, or just the particular bits of the payload. RX channels have been shown to be subject to longer-lasting BEs and these would corrupt any transmission that is taking place during the length of the event. The increasing length of these particular BEs gives them a higher chance of scrambling and losing packets versus just corrupting the user/payload data of a packet. From the estimates, in a one year geo-synchronous mission, the probably of this event happening to MGT TX and RX elements is 0.07% and 0.2% respectively. This is shown in Figure 9-1.

9.2.2 Resynchronization Loss-of-Links

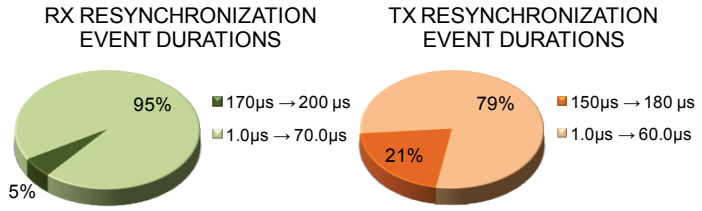

Figure 9-2. Resync-event duration probability for RX and TX channels.

Events requiring resynchronization of the affected channel were observed for TX and RX functions. Two duration centers for these event types were observed, the more common was around 1 to 70µs, for both TX and RX channels, and less frequent ones were observed at 170µs for TX channels, and 200µs for RX channels. The probability of occurrence of one duration type vs. the other is shown in Figure 9-2. RX channels could also be subject to a long-lasting event of random duration which may require the MGT up to 10 seconds to recover from, the cross-sections for these events has been measured separately. In all cases, the channel cannot be recovered until the event's effect has completely dissipated and the channel is resynchronized.

The impact of these types of events will depend on the protocol type, the line rate and the packet size. Assuming typical sizes of 2kB packets and a 3.125Gbps line rate:

- 1 to 70µs events will result in one to ten lost packets,
- 170 to 200us events will result in 26 to 32 lost packets, and
- Long lasting events of random size will result in a directly proportional amount of lost packets.

As with BEs, protocols with delivery verification, and with resynchronization activity in between packets, should be able to re-transmit all of the lost packets, with minimal bandwidth impact since the probability of occurrence is so small. Protocols with resynchronization activity between packets but with no delivery verification, will simply loose all of the data in the packets affected. Theoretical protocols with no resynchronization activity in between packets will be locked indefinitely. In a geosynchronous mission, the shorter TX and RX resynchronization LOL events have a probability of occurrence in a one year mission of 0.02% and 0.05% respectively, as is shown in Figure 9-3 on page 59. The probability for each type of short resync event duration can be extracted by adjusting the overall probability for each of the event duration types. For example, the probability of a TX channel suffering a 170µs Resync event during a year in a geosynchronous orbit is 0.0042% (0.02 x 0.21; values extracted from Figure 9-2 and Figure 9-3), while for a 1.0 to 60µs duration resync event, its 0.0158%. The probability of the long lasting event of random duration observed in RX channels is less than 0.001% in a one year mission and less than 10% in a theoretical 10,000 year mission. It is not unlikely for this type of event to never be observed.

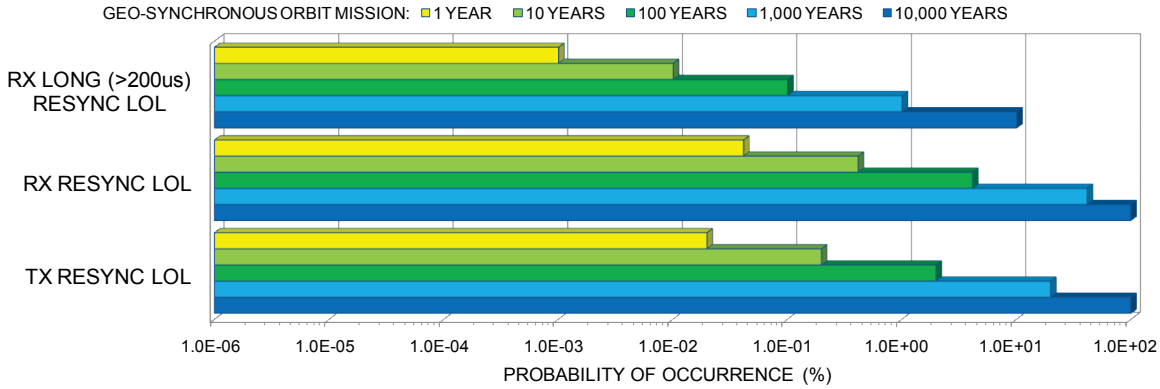

Figure 9-3. Probability of occurrence of Resynchronization Events.

9.2.3 Channel Re-initialization Loss-of-Links

Events requiring re-initialization of the channel have been observed on both RX and TX channels. For TX channels, the re-initialization was required at the interface RX MGTs, while for RX channels, the re-initialization was required on the RX MGT element itself. The duration of these events depends completely on the time it takes the protocol or the design to detect the condition and initiate the re-

initialization sequence. Protocols with delivery verification usually employ a time-out or watch-dog system to re-initialize afflicted channels that are not responsive. A protocol can be built with re-initialization sequences in between packets, eliminating the need for detection systems. Under all cases, the channel will not recover until the event has dissipated and the re-initialization is initiated one way or another. The key to then minimizing this impact is fast recovery.

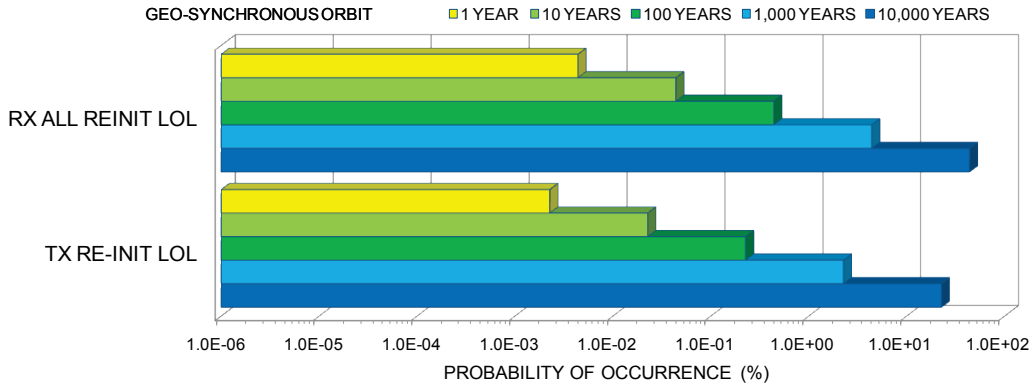

Figure 9-4. Probability of occurrence of channel Re-Initialization Event.

In a one year mission, the probability of RX channels requiring a re-initialization is about 0.05%, while for TX channels is 0.02%. In section 7.2.2.2, the different types of re-initialization signals required to recover from these types of events were presented. For simplicity, the RX CDR Reset and TX Reset should be employed for re-initialization operations, since they encompass all of the channel-level possibilities (reference Figure 6-5 on page 19). If using a combination of periodic re-initialization and re-initialization upon detection, a design could employ the least impacting reset, the RX Buffer Reset periodically, and the RX CDR and TX resets upon detection. Events that recover with simply the RX Buffer Reset signal have a much larger probability of occurrence in a year in orbit, as is seen Figure 9-5; so if a re-initialization event occurs it will more than likely be recovered with an RX Buffer Reset command. The probability of a channel requiring an RX Buffer Reset in a year is 0.002%, decreasing to 0.0003% and 0.00003% for the more impacting channel-level resets.

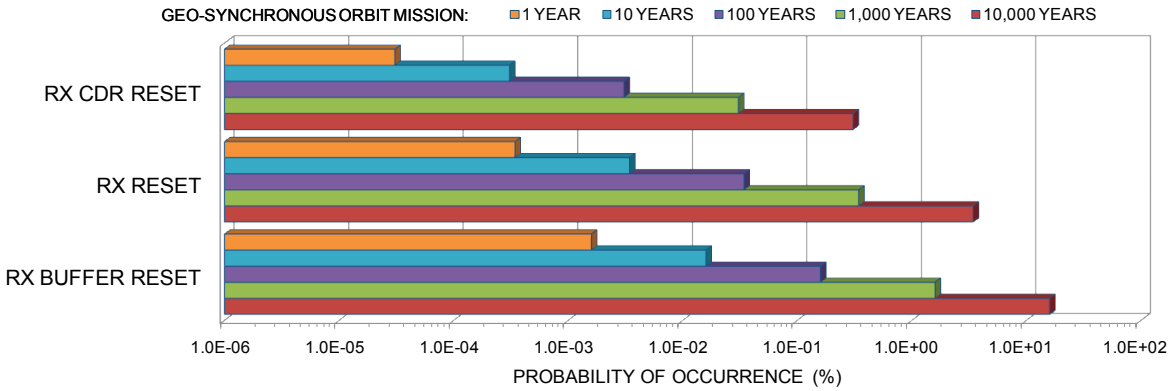

Figure 9-5. Probability of occurrence of different types of RX re-initialization events.

9.2.4 GTX Tile Re-initialization Loss-of-Links

Events were observed that required a MGT tile-level reset (GTX Reset), this type of re-initialization is very impacting, since it affects all 4 of the channels of the tile, and can take milliseconds to recover from (11). These events were only observed for RX channels, and have a very low-rate of probably. These

events will disable the particular MGT channel until the GTX reset is activated. This re-initialization action appears to be more suitable for a detect-and-actuate mitigation system; since it is the lowest-level reset that can be actuated and brings down 3 other channels for a longer period of time. The probability of this event occurring in a year is less than 0.001%, and sis till less than 10% after a theoretical 10,000 years on orbit, as is shown in Figure 9-6. There's a good chance this type of event may also never be seen by a system in orbit.

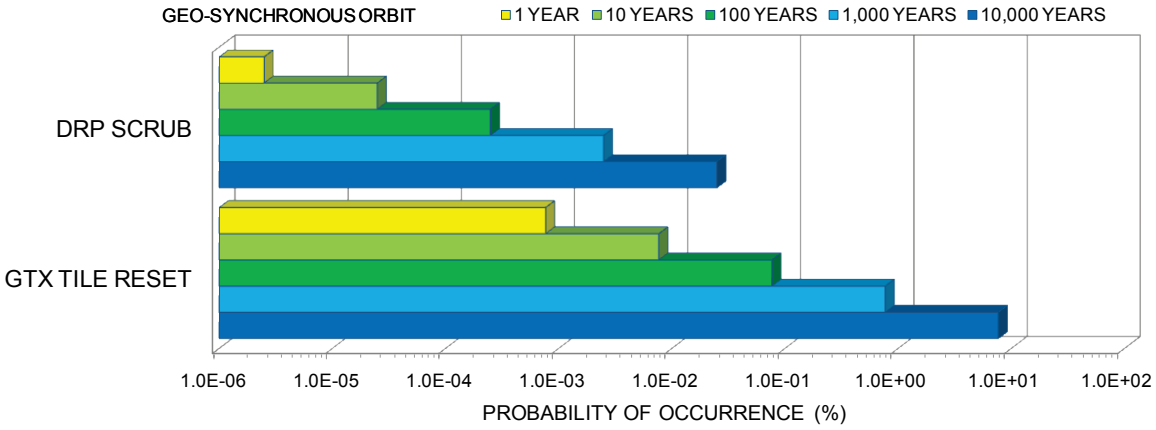

Figure 9-6. Probability of occurrence of tile-level re-initialization events.

Another type of event that is highly impacting but of extremely low probability is one that require a scrub of the MGT tile's DRP system. If such an event were to occur, the only way to recover would be to correct the corrupted bit of the DRP system, or to re-configure the device. The probability of these events occurring is so low, (0.002% in 10,000 years) that it may not be worth-while to mitigate. However, the DRP system can be very attractive to a fully reconfigurable communication system, where periodic scrubbing of the DRPs may be a not very expensive feature to design. It must also be noted that the DRP susceptibility is dependent on the particular MGT tile instantiation; the DRP susceptibility profile is not expected to vary much from design to design. Bench top techniques like fault-injection or analysis can be used to determine the DRP-corruption susceptibility of the MGTs in a design.

9.2.5 Multiple Element Upset (MEU) Resynchronization and Re-Initialization LOLs

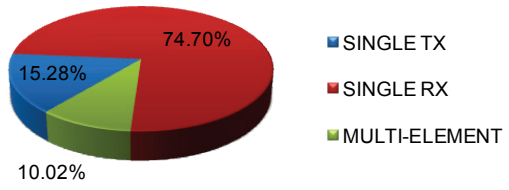

Figure 9-7. Ratio of MEU events vs. single events for TX and RX channels.

All of the events characterized and examined have been done on a per channel basis, but many of these events were coincident with events in other elements of the MGT tile that was suffering the ReSync or ReInit LOL event. These events are referred to as MEU events, and may be a concern when utilizing primary and redundant MGT channel systems, triple-redundant channels, and channel bonding systems. Particularly if both, primary and redundant channels or 2/3 of the triplicated channels share a tile.

The probability of MEUs has been extracted by comparing events on single TX and RX channels to event on multiple channels within a single tile. The ratio of occurrences is shown Figure 9-7. In the same way that was demonstrated in Section 9.2.2, the probability of having LOL events affect multiple channels at once is a fraction of the probability of the single channel occurrence of each type, whether it's a re-initialization or resynchronization event. From Figure 9-7, the fractions are 40% for TX channels and 12% for RX channels. These type of events were described in detail in Section 8.3.

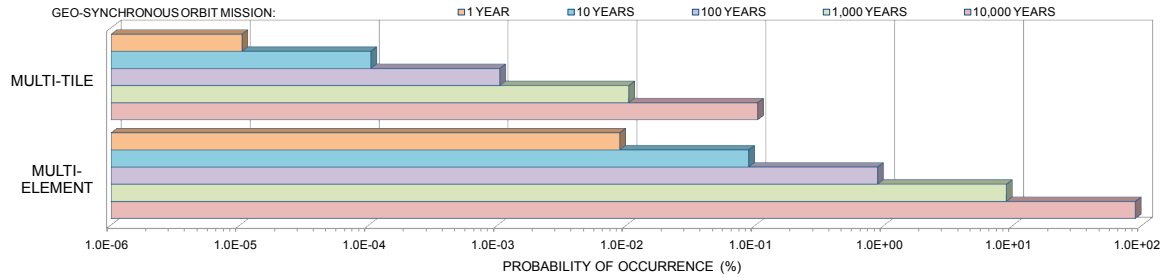

Figure 9-8. Probability of occurrence of MEU events and Multi-Tile events.

In Figure 9-8 it is shown that the probability of MEU events is less than 0.1% after 10 years in orbit, while for multi-tile events, the probability remains less than .1% after the theoretical 10,000 years in orbit.

9.3 Bit-Error-Rate Impact Estimate

To estimate the BER incurred by a MGT communication system as a result of the SEEs incurred by the MGT tiles, we must understand how each one of the events measured contributes to the BER, and then compute the total effective BER from all the different events. For each type of event, which includes all events presented here, there will be an amount of time that the event lasts, which consists of the time required to detect, and if applicable, the time to correct the event. During this total duration, it has to be assumed that every bit transmitted by the system could be in error, thus the number of corrupted bits during each event's total time duration is the effective data rate of the MGT system times the total down time. With the use of on-orbit rate predictions shown in 8.6, it is possible to obtain a number of effective bit-errors per day for each event. The BER expression used in the calculations for each event-type is:

$$\mathrm{BER} = \frac{No.bits\ in\ Error}{Total\ No.bits} = \frac{P_{SEU} \cdot N_{susc} \cdot N_{err} \cdot K}{N_{bits-day}} \qquad (1)$$

Where for the system being analyzed here, $\boldsymbol{P_{SEU}}$ is the SEE upset rate probability of each event type in the orbit used; $\boldsymbol{N_{susc}}$ is the number of susceptible elements to the event, in this case channels or tiles; $\boldsymbol{N_{err}}$ is the total bits in error as an outcome of the SEE event; $\boldsymbol{N_{bits\text{-}day}}$ is the effective maximum number of bits transmitted in one day by our case-study MGT link; and $\boldsymbol{K}$ is the susceptibility duty-cycle factor of each event. The susceptibility duty cycle is essentially the probability of having the event coinciding at the same time as when the pertinent elements are susceptible.

The case study used in the BER analysis is illustrated by 9-9, which shows two FPGAs communicating via a MGT dual-link. The BER of the MGTs used in the communication link is only one of the contributors to the total BER of this communication interface. For the total BER of the interface, we must include the communication core, and any upstream design partitions that provide the data to be transmitted. The operational assumptions used for the case study are listed below:

- Rate: Aggregate, 3.125Gbps; effective, 2.5Gbps
- Data Volume vs. Sync/Alignment Volume: 4/1
- Max. Packet Size: 2kB
- Link Status Verification Capability: YES
- Re-Send on error: NO

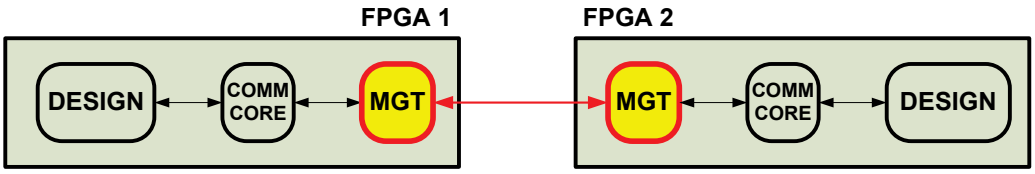

Figure 9-9. Communication link used in Case Study.

Table 15. BER Estimation Analysis.

EVENT TYPE	P_{SEU} (/day)	TIME TO DETECT (S)	TIME TO RECOVER (S)	TOTAL DOWN TIME (S)	N_{err}	N_{susc}	K	BER	CORRECTIVE ACTION
BE TX	**2.13E-04**	-	-	-	1.60E+01	2	75.0%	2.37E-17	AUTOMATIC
BE RX	**5.58E-04**	-	-	-	1.60E+01	2	75.0%	6.20E-17	AUTOMATIC
TX LOL : RESYNC	**5.47E-05**	-	2.00E-04	2.00E-04	5.00E+05	2	100.0%	2.53E-13	PROTOCOL RESYNC
TX LOL : REINIT	**6.21E-06**	1.28E-05	6.40E-06	1.92E-05	4.80E+04	2	100.0%	2.76E-15	PROTOCOL RE-INIT
RX LOL : RESYNC	**1.14E-04**	-	2.00E-04	2.00E-04	5.00E+05	2	100.0%	5.28E-13	PROTOCOL RESYNC
RX LOL : REINIT	**1.20E-05**	1.28E-05	1.00E-03	1.01E-03	2.53E+06	2	100.0%	2.81E-13	PROTOCOL RE-INIT
RX LOL : LONG RNDM RESYNC	**2.77E-06**	-	2.64E+00	2.64E+00	6.60E+09	2	100.0%	1.69E-10	PROTOCOL RESYNC
GTX TILE RESET	**2.10E-06**	5.00E-03	1.00E-01	1.05E-01	2.63E+08	4	100.0%	1.02E-11	PROTOCOL PHY RE-INIT/USER RE-INIT
GTX TILE DRP SCRUB	**6.82E-09**	1.00E+00	1.00E+00	2.00E+00	5.00E+09	4	100.0%	6.31E-13	DRP SCRUB
				TOTAL EFFECTIVE BER: 1.81E-10					
				EFFECTIVE DOWN TIME: 7.59E-06					

All the events discussed of interest to this analysis are summarized in the left column of Table 15. With each type of event is the worst-case time to detect and time to recover assumed for each event, followed by the resulting worst-case estimate of bits in error per event, using an effective line rate of 2.5Gbps, from an aggregate line rate of 3.125Gbps. The aggregate line rate includes the 20% overhead bits required by 8b/10b encoding. For Bit Error events, a worst-case assumption of the event causing 16-bits in error is used, independent of event duration. For the Resync LOL events, the assumption is that they will be corrected autonomously by the time they have dissipated, which is a worst case 200µs. Random, long LOL RX ReSync events are also taken into account, using a duration of 2.64, which is the average duration of this event measured in the testing. ReInit events are assumed to be detected within two 2kB packets (approximately 12.8µs), and require 1ms to complete the re-initialization procedure. The events requiring a GTX Tile Reset and DRP Scrub actions are assumed to be detected within 5ms and 1.0s of the occurrence, and recovered within 100ms and 1.0s respectively. The resulting BER in this example system would be around 1.81E-10. The actual BER could be driven down further by performing a more sophisticated analysis and expediting the recovery by the protocol.

9.4 Impact Summary

Table 16 summarizes the impact on a system for each of the events observed during the testing. This impact analysis assumes a system that performs periodic and continuous configuration image scrubbing, uses 2kB packet sizes with resynchronization in between each packet, a 4/1 ration of sync data vs. payload data, and a 3.125Gbps line rate. As stated earlier, *the protocol is the most important variable in determining the system response*.

- If employing a protocol with transmission verification, and with the ability to detect hang-ups and kick-off re-initialization; no data loss will take place and the band-width impact would be effectively negligible,
- If the protocol possesses transmission verification, but does not have the ability to detect hang-up events or to kick-off a re-initialization, the design will only recover from re-initialization events with a global reset, reconfiguration or reboot; but would be unsusceptible to resynchronization and BE events,

- If the protocol possesses no verification capability, but does have the ability to detect hang-up conditions and kick-off re-initializations; data loss would result from all the types of events, but the system would recover autonomously from any event.

Table 16. System Impact Effects Summary.

Event	Chan. Type	Potential Outcomes (2kB Packet SYstem)	Ref. Cross-Section
Bit Errors	TX, RX	▪ Corrupted payload data (BE affected pkt. payload data) ▪ Lost Packet (BE affected pkt. control data) ▪ No Impact (BE affected inter-pkt gaps)	Figure 7-5
Short Resync LOL	TX, RX	▪ Lost Packets; min. 1, max. 32	Figure 7-7, Figure 7-8
Random Long Resync LOL	RX	▪ Lost Packets; min. 300, max. 3E+6	Figure 8-9
Channel-level Re-initialization	TX, RX	▪ Indefinite Loss of packets until re-initialization of channel	Figure 7-7, Figure 7-8
Tile level Re-initialization	RX	▪ Indefinite Loss of packets in channel, until GTX Reset applied ▪ MGTs of tile unavailable during reset	Figure 7-10
Tile DRP corruption	All	▪ Tile corruption resulting in indefinite loss of packets until DRP is scrubbed ▪ If affected MGT tile is reference tile, multiple-tiles can be corrupt	Figure 7-10

9.5 Overall Assessment

The single event effects of the Virtex-5QV FPGA MGT devices have been studied, classified and quantified through heavy ion accelerator testing in a way which can assist designers in developing radiation hardened or radiation tolerant MGT systems as efficiently as possible.

9.5.1 Functionality Characterized

In this investigation, all of the basic mechanisms of the MGT were evaluated, except for two features that are non-essential but of much interest. These are the MGT tile's RX clock-correction mechanisms, used in asynchronous MGT systems, and the multiple-channel alignment mechanisms, used in channel-bonded systems. The contribution of these mechanisms is not expected to be much different than what has already been reported. Clock-correction is intrinsically immune since its usage has several degrees of elasticity, where a worst-case scenario would not cause anything that wouldn't be fixed by a channel's re-initialization stroke. A system that employs channel bonding implements the channel re-alignment characters as part of the synchronization sequence. At worst, the SEE susceptibility of both of these mechanisms would contribute to perhaps increasing the resynchronization or re-initialization event rates.

9.5.2 Mitigation Required

Analysis demonstrates that the impact of heavy ions on the MGT functionality can be effectively mitigated by the serial communication protocol, assuming that it can be outfitted with the appropriate detection mechanisms which can provide subsequent activation of channel and tile re-initialization procedures. Zero data loss systems can be implemented with negligible little

band-width penalty, by using "guaranteed delivery" protocols. Multiple-channel SEE events have been observed and must be taken into account when evaluating SEE impact on protocols employing channel-bonded systems or redundant systems. Primary, redundant and triplicated channels should be mapped into different tiles, and if needed, with independent reference clocks.

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Appendix A : Characterization Experimental Log Tables

A-1 Experimental Log May 2010 Texas A&M characterization experiments.

TEST DATE	RUN	SN	ENERGY (MeV/u)	ENERGY (MeV)	ION	LET	EFF LET	EFF RANGE (um)	DEGRADER (#@ANGLE)	DUT ANGLE	RUN TIME (S)	FLUX (p/cm2/s)	FLUENCE (p/cm2)	LOL LEVEL (WORDS)	CHAN	LINK TYPE	ACQUISITION ERRORS?	LINK TIME* (S)	LINK FLUENCE* (p/cm2)	LOL COUNT *	BE COUNT *	BiE COUNT (bits)	GTX RESET LOL COUNT	GLUT SCRUB LOL COUNT	LOL EVENT CAPTURES	RESYNC LOL	RX BUFF RST LOL	RX RESET LOL	RX CDR RST LOL	TX RST	SRV RX CDR RST	RESYNC LONG LOL
MAY	27	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	165.7	1.81E+06	3.00E+05	512	0	TX		166.365	3.01E+05	1	9	8.349E+03			1	1						
MAY	27	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	165.7	1.81E+06	3.00E+05	512	1	RX		166.365	3.01E+05	5	15	4.057E+04			5	5						
MAY	27	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	165.7	1.81E+06	3.00E+05	512	4	TX		166.365	3.01E+05	4	12	3.434E+04			4	4						
MAY	27	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	165.7	1.81E+06	3.00E+05	512	5	RX		166.365	3.01E+05	4	15	3.350E+04			4	4						
MAY	27	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	165.7	1.81E+06	3.00E+05	512	6	TX		166.363	3.01E+05	1	11	8.740E+03			1	1						
MAY	27	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	165.7	1.81E+06	3.00E+05	512	7	RX		166.365	3.01E+05	5	16	4.145E+04			5	5						
MAY	27	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	165.7	1.81E+06	3.00E+05	512	8	TX		166.364	3.01E+05	5	21	5.055E+04			5	5						
MAY	27	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	165.7	1.81E+06	3.00E+05	512	9	RX		166.364	3.01E+05	1	26	1.703E+04			1	1						
MAY	27	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	165.7	1.81E+06	3.00E+05	512	10	TX		166.364	3.01E+05	3	20	3.364E+04			3	3						
MAY	27	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	165.7	1.81E+06	3.00E+05	512	11	RX		166.363	3.01E+05	3	17	3.292E+05			3	3						
MAY	27	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	165.7	1.81E+06	3.00E+05	512	16	TX	A	156.685	2.84E+05													
MAY	27	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	165.7	1.81E+06	3.00E+05	512	17	RX		165.856	3.00E+05	10	14	8.337E+04			10	9	1					
MAY	28	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	112.4	3.16E+04	3.56E+06	512	0	TX		113.584	3.60E+06	35	173	2.978E+05			35	35						
MAY	28	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	112.4	3.16E+04	3.56E+06	512	1	RX		98.677	3.13E+06	45	167	3.736E+05			45	43	1					1
MAY	28	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	112.4	3.16E+04	3.56E+06	512	4	TX		113.584	3.60E+06	39	138	3.277E+05			39	39						
MAY	28	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	112.4	3.16E+04	3.56E+06	512	5	RX	B			0		2.893E+09										
MAY	28	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	112.4	3.16E+04	3.56E+06	512	6	TX		113.584	3.60E+06	33	128	2.776E+05			33	33						
MAY	28	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	112.4	3.16E+04	3.56E+06	512	7	RX		113.075	3.58E+06	46	172	3.853E+05			46	45	1					
MAY	28	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	112.4	3.16E+04	3.56E+06	512	8	TX		113.583	3.60E+06	30	151	2.629E+05			30	30						
MAY	28	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	112.4	3.16E+04	3.56E+06	512	9	RX		113.583	3.60E+06	59	197	5.301E+05			59	59						
MAY	28	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	112.4	3.16E+04	3.56E+06	512	10	TX		113.583	3.60E+06	36	163	3.062E+05			36	36						
MAY	28	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	112.4	3.16E+04	3.56E+06	512	11	RX		90.452	2.86E+06	57	168	4.768E+05	1		57	51			1			4
MAY	28	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	112.4	3.16E+04	3.56E+06	512	16	TX		113.584	3.60E+06	38	161	3.215E+05			38	38						
MAY	28	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	112.4	3.16E+04	3.56E+06	512	17	RX	A	95.973	3.04E+06	0		4.242E+09		1								
MAY	29	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	117.6	2.20E+04	2.59E+06	512	0	TX	C	115.196	2.53E+06	22	116	1.952E+05			22	22						
MAY	29	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	117.6	2.20E+04	2.59E+06	512	1	TX	A, C	93.568	2.06E+06	0		3.520E+06	1	1								
MAY	29	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	117.6	2.20E+04	2.59E+06	512	4	TX	C	115.196	2.53E+06	25	100	1.967E+05			22	26						
MAY	29	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	117.6	2.20E+04	2.59E+06	512	5	RX	C	114.687	2.52E+06	49	137	4.095E+05			47	50	1					
MAY	29	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	117.6	2.20E+04	2.59E+06	512	6	TX	C	115.196	2.53E+06	20	102	1.678E+05			19	21						
MAY	29	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	117.6	2.20E+04	2.59E+06	512	7	RX	C	90.588	1.99E+06	48	235	8.110E+05	1	1	48	40			2			1
MAY	29	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	117.6	2.20E+04	2.59E+06	512	8	TX	C	115.196	2.53E+06	30	109	2.531E+05			29	31						
MAY	29	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	117.6	2.20E+04	2.59E+06	512	9	RX	C	112.140	2.47E+06	47	131	3.778E+05			44	45	3	2				
MAY	29	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	117.6	2.20E+04	2.59E+06	512	10	TX	C	115.196	2.53E+06	23	100	1.969E+05			21	25						
MAY	29	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	117.6	2.20E+04	2.59E+06	512	11	RX	C	99.544	2.19E+06	42	103	3.485E+05	1		40	42						
MAY	29	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	117.6	2.20E+04	2.59E+06	512	16	TX	C	115.196	2.53E+06	32	124	2.720E+05			29	35						
MAY	29	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	117.6	2.20E+04	2.59E+06	512	17	RX	A, C	111.831	2.46E+06	0		2.138E+09										
MAY	30	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	206.4	1.66E+04	3.44E+06	512	0	TX		204.529	3.40E+06	43	142	7.060E+05			37	49						
MAY	30	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	206.4	1.66E+04	3.44E+06	512	1	RX	A	162.622	2.71E+06	0		4.277E+09	1									
MAY	30	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	206.4	1.66E+04	3.44E+06	512	4	TX		204.530	3.40E+06	44	150	7.410E+05			39	50						
MAY	30	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	206.4	1.66E+04	3.44E+06	512	5	RX		203.256	3.38E+06	57	196	9.516E+05			52	62	1					
MAY	30	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	206.4	1.66E+04	3.44E+06	512	6	TX		204.530	3.40E+06	40	141	6.720E+05			34	47						
MAY	30	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	206.4	1.66E+04	3.44E+06	512	7	RX		187.710	3.12E+06	58	186	9.507E+05	2		50	63					1	
MAY	30	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	206.4	1.66E+04	3.44E+06	512	8	TX	A	204.530	3.40E+06	0		1.430E+09										
MAY	30	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	206.4	1.66E+04	3.44E+06	512	9	RX		202.748	3.37E+06	59	181	9.743E+05			55	61	2	1				
MAY	30	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	206.4	1.66E+04	3.44E+06	512	10	TX		204.530	3.40E+06	32	134	5.394E+05			28	37						
MAY	30	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	206.4	1.66E+04	3.44E+06	512	11	RX		191.471	3.19E+06	49	168	8.118E+05	1		45	51	1	1				
MAY	30	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	206.4	1.66E+04	3.44E+06	512	16	TX		204.530	3.40E+06	47	150	7.875E+05			42	52						
MAY	30	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	206.4	1.66E+04	3.44E+06	512	17	RX		201.984	3.36E+06	67	186	1.119E+06			61	70	2	1				
MAY	31	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	223.6	1.56E+04	3.48E+06	64	0	TX		218.742	3.40E+06	32	156	3.595E+04			32	32						
MAY	31	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	223.6	1.56E+04	3.48E+06	64	1	RX		192.261	2.99E+06	55	167	5.856E+04	2	1	55	52						
MAY	31	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	223.6	1.56E+04	3.48E+06	64	4	TX	A	218.742	3.40E+06	46												
MAY	31	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	223.6	1.56E+04	3.48E+06	64	5	RX	A	217.214	3.38E+06	179												
MAY	31	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	223.6	1.56E+04	3.48E+06	64	6	TX		218.742	3.40E+06	43	156	4.682E+04			43	43						
MAY	31	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	223.6	1.56E+04	3.48E+06	64	7	RX		218.742	3.40E+06	60	207	6.537E+04			60	60						
MAY	31	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	223.6	1.56E+04	3.48E+06	64	8	TX		210.830	3.28E+06	27	159	3.389E+04			29	28						
MAY	31	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	223.6	1.56E+04	3.48E+06	64	9	RX		198.688	3.09E+06	61	178	6.592E+04	1	1	61	59		1				
MAY	31	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	223.6	1.56E+04	3.48E+06	64	10	TX		210.830	3.28E+06	28	151	3.224E+04			28	29						
MAY	31	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	223.6	1.56E+04	3.48E+06	64	11	RX		192.620	3.00E+06	48	174	5.274E+04	1		48	47						1
MAY	31	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	223.6	1.56E+04	3.48E+06	64	16	TX		218.742	3.40E+06	39	143	4.368E+04			39	39						
MAY	31	A4464	25.0	1751	Xe	49.0	49.0	140	NONE	0	223.6	1.56E+04	3.48E+06	64	17	RX		216.704	3.37E+06	72	175	7.541E+04			72	68	4					
MAY	63	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	222.8	4.54E+04	1.01E+07	512	0	TX		218.753	9.94E+06	52	276	4.423E+05			52	52						
MAY	63	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	222.8	4.54E+04	1.01E+07	512	1	RX		169.614	7.71E+06	60	272	4.973E+05	2		60	55		1				2
MAY	63	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	222.8	4.54E+04	1.01E+07	512	4	TX		218.752	9.94E+06	42	292	3.511E+05			42	42						
MAY	63	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	222.8	4.54E+04	1.01E+07	512	5	RX		214.839	9.76E+06	62	361	5.068E+05			62	57	3	2				
MAY	63	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	222.8	4.54E+04	1.01E+07	512	6	TX		218.752	9.94E+06	42	274	3.559E+05			42	42						
MAY	63	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	222.8	4.54E+04	1.01E+07	512	7	RX		198.859	9.03E+06	49	310	4.001E+05	2		49	45			1			1
MAY	63	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	222.8	4.54E+04	1.01E+07	512	8	TX		218.752	9.94E+06	48	276	4.087E+05			48	48						
MAY	63	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	222.8	4.54E+04	1.01E+07	512	9	RX		214.678	9.75E+06	87	324	7.116E+05			87	81	2	4				
MAY	63	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	222.8	4.54E+04	1.01E+07	512	10	TX		218.752	9.94E+06	55	251	4.618E+05			55	55						
MAY	63	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	222.8	4.54E+04	1.01E+07	512	11	RX		197.752	8.98E+06	64	297	5.392E+05			64	62						2
MAY	63	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	222.8	4.54E+04	1.01E+07	512	16	TX		218.753	9.94E+06	37	264	3.135E+05			37	37						
MAY	63	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	222.8	4.54E+04	1.01E+07	512	17	RX		213.406	9.69E+06	68	312	5.459E+05			68	61	3	1	3			
MAY	64	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	245.6	4.32E+04	1.06E+07	8	0	TX	D			0					52	52						
MAY	64	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	245.6	4.32E+04	1.06E+07	8	1	RX	D			0			1		77	73		1	1			1
MAY	64	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	245.6	4.32E+04	1.06E+07	8	4	TX	D			0					53	53						
MAY	64	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	245.6	4.32E+04	1.06E+07	8	5	RX	D			0					85	82	3					
MAY	64	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	245.6	4.32E+04	1.06E+07	8	6	TX	D			0					51	51						
MAY	64	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	245.6	4.32E+04	1.06E+07	8	7	RX	D			0			3		70	66		1				
MAY	64	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	245.6	4.32E+04	1.06E+07	8	8	TX	A, D			0												
MAY	64	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	245.6	4.32E+04	1.06E+07	8	9	RX	D			0					75	69	3	1	2			
MAY	64	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	245.6	4.32E+04	1.06E+07	8	10	TX	D			0					50	50						
MAY	64	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	245.6	4.32E+04	1.06E+07	8	11	RX	D			0			3		51	45	1			1		1
MAY	64	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	245.6	4.32E+04	1.06E+07	8	16	TX	D			0					57	57						
MAY	64	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	245.6	4.32E+04	1.06E+07	8	17	RX	D			0					83	82	1					

A–1 (Continued)

RUN	SN	ENERGY (MeV/u)	ENERGY (MeV)	ION	LET	EFF LET	EFF RANGE (um)	DEGRADER (#@ANGLE)	DUT ANGLE	RUN TIME (S)	FLUX (p/cm2/s)	FLUENCE (p/cm2)	LOL LEVEL (WORDS)	CHAN	LINK TYPE	ACQUISITION ERRORS?	LINK TIME* (S)	LINK FLUENCE* (p/cm2)	LOL COUNT *	BE COUNT *	BiE COUNT (bits)	GTX RESET LOL COUNT	GLUT SCRUB LOL COUNT	LOL EVENT CAPTURES	RESYNC LOL	RX BUFF RST LOL	RX RESET LOL	RX CDR RST LOL
65	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	276.7	3.62E+04	1.00E+07	1024	0	TX		269.427	9.75E+06	47	309	7.897E+05			47	47			
65	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	276.7	3.62E+04	1.00E+07	1024	1	RX		224.664	8.13E+06	66	320	1.079E+06	5		66	60			
65	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	276.7	3.62E+04	1.00E+07	1024	4	TX		269.427	9.75E+06	47	301	7.940E+05			47	47			
65	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	276.7	3.62E+04	1.00E+07	1024	5	RX		265.773	9.61E+06	82	340	1.344E+06			82	76	5		1
65	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	276.7	3.62E+04	1.00E+07	1024	6	TX		269.427	9.75E+06	43	265	7.247E+05			43	43			
65	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	276.7	3.62E+04	1.00E+07	1024	7	RX		242.664	8.78E+06	83	318	1.372E+06	1		83	79			
65	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	276.7	3.62E+04	1.00E+07	1024	8	TX		269.427	9.75E+06	39	280	6.589E+05			39	39			
65	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	276.7	3.62E+04	1.00E+07	1024	9	RX		267.390	9.67E+06	75	343	1.244E+06			75	71	4		
65	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	276.7	3.62E+04	1.00E+07	1024	10	TX		269.427	9.75E+06	37	266	6.236E+05			37	37			
65	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	276.7	3.62E+04	1.00E+07	1024	11	RX		212.543	7.69E+06	63	267	1.020E+06	5		63	56		1	
65	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	276.7	3.62E+04	1.00E+07	1024	16	TX		269.427	9.75E+06	36	267	6.053E+05			36	36			
65	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	276.7	3.62E+04	1.00E+07	1024	17	RX		266.864	9.65E+06	72	365	1.183E+06			72	68	2	2	
66	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	379.0	2.70E+04	1.02E+07	1024	0	TX		368.928	9.95E+06	64	351	1.074E+06			64	64			
66	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	379.0	2.70E+04	1.02E+07	1024	1	RX		327.491	8.83E+06	90	430	1.454E+06	3		90	82	1		
66	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	379.0	2.70E+04	1.02E+07	1024	4	TX		368.928	9.95E+06	70	339	1.179E+06			70	70			
66	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	379.0	2.70E+04	1.02E+07	1024	5	RX		366.128	9.87E+06	110	421	1.812E+06			110	105	4	1	
66	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	379.0	2.70E+04	1.02E+07	1024	6	TX		368.928	9.95E+06	66	341	1.108E+06			66	66			
66	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	379.0	2.70E+04	1.02E+07	1024	7	RX		321.632	8.67E+06	106	391	1.744E+06	5		106	99			
66	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	379.0	2.70E+04	1.02E+07	1024	8	TX		368.928	9.95E+06	64	333	1.076E+06			64	64			
66	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	379.0	2.70E+04	1.02E+07	1024	9	RX		363.582	9.80E+06	112	409	1.812E+06			112	103	6	3	
66	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	379.0	2.70E+04	1.02E+07	1024	10	TX		353.933	9.54E+06	61	335	1.024E+06	1		61	60			
66	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	379.0	2.70E+04	1.02E+07	1024	11	RX		341.377	9.21E+06	106	409	1.737E+06	4		106	100	1		
66	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	379.0	2.70E+04	1.02E+07	1024	16	TX		368.928	9.95E+06	58	337	9.764E+05			58	58			
66	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	379.0	2.70E+04	1.02E+07	1024	17	RX		358.947	9.68E+06	107	420	1.778E+06		1	107	100	3	1	1
67	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	140.6	4.98E+04	7.00E+06	8	0	TX	C	140.489	6.99E+06	55	288	1.106E+04			55	55			
67	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	140.6	4.98E+04	7.00E+06	8	1	RX	C	112.490	5.60E+06	66	269	1.163E+04	1		66	66			
67	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	140.6	4.98E+04	7.00E+06	8	4	TX	C	140.489	6.99E+06	46	224	8.356E+03			46	46			
67	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	140.6	4.98E+04	7.00E+06	8	5	RX	C	139.469	6.94E+06	80	281	1.216E+04			80	79			1
67	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	140.6	4.98E+04	7.00E+06	8	6	TX	C	140.489	6.99E+06	49	230	8.942E+03			49	49			
67	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	140.6	4.98E+04	7.00E+06	8	7	RX	C	134.823	6.71E+06	72	274	1.092E+04			72	70			
67	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	140.6	4.98E+04	7.00E+06	8	8	TX	A, C	139.778	6.96E+06	0									
67	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	140.6	4.98E+04	7.00E+06	8	9	RX	C	139.724	6.95E+06	69	262	1.040E+04			69	68		1	
67	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	140.6	4.98E+04	7.00E+06	8	10	TX	A, C	136.757	6.81E+06	0									
67	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	140.6	4.98E+04	7.00E+06	8	11	RX	C	128.166	6.38E+06	46	259	7.522E+03	1		46	43			1
67	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	140.6	4.98E+04	7.00E+06	8	16	TX	C	140.487	6.99E+06	50	210	8.775E+03			50	50			
67	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	140.6	4.98E+04	7.00E+06	8	17	RX	C	136.412	6.79E+06	75	283	1.146E+04			75	69	2	4	
68	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	290.6	3.46E+04	1.01E+07	128	0	TX		281.453	9.74E+06	73	336	1.641E+05			73	73			
68	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	290.6	3.46E+04	1.01E+07	128	1	RX		250.139	8.66E+06	101	346	2.126E+05	2		101	95			1
68	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	290.6	3.46E+04	1.01E+07	128	4	TX		281.454	9.74E+06	65	439	1.443E+05			65	65			
68	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	290.6	3.46E+04	1.01E+07	128	5	RX		254.748	8.82E+06	87	394	1.831E+05		1	87	79	4	2	
68	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	290.6	3.46E+04	1.01E+07	128	6	TX		281.454	9.74E+06	55	350	1.186E+05			55	55			
68	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	290.6	3.46E+04	1.01E+07	128	7	RX		260.556	9.02E+06	96	380	2.066E+05	1		96	88	4		
68	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	290.6	3.46E+04	1.01E+07	128	8	TX		281.453	9.74E+06	50	344	1.126E+05			50	50			
68	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	290.6	3.46E+04	1.01E+07	128	9	RX		276.871	9.59E+06	105	395	2.162E+05			105	97	7		1
68	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	290.6	3.46E+04	1.01E+07	128	10	RX	A	281.452	9.74E+06	0									
68	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	290.6	3.46E+04	1.01E+07	128	11	RX		265.776	9.20E+06	98	406	2.043E+05	2		98	93	2	1	
68	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	290.6	3.46E+04	1.01E+07	128	16	TX		279.926	9.69E+06	72	310	1.567E+05			72	71			
68	A4464	25.0	860	Kr	30.0	30.0	108	2@52.5°	0	290.6	3.46E+04	1.01E+07	128	17	RX		276.359	9.57E+06	120	380	2.484E+05			120	116	2	2	
69	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	386.2	2.68E+04	1.03E+07	128	0	TX		378.461	1.01E+07	52	266	1.114E+05			52	52			
69	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	386.2	2.68E+04	1.03E+07	128	1	RX		327.733	8.77E+06	68	309	1.420E+05	1		68	66			
69	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	386.2	2.68E+04	1.03E+07	128	4	TX		378.461	1.01E+07	51	260	1.114E+05			51	51			
69	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	386.2	2.68E+04	1.03E+07	128	5	RX		377.188	1.01E+07	72	327	1.527E+05			72	70	1	1	
69	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	386.2	2.68E+04	1.03E+07	128	6	TX		378.461	1.01E+07	44	246	9.537E+04			44	44			
69	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	386.2	2.68E+04	1.03E+07	128	7	RX		316.854	8.48E+06	71	259	1.455E+05	4		71	65			
69	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	386.2	2.68E+04	1.03E+07	128	8	TX		378.461	1.01E+07	37	248	8.030E+04			37	37			
69	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	386.2	2.68E+04	1.03E+07	128	9	RX		377.442	1.01E+07	69	325	1.479E+05			69	67	2		
69	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	386.2	2.68E+04	1.03E+07	128	10	TX		378.461	1.01E+07	38	250	8.484E+04			38	38			
69	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	386.2	2.68E+04	1.03E+07	128	11	RX		348.043	9.32E+06	59	298	1.269E+05	2		59	56			
69	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	386.2	2.68E+04	1.03E+07	128	16	TX		377.356	1.01E+07	49	267	1.065E+05			49	48			1
69	A4464	25.0	1436	Kr	23.8	23.8	202	NONE	0	386.2	2.68E+04	1.03E+07	128	17	RX		377.952	1.01E+07	69	357	1.497E+05			69	68	1		

A–1 (Continued)

RUN	SN	ENERGY (MeV/u)	ENERGY (MeV)	ION	LET	EFF LET	EFF RANGE (um)	DEGRADER (#@ANGLE)	DUT ANGLE	RUN TIME (S)	FLUX (p/cm2/s)	FLUENCE (p/cm2)	LOL LEVEL (WORDS)	CHAN	LINK TYPE	ACQUISITION ERRORS ?	LINK TIME* (S)	LINK FLUENCE* (p/cm2)	LOL COUNT *	BE COUNT *	BiE COUNT (bits)	GTX RESET LOL COUNT	GLUT SCRUB LOL COUNT	LOL EVENT CAPTURES	RESYNC LOL	RX BUFF RST LOL	RX RESET LOL	RX CDR RST LOL	TX RST	SRV RX CDR RST	RESYNC LONG LOL
72	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	361.5	2.81E+04	1.02E+07	128	0	TX		356.966	1.00E+07	95	354	2.058E+05			94	95						
72	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	361.5	2.81E+04	1.02E+07	128	1	RX		327.228	9.21E+06	145	508	3.459E+05	1	1	141	138		1	1	1		2
72	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	361.5	2.81E+04	1.02E+07	128	4	TX		356.967	1.00E+07	80	384	1.731E+05			78	80						
72	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	361.5	2.81E+04	1.02E+07	128	5	TX	A	334.796	9.42E+06	0		8.795E+08		1								
72	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	361.5	2.81E+04	1.02E+07	128	6	TX		356.967	1.00E+07	61	358	1.340E+05			59	61						
72	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	361.5	2.81E+04	1.02E+07	128	7	RX		327.793	9.22E+06	116	432	2.478E+05	3		114	111		1				1
72	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	361.5	2.81E+04	1.02E+07	128	8	TX		356.966	1.00E+07	67	343	1.499E+05			62	67						
72	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	361.5	2.81E+04	1.02E+07	128	9	RX		353.148	9.93E+06	115	437	2.408E+05			110	109	3	3				
72	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	361.5	2.81E+04	1.02E+07	128	10	TX		356.966	1.00E+07	66	344	1.484E+05			61	66						
72	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	361.5	2.81E+04	1.02E+07	128	11	RX		341.343	9.60E+06	116	431	2.442E+05	2		113	109		1	2			
72	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	361.5	2.81E+04	1.02E+07	128	16	TX		356.967	1.00E+07	71	417	1.565E+05			71	71						
72	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	361.5	2.81E+04	1.02E+07	128	17	RX		353.912	9.96E+06	130	515	2.793E+05			129	125	4		1			
73	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	181.4	2.45E+04	4.44E+06	1024	0	TX	C	180.346	4.41E+06	43	240	7.602E+05			43	43						
73	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	181.4	2.45E+04	4.44E+06	1024	1	RX	A, C	168.422	4.12E+06	0		2.411E+09	1									
73	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	181.4	2.45E+04	4.44E+06	1024	4	TX	C	180.346	4.41E+06	42	171	7.070E+05			41	42						
73	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	181.4	2.45E+04	4.44E+06	1024	5	TX	C	179.328	4.39E+06	61	226	1.029E+06			61	58	2					
73	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	181.4	2.45E+04	4.44E+06	1024	6	TX	C	180.346	4.41E+06	42	199	7.200E+05			42	42						
73	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	181.4	2.45E+04	4.44E+06	1024	7	RX	A, C	155.977	3.81E+06	0		1.004E+07	1									
73	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	181.4	2.45E+04	4.44E+06	1024	8	TX	C	180.346	4.41E+06	33	161	5.683E+05			33	33						
73	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	181.4	2.45E+04	4.44E+06	1024	9	RX	C	179.072	4.38E+06	52	215	8.948E+05			52	50	1	1				
73	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	181.4	2.45E+04	4.44E+06	1024	10	TX	A, C	180.346	4.41E+06	0		3.254E+09										
73	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	181.4	2.45E+04	4.44E+06	1024	11	RX	C	180.345	4.41E+06	60	203	1.065E+06			60	60						
73	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	181.4	2.45E+04	4.44E+06	1024	16	TX	C	180.346	4.41E+06	40	182	6.887E+05			38	40						
73	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	181.4	2.45E+04	4.44E+06	1024	17	RX	C	178.564	4.37E+06	70	219	1.251E+06			70	67	2	1				
74	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	571.2	1.77E+04	1.01E+07	1024	0	TX		549.963	9.73E+06	82	372	1.385E+06			82	82						
74	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	571.2	1.77E+04	1.01E+07	1024	1	RX		488.063	8.64E+06	140	448	2.315E+06	4	1	140	131	3					1
74	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	571.2	1.77E+04	1.01E+07	1024	4	TX		549.963	9.73E+06	79	405	1.346E+06			79	79						
74	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	571.2	1.77E+04	1.01E+07	1024	5	RX		548.690	9.71E+06	130	500	2.178E+06			130	125	4	1				
74	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	571.2	1.77E+04	1.01E+07	1024	6	TX		538.144	9.53E+06	74	401	1.256E+06			74	72						2
74	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	571.2	1.77E+04	1.01E+07	1024	7	RX	A	509.050	9.01E+06	3348			3									
74	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	571.2	1.77E+04	1.01E+07	1024	8	TX		549.962	9.73E+06	84	365	1.407E+06			84	84						
74	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	571.2	1.77E+04	1.01E+07	1024	9	RX	E	496.106		126												
74	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	571.2	1.77E+04	1.01E+07	1024	10	TX		549.962	9.73E+06	88	360	1.476E+06			88	88						
74	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	571.2	1.77E+04	1.01E+07	1024	11	RX		485.538	8.59E+06	130	382	2.120E+06	4		130	119	3	1				3
74	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	571.2	1.77E+04	1.01E+07	1024	16	TX		545.378	9.65E+06	83	358	1.404E+06			83	81					2	
74	A4464	25.0	519	Kr	35.1	35.1	63	3@35°	0	571.2	1.77E+04	1.01E+07	1024	17	RX		531.185	9.40E+06	140	438	2.320E+06		2	140	128	8	2				
102	A4464	24.8	321	N	0.9	0.9	878	NONE	0	92.1	1.18E+06	1.09E+08	8	0	TX	C	36.323	4.30E+07	5	3	1.950E+02				5						
102	A4464	24.8	321	N	0.9	0.9	878	NONE	0	92.1	1.18E+06	1.09E+08	8	1	RX	C	25.498	3.02E+07	7	10	4.110E+02	1		2	5						1
102	A4464	24.8	321	N	0.9	0.9	878	NONE	0	92.1	1.18E+06	1.09E+08	8	4	TX	C	36.323	4.30E+07	2	3	2.630E+02								2		
102	A4464	24.8	321	N	0.9	0.9	878	NONE	0	92.1	1.18E+06	1.09E+08	8	5	RX	C	35.815	4.24E+07	4	12	4.260E+02			1	2	2					
102	A4464	24.8	321	N	0.9	0.9	878	NONE	0	92.1	1.18E+06	1.09E+08	8	6	TX	C	36.323	4.30E+07	2	1	2.380E+02				1				1		
102	A4464	24.8	321	N	0.9	0.9	878	NONE	0	92.1	1.18E+06	1.09E+08	8	7	RX	C	27.902	3.30E+07	4	8	4.110E+02			1	3						
102	A4464	24.8	321	N	0.9	0.9	878	NONE	0	92.1	1.18E+06	1.09E+08	8	8	TX	C	36.323	4.30E+07	3	1	1.510E+02				3						
102	A4464	24.8	321	N	0.9	0.9	878	NONE	0	92.1	1.18E+06	1.09E+08	8	9	RX	C	35.561	4.21E+07	10	19	8.940E+02			2	9		1				
102	A4464	24.8	321	N	0.9	0.9	878	NONE	0	92.1	1.18E+06	1.09E+08	8	10	TX	C	36.323	4.30E+07	3	2	1.320E+02				3						
102	A4464	24.8	321	N	0.9	0.9	878	NONE	0	92.1	1.18E+06	1.09E+08	8	11	RX	C	25.690	3.04E+07	5	12	3.520E+02	1		1	4						
102	A4464	24.8	321	N	0.9	0.9	878	NONE	0	92.1	1.18E+06	1.09E+08	8	16	TX	C	36.323	4.30E+07	3	6	1.380E+02				2						1
102	A4464	24.8	321	N	0.9	0.9	878	NONE	0	92.1	1.18E+06	1.09E+08	8	17	RX	C	34.796	4.12E+07	7	17	5.530E+02			1	6					1	
104	A4464	24.8	321	N	0.9	0.9	878	NONE	0	86.5	1.17E+06	1.01E+08	512	0	TX		84.100	9.78E+07	1	19	8.362E+03				1						
104	A4464	24.8	321	N	0.9	0.9	878	NONE	0	86.5	1.17E+06	1.01E+08	512	1	RX		80.202	9.33E+07	3	41	2.117E+04			1	2						1
104	A4464	24.8	321	N	0.9	0.9	878	NONE	0	86.5	1.17E+06	1.01E+08	512	4	TX		84.100	9.78E+07	1	19	8.286E+03				1						
104	A4464	24.8	321	N	0.9	0.9	878	NONE	0	86.5	1.17E+06	1.01E+08	512	5	RX		83.590	9.72E+07	5	22	3.738E+04			1	3	1		1			
104	A4464	24.8	321	N	0.9	0.9	878	NONE	0	86.5	1.17E+06	1.01E+08	512	6	TX		84.100	9.78E+07	2	15	1.677E+04				1			1			
104	A4464	24.8	321	N	0.9	0.9	878	NONE	0	86.5	1.17E+06	1.01E+08	512	7	RX		72.107	8.38E+07	9	30	6.590E+04	2		3	5						1
104	A4464	24.8	321	N	0.9	0.9	878	NONE	0	86.5	1.17E+06	1.01E+08	512	8	TX		84.099	9.78E+07	6	7	4.260E+04				6						
104	A4464	24.8	321	N	0.9	0.9	878	NONE	0	86.5	1.17E+06	1.01E+08	512	9	RX		83.081	9.66E+07	15	33	1.090E+05			1	11	1					
104	A4464	24.8	321	N	0.9	0.9	878	NONE	0	86.5	1.17E+06	1.01E+08	512	10	TX		84.099	9.78E+07	5	15	3.324E+04				5						
104	A4464	24.8	321	N	0.9	0.9	878	NONE	0	86.5	1.17E+06	1.01E+08	512	11	RX		72.980	8.49E+07	12	21	8.681E+04	1		3	9			1			1
104	A4464	24.8	321	N	0.9	0.9	878	NONE	0	86.5	1.17E+06	1.01E+08	512	16	TX		84.100	9.78E+07	2	16	1.643E+04				2						
104	A4464	24.8	321	N	0.9	0.9	878	NONE	0	86.5	1.17E+06	1.01E+08	512	17	RX		82.571	9.60E+07	3	39	1.736E+04			2	1	1		1			

a) Channel data scratched, oscillatory event.
b) Channel data scratched, Corrupted SYNC_TIME counts in Service.
c) Bug in Service FPGA required a Reset of the Service FPGA, corrected by only accounting events up to the Reset.
d) Service Log File was corrupt, only LOL Event data available.
e) Channel data scratched, event required Service TX MGT Tile of channel to be continuously reset, corrupted the data.

A-2. Experimental Log August 2010 Texas A&M characterization experiments.

RUN	SN	ENERGY (MeV/u)	ENERGY (MeV)	ION	LET	EFF LET	EFF RANGE (um)	DEGRADER (#@ANGLE)	DUT ANGLE	RUN TIME (S)	FLUX (p/cm2/s)	FLUENCE (p/cm2)	LOL LEVEL (WORDS)	CHAN	LINK TYPE	ACQUISITION ERRORS?	LINK TIME* (S)	LINK FLUENCE* (p/cm2)	LOL COUNT *	BE COUNT *	BiE COUNT (bits)	GTX RESET LOL COUNT	DRP SCRUB LOL COUNT	LOL EVENT CAPTURES	RESYNC LOL	RX BUFF RST LOL	RX RESET LOL	RX CDR RST LOL	TX RST	SRV RX CDR RST	RESYNC LONG LOL
178	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	893.2	2.26E+04	2.02E+07	512	0	TX		445.482	2.02E+07	2	27	1.660E+04			2	2						
178	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	893.2	2.26E+04	2.02E+07	512	1	RX		445.482	2.02E+07	6	68	5.023E+04			6	6						
178	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	893.2	2.26E+04	2.02E+07	512	4	TX		445.482	2.02E+07	4	38	3.896E+04			4	4						
178	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	893.2	2.26E+04	2.02E+07	512	5	RX		444.973	2.01E+07	11	70	9.425E+04			11	10	1					
178	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	893.2	2.26E+04	2.02E+07	512	6	TX		445.482	2.02E+07	6	35	4.967E+04			6	6						
178	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	893.2	2.26E+04	2.02E+07	512	7	RX		430.562	1.95E+07	14	66	1.085E+05	1		14	12		1				
178	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	893.2	2.26E+04	2.02E+07	512	8	TX		445.482	2.02E+07	4	26	3.335E+04			4	4						
178	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	893.2	2.26E+04	2.02E+07	512	9	RX		444.973	2.01E+07	15	91	1.213E+05			15	14	1					
178	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	893.2	2.26E+04	2.02E+07	512	10	TX		445.482	2.02E+07	3	25	2.699E+04			3	3						
178	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	893.2	2.26E+04	2.02E+07	512	11	RX		445.482	2.02E+07	7	70	5.755E+04			7	7						
178	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	893.2	2.26E+04	2.02E+07	512	16	TX		445.482	2.02E+07	2	29	1.644E+04			2	2						
178	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	893.2	2.26E+04	2.02E+07	512	17	RX		444.718	2.01E+07	7	74	5.405E+04			7	6		1				
179	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	978.4	1.42E+04	1.39E+07	8	0	TX		484.949	1.37E+07	8	27	1.040E+03			8	8						
179	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	978.4	1.42E+04	1.39E+07	8	1	RX		477.804	1.35E+07	14	29	1.564E+03	1		14	13						
179	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	978.4	1.42E+04	1.39E+07	8	4	TX		484.949	1.37E+07	5	23	7.490E+02			5	5						
179	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	978.4	1.42E+04	1.39E+07	8	5	RX		483.930	1.37E+07	14	46	1.626E+03			14	13			1			
179	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	978.4	1.42E+04	1.39E+07	8	6	TX		484.949	1.37E+07	4	31	6.450E+02			4	4						
179	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	978.4	1.42E+04	1.39E+07	8	7	RX		438.886	1.24E+07	12	50	1.332E+03	3		11	9						
179	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	978.4	1.42E+04	1.39E+07	8	8	TX		484.949	1.37E+07	1	23	3.340E+02			1	1						
179	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	978.4	1.42E+04	1.39E+07	8	9	RX		484.440	1.37E+07	7	54	9.310E+02			7	6	1					
179	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	978.4	1.42E+04	1.39E+07	8	10	TX		484.949	1.37E+07	1	23	2.880E+02			1	1						
179	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	978.4	1.42E+04	1.39E+07	8	11	RX		450.254	1.28E+07	7	54	7.890E+02	2		7	5						
179	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	978.4	1.42E+04	1.39E+07	8	16	TX		484.949	1.37E+07	2	33	4.670E+02			2	2						
179	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	978.4	1.42E+04	1.39E+07	8	17	RX		483.421	1.37E+07	9	61	1.177E+03			9	7	1		1			
180	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	1195.2	1.71E+04	2.04E+07	1024	0	TX		596.283	2.04E+07	4	23	5.198E+04			3	3						
180	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	1195.2	1.71E+04	2.04E+07	1024	1	RX		589.089	2.01E+07	10	69	1.421E+05	1		9	8						
180	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	1195.2	1.71E+04	2.04E+07	1024	4	TX		596.284	2.04E+07	2	28	1.906E+04			1	1						
180	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	1195.2	1.71E+04	2.04E+07	1024	5	RX		596.284	2.04E+07	12	69	1.858E+05			11	11						
180	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	1195.2	1.71E+04	2.04E+07	1024	6	TX		596.284	2.04E+07	1	33	3.530E+02										
180	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	1195.2	1.71E+04	2.04E+07	1024	7	RX		596.284	2.04E+07	12	69	1.844E+05			11	11						
180	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	1195.2	1.71E+04	2.04E+07	1024	8	TX		596.284	2.04E+07	6	36	8.565E+04			5	5						
180	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	1195.2	1.71E+04	2.04E+07	1024	9	RX		595.520	2.04E+07	19	47	2.951E+05			18	17		1				
180	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	1195.2	1.71E+04	2.04E+07	1024	10	TX		596.284	2.04E+07	7	26	1.015E+05			6	6						
180	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	1195.2	1.71E+04	2.04E+07	1024	11	RX		587.909	2.01E+07	15	57	2.285E+05	1		14	13						
180	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	1195.2	1.71E+04	2.04E+07	1024	16	TX		596.283	2.04E+07	5	30	6.812E+04			4	4						
180	A4421	40.0	1484	Ar	4.0	4.0	952	NONE	0	1195.2	1.71E+04	2.04E+07	1024	17	RX		595.520	2.04E+07	13	69	1.901E+05			12	11		1				
181	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	767.4	1.47E+04	1.13E+07	512	0	TX		377.336	1.11E+07	14	46	1.172E+05			14	14						
181	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	767.4	1.47E+04	1.13E+07	512	1	RX		336.902	9.92E+06	23	126	1.813E+05	1		23	20					1	
181	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	767.4	1.47E+04	1.13E+07	512	4	TX		377.336	1.11E+07	12	70	1.008E+05			12	12						
181	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	767.4	1.47E+04	1.13E+07	512	5	RX		376.827	1.11E+07	42	133	3.475E+05			42	41	1					
181	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	767.4	1.47E+04	1.13E+07	512	6	TX		377.336	1.11E+07	13	66	1.087E+05			13	13						
181	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	767.4	1.47E+04	1.13E+07	512	7	RX		369.755	1.09E+07	24	103	1.971E+05	1		24	23						
181	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	767.4	1.47E+04	1.13E+07	512	8	TX		368.110	1.08E+07	22	100	1.953E+05			22	22						
181	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	767.4	1.47E+04	1.13E+07	512	9	RX		364.291	1.07E+07	36	151	2.905E+05			36	30	4	1	1			
181	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	767.4	1.47E+04	1.13E+07	512	10	TX		368.110	1.08E+07	16	68	1.421E+05			16	16						
181	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	767.4	1.47E+04	1.13E+07	512	11	RX		338.153	9.96E+06	41	120	3.270E+05	3	1	40	36						
181	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	767.4	1.47E+04	1.13E+07	512	16	TX		377.336	1.11E+07	11	56	8.843E+04			11	11						
181	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	767.4	1.47E+04	1.13E+07	512	17	RX		375.809	1.11E+07	22	127	1.717E+05			22	19	3					
182	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	1192.8	1.10E+04	1.31E+07	8	0	TX		586.886	1.29E+07	6	63	1.038E+03			6	6						
182	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	1192.8	1.10E+04	1.31E+07	8	1	RX		562.566	1.23E+07	31	143	3.578E+03	2		31	28						
182	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	1192.8	1.10E+04	1.31E+07	8	4	TX		586.886	1.29E+07	25	71	3.061E+03			25	25						
182	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	1192.8	1.10E+04	1.31E+07	8	5	RX		585.103	1.28E+07	66	127	7.560E+03			66	64	1			1		
182	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	1192.8	1.10E+04	1.31E+07	8	6	TX		586.886	1.29E+07	19	68	2.489E+03			17	17						
182	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	1192.8	1.10E+04	1.31E+07	8	7	RX		566.880	1.24E+07	43	145	4.987E+03	3		42	39						
182	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	1192.8	1.10E+04	1.31E+07	8	8	TX		586.886	1.29E+07	33	80	4.168E+03			33	33						
182	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	1192.8	1.10E+04	1.31E+07	8	9	RX		581.283	1.27E+07	61	154	6.755E+03			61	53	4	3		1		
182	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	1192.8	1.10E+04	1.31E+07	8	10	TX		586.886	1.29E+07	27	83	3.555E+03			27	27						
182	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	1192.8	1.10E+04	1.31E+07	8	11	RX		585.866	1.28E+07	55	154	6.509E+03			55	54			1			
182	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	1192.8	1.10E+04	1.31E+07	8	16	TX		586.886	1.29E+07	9	57	1.294E+03			9	9						
182	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	1192.8	1.10E+04	1.31E+07	8	17	RX	A	571.544	1.25E+07	65431	-80	5.094E+07		1								
183	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	945.7	1.16E+04	1.10E+07	1024	0	TX		465.106	1.08E+07	10	52	1.804E+05			11	11						
183	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	945.7	1.16E+04	1.10E+07	1024	1	RX		424.338	9.84E+06	20	112	2.959E+05	3		18	15						
183	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	945.7	1.16E+04	1.10E+07	1024	4	TX		465.106	1.08E+07	15	67	2.538E+05			15	15						
183	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	945.7	1.16E+04	1.10E+07	1024	5	RX		458.996	1.06E+07	46	114	7.047E+05			46	37	5	3		1		
183	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	945.7	1.16E+04	1.10E+07	1024	6	TX		465.106	1.08E+07	17	54	2.861E+05			16	16						
183	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	945.7	1.16E+04	1.10E+07	1024	7	RX		448.450	1.04E+07	37	101	5.816E+05	2		37	34			1			
183	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	945.7	1.16E+04	1.10E+07	1024	8	TX		465.106	1.08E+07	32	62	5.408E+05			32	32						
183	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	945.7	1.16E+04	1.10E+07	1024	9	RX		453.717	1.05E+07	49	129	7.634E+05	1		47	40	5	1				
183	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	945.7	1.16E+04	1.10E+07	1024	10	TX		465.106	1.08E+07	24	72	3.991E+05			24	24						
183	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	945.7	1.16E+04	1.10E+07	1024	11	RX		455.489	1.06E+07	51	137	8.469E+05	1		51	49	1					
183	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	945.7	1.16E+04	1.10E+07	1024	16	TX		465.107	1.08E+07	3	56	4.937E+04			3	3						
183	A4421	40.0	155	Ar	15.0	15.0	40.2	6@0°	0	945.7	1.16E+04	1.10E+07	1024	17	RX	A	457.472	1.06E+07	64892	414	4.269E+09										
184	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	999.1	1.20E+04	1.20E+07	512	0	TX		495.389	1.19E+07	17	126	1.426E+05			17	17						
184	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	999.1	1.20E+04	1.20E+07	512	1	RX		489.364	1.18E+07	31	181	2.577E+05	1		31	30						
184	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	999.1	1.20E+04	1.20E+07	512	4	TX		495.389	1.19E+07	10	114	8.384E+04			10	10						
184	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	999.1	1.20E+04	1.20E+07	512	5	RX		493.861	1.19E+07	24	159	1.986E+05			24	22		2				
184	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	999.1	1.20E+04	1.20E+07	512	6	TX		495.389	1.19E+07	11	125	9.347E+04			11	11						
184	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	999.1	1.20E+04	1.20E+07	512	7	RX		475.858	1.14E+07	36	132	2.935E+05	2		36	33	1					
184	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	999.1	1.20E+04	1.20E+07	512	8	TX		495.389	1.19E+07	14	109	1.171E+05			14	14						
184	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	999.1	1.20E+04	1.20E+07	512	9	RX		492.588	1.18E+07	29	143	2.217E+05			29	24	4	1				
184	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	999.1	1.20E+04	1.20E+07	512	10	TX		495.389	1.19E+07	13	100	1.089E+05			13	13						
184	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	999.1	1.20E+04	1.20E+07	512	11	RX		469.517	1.13E+07	29	131	2.338E+05	3		29	26						
184	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	999.1	1.20E+04	1.20E+07	512	16	TX		495.389	1.19E+07	16	90	1.371E+05			16	16						
184	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	999.1	1.20E+04	1.20E+07	512	17	RX		492.588	1.18E+07	31	131	2.436E+05			31	27	2	1	1			

A–2 (Continued)

RUN	SN	ENERGY (MeV/u)	ENERGY (MeV)	ION	LET	EFF LET	EFF RANGE (um)	DEGRADER (#@ANGLE)	DUT ANGLE	RUN TIME (S)	FLUX (p/cm2/s)	FLUENCE (p/cm2)	LOL LEVEL (WORDS)	CHAN	LINK TYPE	ACQUISITION ERRORS?	LINK TIME* (S)	LINK FLUENCE* (p/cm2)	LOL COUNT *	BE COUNT *	BiE COUNT (bits)	GTX RESET LOL COUNT	DRP SCRUB LOL COUNT	LOL EVENT CAPTURES	RESYNC LOL	RX BUFF RST LOL	RX RESET LOL	RX CDR RST LOL	TX RST	SRV RX CDR RST	RESYNC LONG LOL
185	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	1183.0	1.10E+04	1.30E+07	8	0	TX		588.623	1.29E+07	19	140	3.580E+03			19	19						
185	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	1183.0	1.10E+04	1.30E+07	8	1	RX		547.933	1.20E+07	36	162	5.076E+03	2		36	33						
185	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	1183.0	1.10E+04	1.30E+07	8	4	TX		588.624	1.29E+07	12	94	2.155E+03			12	12						
185	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	1183.0	1.10E+04	1.30E+07	8	5	RX		587.605	1.29E+07	27	123	3.942E+03			27	25	2					
185	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	1183.0	1.10E+04	1.30E+07	8	6	TX		588.623	1.29E+07	16	111	2.772E+03			16	16						
185	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	1183.0	1.10E+04	1.30E+07	8	7	RX		577.609	1.27E+07	31	136	4.223E+03	1		31	29						
185	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	1183.0	1.10E+04	1.30E+07	8	8	TX		588.623	1.29E+07	18	119	3.079E+03			18	18						
185	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	1183.0	1.10E+04	1.30E+07	8	9	RX		587.304	1.29E+07	35	147	4.665E+03			35	33	1	1				
185	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	1183.0	1.10E+04	1.30E+07	8	10	TX		588.623	1.29E+07	19	101	2.974E+03			19	19						
185	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	1183.0	1.10E+04	1.30E+07	8	11	RX		588.623	1.29E+07	25	135	3.530E+03			25	25						
185	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	1183.0	1.10E+04	1.30E+07	8	16	TX		588.623	1.29E+07	11	113	2.049E+03			11	11						
185	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	1183.0	1.10E+04	1.30E+07	8	17	RX		586.586	1.29E+07	27	134	3.590E+03			27	24	2		1			
186	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	1134.4	1.05E+04	1.19E+07	1024	0	TX		560.145	1.17E+07	11	128	1.896E+05			11	11						
186	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	1134.4	1.05E+04	1.19E+07	1024	1	RX		530.665	1.11E+07	28	155	4.553E+05	2		28	26						
186	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	1134.4	1.05E+04	1.19E+07	1024	4	TX		560.145	1.17E+07	8	101	2.051E+05			12	12						
186	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	1134.4	1.05E+04	1.19E+07	1024	5	RX		557.852	1.17E+07	27	113	4.226E+05			27	24	2		1			
186	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	1134.4	1.05E+04	1.19E+07	1024	6	TX		560.145	1.17E+07	11	100	1.919E+05			11	11						
186	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	1134.4	1.05E+04	1.19E+07	1024	7	RX		539.935	1.13E+07	25	117	4.086E+05	2		25	23						
186	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	1134.4	1.05E+04	1.19E+07	1024	8	TX		560.145	1.17E+07	13	94	2.162E+05			13	13						
186	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	1134.4	1.05E+04	1.19E+07	1024	9	RX		559.382	1.17E+07	27	107	4.509E+05			27	26		1				
186	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	1134.4	1.05E+04	1.19E+07	1024	10	TX		560.145	1.17E+07	11	91	1.842E+05			11	11						
186	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	1134.4	1.05E+04	1.19E+07	1024	11	RX		524.700	1.10E+07	31	93	5.175E+05	1		31	30						
186	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	1134.4	1.05E+04	1.19E+07	1024	16	TX		560.145	1.17E+07	16	98	2.652E+05			16	16						
186	A4421	40.0	427	Ar	9.5	9.5	142	5@55.8°	0	1134.4	1.05E+04	1.19E+07	1024	17	RX		559.127	1.17E+07	30	127	4.869E+05			30	28	2					
208	A4421	40.0	541	Ne	1.3	1.3	1481	NONE	0	501.9	1.01E+05	5.07E+07	512	0	TX		250.115	5.06E+07	0	14	8.400E+01										
208	A4421	40.0	541	Ne	1.3	1.3	1481	NONE	0	501.9	1.01E+05	5.07E+07	512	1	RX		245.254	4.96E+07	5	55	3.708E+04	1		5	4						
208	A4421	40.0	541	Ne	1.3	1.3	1481	NONE	0	501.9	1.01E+05	5.07E+07	512	4	TX		250.115	5.06E+07	1	13	8.122E+03			1	1						
208	A4421	40.0	541	Ne	1.3	1.3	1481	NONE	0	501.9	1.01E+05	5.07E+07	512	5	RX		248.588	5.02E+07	6	49	3.773E+04			6	3	3					
208	A4421	40.0	541	Ne	1.3	1.3	1481	NONE	0	501.9	1.01E+05	5.07E+07	512	6	TX		250.115	5.06E+07	1	14	7.976E+03			1	1						
208	A4421	40.0	541	Ne	1.3	1.3	1481	NONE	0	501.9	1.01E+05	5.07E+07	512	7	RX		250.115	5.06E+07	4	54	3.384E+04			4	4						
208	A4421	40.0	541	Ne	1.3	1.3	1481	NONE	0	501.9	1.01E+05	5.07E+07	512	8	TX		250.115	5.06E+07	2	15	1.695E+04			2	2						
208	A4421	40.0	541	Ne	1.3	1.3	1481	NONE	0	501.9	1.01E+05	5.07E+07	512	9	RX		250.115	5.06E+07	5	68	4.294E+04			5	5						
208	A4421	40.0	541	Ne	1.3	1.3	1481	NONE	0	501.9	1.01E+05	5.07E+07	512	10	TX		250.115	5.06E+07	2	22	1.699E+04			2	2						
208	A4421	40.0	541	Ne	1.3	1.3	1481	NONE	0	501.9	1.01E+05	5.07E+07	512	11	RX		250.115	5.06E+07	3	51	2.569E+04			3	3						
208	A4421	40.0	541	Ne	1.3	1.3	1481	NONE	0	501.9	1.01E+05	5.07E+07	512	16	TX		250.115	5.06E+07	1	10	8.152E+03			1	1						
208	A4421	40.0	541	Ne	1.3	1.3	1481	NONE	0	501.9	1.01E+05	5.07E+07	512	17	RX		248.842	5.03E+07	6	36	4.172E+04			6	4	1	1				
209	A4421	40.0	541	Ne	1.3	1.3	1481	NONE	0	863.0	5.83E+04	5.03E+07	8	0	TX		430.006	5.01E+07	0	12	4.300E+01										
209	A4421	40.0	541	Ne	1.3	1.3	1481	NONE	0	863.0	5.83E+04	5.03E+07	8	1	RX		430.006	5.01E+07	3	47	4.680E+02			3	3						
209	A4421	40.0	541	Ne	1.3	1.3	1481	NONE	0	863.0	5.83E+04	5.03E+07	8	4	TX		430.006	5.01E+07	2	14	2.910E+02			2	2						
209	A4421	40.0	541	Ne	1.3	1.3	1481	NONE	0	863.0	5.83E+04	5.03E+07	8	5	RX		430.006	5.01E+07	4	56	5.810E+02			4	4						
209	A4421	40.0	541	Ne	1.3	1.3	1481	NONE	0	863.0	5.83E+04	5.03E+07	8	6	TX		430.006	5.01E+07	1	16	2.270E+02			1	1						
209	A4421	40.0	541	Ne	1.3	1.3	1481	NONE	0	863.0	5.83E+04	5.03E+07	8	7	RX		430.006	5.01E+07	8	61	1.005E+03			8	8						
209	A4421	40.0	541	Ne	1.3	1.3	1481	NONE	0	863.0	5.83E+04	5.03E+07	8	8	TX		430.006	5.01E+07	5	16	6.410E+02			5	5						
209	A4421	40.0	541	Ne	1.3	1.3	1481	NONE	0	863.0	5.83E+04	5.03E+07	8	9	RX		430.006	5.01E+07	11	35	1.261E+03			11	11						
209	A4421	40.0	541	Ne	1.3	1.3	1481	NONE	0	863.0	5.83E+04	5.03E+07	8	10	TX		430.006	5.01E+07	3	22	4.720E+02			3	3						
209	A4421	40.0	541	Ne	1.3	1.3	1481	NONE	0	863.0	5.83E+04	5.03E+07	8	11	RX		413.960	4.83E+07	7	48	8.550E+02	1		7	6						
209	A4421	40.0	541	Ne	1.3	1.3	1481	NONE	0	863.0	5.83E+04	5.03E+07	8	16	TX		430.006	5.01E+07	6	12	6.770E+02			6	6						
209	A4421	40.0	541	Ne	1.3	1.3	1481	NONE	0	863.0	5.83E+04	5.03E+07	8	17	RX		428.987	5.00E+07	7	41	7.420E+02			7	5	2					
210	A4421	40.0	750	Ne	1.3	1.3	1481	NONE	0	399.5	1.10E+05	4.41E+07	1024	0	TX		200.012	4.41E+07	2	15	3.295E+04			2	2						
210	A4421	40.0	750	Ne	1.3	1.3	1481	NONE	0	399.5	1.10E+05	4.41E+07	1024	1	RX		177.112	3.91E+07	7	39	1.066E+05			7	6						
210	A4421	40.0	750	Ne	1.3	1.3	1481	NONE	0	399.5	1.10E+05	4.41E+07	1024	4	TX		200.012	4.41E+07	1	12	1.790E+04			1	1						
210	A4421	40.0	750	Ne	1.3	1.3	1481	NONE	0	399.5	1.10E+05	4.41E+07	1024	5	RX		198.484	4.38E+07	12	48	1.802E+05			12	10		2				
210	A4421	40.0	750	Ne	1.3	1.3	1481	NONE	0	399.5	1.10E+05	4.41E+07	1024	6	TX		200.012	4.41E+07	2	16	3.460E+04			2	2						
210	A4421	40.0	750	Ne	1.3	1.3	1481	NONE	0	399.5	1.10E+05	4.41E+07	1024	7	RX		200.012	4.41E+07	2	43	3.393E+04			2	2						
210	A4421	40.0	750	Ne	1.3	1.3	1481	NONE	0	399.5	1.10E+05	4.41E+07	1024	8	TX		200.012	4.41E+07	0	5	1.120E+02										
210	A4421	40.0	750	Ne	1.3	1.3	1481	NONE	0	399.5	1.10E+05	4.41E+07	1024	9	RX		199.503	4.40E+07	5	45	7.584E+04			5	4	1					
210	A4421	40.0	750	Ne	1.3	1.3	1481	NONE	0	399.5	1.10E+05	4.41E+07	1024	10	TX		200.012	4.41E+07	1	13	1.630E+04			1	1						
210	A4421	40.0	750	Ne	1.3	1.3	1481	NONE	0	399.5	1.10E+05	4.41E+07	1024	11	RX		193.546	4.27E+07	6	62	9.459E+04	1		6	5						
210	A4421	40.0	750	Ne	1.3	1.3	1481	NONE	0	399.5	1.10E+05	4.41E+07	1024	16	TX		200.012	4.41E+07	0	12	5.900E+01										
210	A4421	40.0	750	Ne	1.3	1.3	1481	NONE	0	399.5	1.10E+05	4.41E+07	1024	17	RX		200.012	4.41E+07	1	49	1.803E+04			1	1						
211	A4421	40.0	219	Ne	3.2	3.2	1481	6@45°	0	698.1	4.13E+04	2.88E+07	512	0	TX		347.901	2.87E+07	6	23	4.959E+04			6	6						
211	A4421	40.0	219	Ne	3.2	3.2	1481	6@45°	0	698.1	4.13E+04	2.88E+07	512	1	RX		318.871	2.63E+07	14	53	1.209E+05	1		14	13						
211	A4421	40.0	219	Ne	3.2	3.2	1481	6@45°	0	698.1	4.13E+04	2.88E+07	512	4	TX		347.901	2.87E+07	5	32	4.413E+04			5	5						
211	A4421	40.0	219	Ne	3.2	3.2	1481	6@45°	0	698.1	4.13E+04	2.88E+07	512	5	RX		343.984	2.84E+07	15	53	1.201E+05			15	13		1				
211	A4421	40.0	219	Ne	3.2	3.2	1481	6@45°	0	698.1	4.13E+04	2.88E+07	512	6	TX		347.901	2.87E+07	4	26	3.363E+04			4	4						
211	A4421	40.0	219	Ne	3.2	3.2	1481	6@45°	0	698.1	4.13E+04	2.88E+07	512	7	RX		336.283	2.78E+07	18	68	1.453E+05	1		18	16						
211	A4421	40.0	219	Ne	3.2	3.2	1481	6@45°	0	698.1	4.13E+04	2.88E+07	512	8	TX		347.900	2.87E+07	5	16	4.194E+04			5	5						
211	A4421	40.0	219	Ne	3.2	3.2	1481	6@45°	0	698.1	4.13E+04	2.88E+07	512	9	RX		347.900	2.87E+07	8	68	6.685E+04			8	8						
211	A4421	40.0	219	Ne	3.2	3.2	1481	6@45°	0	698.1	4.13E+04	2.88E+07	512	10	TX		347.900	2.87E+07	8	28	6.759E+04			8	8						
211	A4421	40.0	219	Ne	3.2	3.2	1481	6@45°	0	698.1	4.13E+04	2.88E+07	512	11	RX		336.404	2.78E+07	9	57	7.792E+04			9	8						
211	A4421	40.0	219	Ne	3.2	3.2	1481	6@45°	0	698.1	4.13E+04	2.88E+07	512	16	TX		347.901	2.87E+07	5	24	4.603E+04			5	5						
211	A4421	40.0	219	Ne	3.2	3.2	1481	6@45°	0	698.1	4.13E+04	2.88E+07	512	17	RX		347.900	2.87E+07	15	74	1.263E+05			15	15						
212	A4421	40.0	219	Ne	3.2	3.2	193	6@45°	0	727.8	7.54E+04	5.49E+07	8	0	TX		357.052	5.38E+07	10	50	1.447E+03			10	10						
212	A4421	40.0	219	Ne	3.2	3.2	193	6@45°	0	727.8	7.54E+04	5.49E+07	8	1	RX		336.139	5.07E+07	27	117	3.243E+03	2		27	25						
212	A4421	40.0	219	Ne	3.2	3.2	193	6@45°	0	727.8	7.54E+04	5.49E+07	8	4	TX		357.052	5.38E+07	9	44	1.366E+03			9	9						
212	A4421	40.0	219	Ne	3.2	3.2	193	6@45°	0	727.8	7.54E+04	5.49E+07	8	5	RX		356.033	5.37E+07	20	113	2.388E+03			20	18	2					
212	A4421	40.0	219	Ne	3.2	3.2	193	6@45°	0	727.8	7.54E+04	5.49E+07	8	6	TX		357.052	5.38E+07	10	50	1.436E+03			10	10						
212	A4421	40.0	219	Ne	3.2	3.2	193	6@45°	0	727.8	7.54E+04	5.49E+07	8	7	RX		357.052	5.38E+07	17	126	2.153E+03			17	17						
212	A4421	40.0	219	Ne	3.2	3.2	193	6@45°	0	727.8	7.54E+04	5.49E+07	8	8	TX		357.052	5.38E+07	12	57	1.855E+03			12	12						
212	A4421	40.0	219	Ne	3.2	3.2	193	6@45°	0	727.8	7.54E+04	5.49E+07	8	9	RX		357.051	5.38E+07	26	126	3.046E+03			26	26						
212	A4421	40.0	219	Ne	3.2	3.2	193	6@45°	0	727.8	7.54E+04	5.49E+07	8	10	TX		357.052	5.38E+07	16	43	2.102E+03			16	16						
212	A4421	40.0	219	Ne	3.2	3.2	193	6@45°	0	727.8	7.54E+04	5.49E+07	8	11	RX		300.766	4.54E+07	28	89	2.981E+03	4		28	22						
212	A4421	40.0	219	Ne	3.2	3.2	193	6@45°	0	727.8	7.54E+04	5.49E+07	8	16	TX		357.052	5.38E+07	9	49	1.367E+03			9	9						
212	A4421	40.0	219	Ne	3.2	3.2	193	6@45°	0	727.8	7.54E+04	5.49E+07	8	17	RX		355.779	5.36E+07	19	112	2.361E+03			19	17	1	1				

A–2 (Continued)

RUN	SN	ENERGY (MeV/u)	ENERGY (MeV)	ION	LET	EFF LET	EFF RANGE (um)	DEGRADER (#@ANGLE)	DUT ANGLE	RUN TIME (S)	FLUX (p/cm2/s)	FLUENCE (p/cm2)	LOL LEVEL (WORDS)	CHAN	LINK TYPE	ACQUISITION ERRORS?	LINK TIME* (S)	LINK FLUENCE* (p/cm2)	LOL COUNT *	BE COUNT *	BiE COUNT (bits)	GTX RESET LOL COUNT	DRP SCRUB LOL COUNT	LOL EVENT CAPTURES	RESYNC LOL	RX BUFF RST LOL	RX RESET LOL	RX CDR RST LOL	TX RST	SRV RX CDR RST	RESYNC LONG LOL
213	A4421	40.0	219	Ne	3.2	3.2	193	6@45°	0	1420.3	3.62E+04	5.15E+07	1024	0	TX		566.469	4.10E+07	7	37	1.156E+05			7	7						
213	A4421	40.0	219	Ne	3.2	3.2	193	6@45°	0	1420.3	3.62E+04	5.15E+07	1024	1	RX		555.378	4.02E+07	24	98	3.875E+05			24	22	1					
213	A4421	40.0	219	Ne	3.2	3.2	193	6@45°	0	1420.3	3.62E+04	5.15E+07	1024	4	TX		566.487	4.10E+07	4	44	6.637E+04			4	4						
213	A4421	40.0	219	Ne	3.2	3.2	193	6@45°	0	1420.3	3.62E+04	5.15E+07	1024	5	RX		565.983	4.10E+07	20	87	3.265E+05			20	19	1					
213	A4421	40.0	219	Ne	3.2	3.2	193	6@45°	0	1420.3	3.62E+04	5.15E+07	1024	6	TX		566.497	4.10E+07	8	36	1.338E+05			8	8						
213	A4421	40.0	219	Ne	3.2	3.2	193	6@45°	0	1420.3	3.62E+04	5.15E+07	1024	7	RX		565.993	4.10E+07	12	98	1.966E+05			12	11	1					
213	A4421	40.0	219	Ne	3.2	3.2	193	6@45°	0	1420.3	3.62E+04	5.15E+07	1024	8	TX		566.506	4.10E+07	9	37	1.484E+05			9	9						
213	A4421	40.0	219	Ne	3.2	3.2	193	6@45°	0	1420.3	3.62E+04	5.15E+07	1024	9	RX		566.511	4.10E+07	15	89	2.535E+05			15	15						
213	A4421	40.0	219	Ne	3.2	3.2	193	6@45°	0	1420.3	3.62E+04	5.15E+07	1024	10	TX		566.516	4.10E+07	8	25	1.304E+05			8	8						
213	A4421	40.0	219	Ne	3.2	3.2	193	6@45°	0	1420.3	3.62E+04	5.15E+07	1024	11	RX		553.496	4.01E+07	21	68	3.379E+05	2		21	19						
213	A4421	40.0	219	Ne	3.2	3.2	193	6@45°	0	1420.3	3.62E+04	5.15E+07	1024	16	TX		566.448	4.10E+07	6	41	1.049E+05			6	6						
213	A4421	40.0	219	Ne	3.2	3.2	193	6@45°	0	1420.3	3.62E+04	5.15E+07	1024	17	RX		566.453	4.10E+07	16	97	2.696E+05			16	16						
214	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	485.6	1.04E+05	5.05E+07	512	0	TX		234.049	4.87E+07	13	116	1.108E+05			13	13						
214	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	485.6	1.04E+05	5.05E+07	512	1	RX		216.634	4.51E+07	35	220	2.709E+05	1		31	26	2					
214	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	485.6	1.04E+05	5.05E+07	512	4	TX		234.049	4.87E+07	11	118	1.015E+05			11	11						
214	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	485.6	1.04E+05	5.05E+07	512	5	RX		225.981	4.70E+07	42	184	3.288E+05			42	35	5	1				
214	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	485.6	1.04E+05	5.05E+07	512	6	TX		234.049	4.87E+07	9	107	8.129E+04			9	9						
214	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	485.6	1.04E+05	5.05E+07	512	7	RX		206.516	4.30E+07	34	206	2.668E+05	3		33	30	1					
214	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	485.6	1.04E+05	5.05E+07	512	8	TX		234.049	4.87E+07	14	115	1.201E+05			14	14						
214	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	485.6	1.04E+05	5.05E+07	512	9	RX		229.975	4.78E+07	45	226	3.572E+05			45	40		4	1			
214	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	485.6	1.04E+05	5.05E+07	512	10	TX		234.049	4.87E+07	14	108	1.234E+05			14	14						
214	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	485.6	1.04E+05	5.05E+07	512	11	RX		167.898	3.49E+07	47	176	3.633E+05	4		46	41						
214	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	485.6	1.04E+05	5.05E+07	512	16	TX		234.049	4.87E+07	16	184	1.340E+05			16	16						
214	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	485.6	1.04E+05	5.05E+07	512	17	RX	A	225.510	4.69E+07	65491	-644	2.480E+09	1									
215	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	576.7	8.73E+04	5.04E+07	8	0	TX		283.453	4.95E+07	18	96	2.670E+03			18	18						
215	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	576.7	8.73E+04	5.04E+07	8	1	RX		260.738	4.55E+07	45	204	5.361E+03	1		45	41		1				
215	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	576.7	8.73E+04	5.04E+07	8	4	TX		283.452	4.95E+07	18	110	2.759E+03			18	18						
215	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	576.7	8.73E+04	5.04E+07	8	5	RX		277.400	4.85E+07	55	193	6.140E+03			55	47	3	4	1			
215	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	576.7	8.73E+04	5.04E+07	8	6	TX		283.452	4.95E+07	19	119	2.954E+03			19	19						
215	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	576.7	8.73E+04	5.04E+07	8	7	RX		260.142	4.54E+07	36	205	4.624E+03	2		36	32						
215	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	576.7	8.73E+04	5.04E+07	8	8	TX		283.453	4.95E+07	10	111	1.865E+03			10	10						
215	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	576.7	8.73E+04	5.04E+07	8	9	RX		275.092	4.81E+07	39	196	4.541E+03	1		39	32	3	2	1			
215	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	576.7	8.73E+04	5.04E+07	8	10	TX		283.453	4.95E+07	7	88	1.474E+03			7	7						
215	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	576.7	8.73E+04	5.04E+07	8	11	RX		255.495	4.46E+07	41	203	4.963E+03	2		41	36		1				1
215	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	576.7	8.73E+04	5.04E+07	8	16	TX		283.452	4.95E+07	26	174	4.446E+03			26	26						
215	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	576.7	8.73E+04	5.04E+07	8	17	RX		279.378	4.88E+07	59	276	7.629E+03			59	53	3	2	1			
216	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	535.3	9.53E+04	5.10E+07	1024	0	TX		265.731	5.07E+07	17	110	2.839E+05			17	17						
216	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	535.3	9.53E+04	5.10E+07	1024	1	RX		247.399	4.72E+07	41	190	6.555E+05	2		41	37	1					
216	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	535.3	9.53E+04	5.10E+07	1024	4	TX		265.731	5.07E+07	17	102	2.847E+05			17	17						
216	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	535.3	9.53E+04	5.10E+07	1024	5	RX		261.913	4.99E+07	33	211	5.252E+05			33	27	3	3				
216	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	535.3	9.53E+04	5.10E+07	1024	6	TX		265.731	5.07E+07	15	106	2.486E+05			15	15						
216	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	535.3	9.53E+04	5.10E+07	1024	7	RX		243.217	4.64E+07	43	176	6.728E+05	2		43	38		1			1	
216	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	535.3	9.53E+04	5.10E+07	1024	8	TX		265.731	5.07E+07	15	110	2.563E+05			15	15						
216	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	535.3	9.53E+04	5.10E+07	1024	9	RX		262.930	5.01E+07	39	228	6.124E+05			39	34	4	1				
216	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	535.3	9.53E+04	5.10E+07	1024	10	TX		265.731	5.07E+07	14	131	2.400E+05			14	14						
216	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	535.3	9.53E+04	5.10E+07	1024	11	RX		252.188	4.81E+07	36	192	5.712E+05	2		36	32	1					
216	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	535.3	9.53E+04	5.10E+07	1024	16	TX		265.731	5.07E+07	16	169	2.702E+05			16	16						
216	A4421	40.0	62	Ne	6.6	6.6	33.9	6@45°	0	535.3	9.53E+04	5.10E+07	1024	17	RX		263.949	5.03E+07	47	266	7.595E+05			47	44	2	1				

a) Channel data scratched, oscillatory event.
b) Channel data scratched, Corrupted SYNC_TIME counts in Service.
c) Bug in Service FPGA required a Reset of the Service FPGA, corrected by only accounting events up to the Reset.
d) Service Log File was corrupt, only LOL Event data available.
e) Channel data scratched, event required Service TX MGT Tile of channel to be continuously reset, corrupted the data.

Appendix B : CRÈME-MC Estimate Procedure

CRÈME-MC is web-based SW tool (12) that generates device upset estimates at different satellite orbits. It utilizes the industry accepted protons, electrons and heavy ion models, as well as modeling the shielding of the earth's geo-magnetic fields, to obtain upset rates. It also generates flux and fluence curves after transport through shielding using simple spherical-shield transport models. CRÈME-MC was used to generate all of the orbit upset rate estimates, and each of the CRÈME routine modules were set up as follows:

- Trapped Proton Fluxes (TRP) – *Not used*
- Geomagnetic Transmission Routine (GTRN) - *Not used*
- Space Ionizing Radiation Motel at Spacecraft Surface (FLUX)

Atomic number of lightest element included	2
Atomic number of heaviest element included	92
Nominal Environment Model GCR	Solar Minimum
Spacecraft Location	Outside Earth's Magnetosphere
Include Trapped Protons	No

- Nuclear Transport Routine Though Space Craft Shielding (TRANS)

Shielding material	Aluminum
Shield thickness	0.150 inches

- Linear Energy Transfer (LET) Spectra (LETSPEC)

Atomic number of lightest element included	2
Atomic number of heaviest element included	92
Minimum Energy value	0.1 MeV/nuc
Device material	Silicon

- Direct-Ionization-Induced Single Event Upset (SEU) Rate User-Supplied Parameters (HUP)

  The Weibull parameters utilized for each event are listed in Table 14 on page 57. The HUP routine utilizes the output of LETSPEC routine to obtain the upset rates due to heavy ions. The LETSPEC function uses the output of the TRANS routine. For all events the Rectangular Parallel-Piped model parameters X, Y, Z and funnel depth are 0, 0, 1.0µm and 0, respectively.

Appendix C : Cross-Section vs. LET Calculations

For each run and each channel, upper and lower errors are extracted depending on count size (σ_i). The XRTC employs a Poisson distribution table with 0.01 statistical significance and 3σ error bars to obtain the positive and negative errors for all the experimental counts obtained.

The cross-section per cm^2 is obtained dividing the event counts by the corrected fluence of each run, which is shown in Appendix A. For all of the runs with equivalent LET, the final cross-section data point is obtained by averaging all the TX and RX channels. The error per cross-section data point is obtained by weighing out each of the channel's positive and negative Poisson error by utilizing the formula for weighted average error of a mean or the variance of a mean (13).

$$\sigma_{\mu}^{2} = \frac{1}{\Sigma\left[{}^{1}/_{\sigma_i^2}\right]} \qquad (2)$$

Appendix D : Test GTX Tile Instantiation

```
gtx_dual_i:GTX_DUAL
    generic map (

        --Simulation-Only Attributes
        SIM_RECEIVER_DETECT_PASS_0  =>       TRUE,
        SIM_RECEIVER_DETECT_PASS_1  =>       TRUE,
        SIM_MODE                    =>       TILE_SIM_MODE,
        SIM_GTXRESET_SPEEDUP        =>       TILE_SIM_GTXRESET_SPEEDUP,
        SIM_PLL_PERDIV2             =>       TILE_SIM_PLL_PERDIV2,


        -- SHARED ATTRIBUTES
        -------------------------- Tile and PLL Attributes ---------------------
        CLK25_DIVIDER               =>       10,
        CLKINDC_B                   =>       TRUE,
        CLKRCV_TRST                 =>       TRUE,
        OOB_CLK_DIVIDER             =>       6,
        OVERSAMPLE_MODE             =>       FALSE,
        PLL_COM_CFG                 =>       x"21680a",
        PLL_CP_CFG                  =>       x"00",
        PLL_DIVSEL_FB               =>       2,
        PLL_DIVSEL_REF              =>       1,
        PLL_FB_DCCEN                =>       FALSE,
        PLL_LKDET_CFG               =>       "101",
        PLL_TDCC_CFG                =>       "000",
        PMA_COM_CFG                 =>       x"000000000000000000",

        -- TRANSMIT INTERFACE ATTRIBUTES
        ------------------- TX Buffering and Phase Alignment -------------------
        TX_BUFFER_USE_0             =>       TRUE,
        TX_XCLK_SEL_0               =>       "TXOUT",
        TXRX_INVERT_0               =>       "011",
        TX_BUFFER_USE_1             =>       TRUE,
        TX_XCLK_SEL_1               =>       "TXOUT",
        TXRX_INVERT_1               =>       "011",
        --------------------- TX Gearbox Settings ----------------------------
        GEARBOX_ENDEC_0             =>       "000",
        TXGEARBOX_USE_0            =>        FALSE,
        GEARBOX_ENDEC_1            =>        "000",
        TXGEARBOX_USE_1            =>        FALSE,
        --------------------- TX Serial Line Rate settings ---------------------
        PLL_TXDIVSEL_OUT_0          =>       1,
        PLL_TXDIVSEL_OUT_1          =>       1,
        --------------------- TX Driver and OOB signalling --------------------
        CM_TRIM_0                   =>       "10",
        PMA_TX_CFG_0                =>       x"80082",
        TX_DETECT_RX_CFG_0          =>       x"1832",
        TX_IDLE_DELAY_0             =>       "010",
        CM_TRIM_1                   =>       "10",
        PMA_TX_CFG_1                =>       x"80082",
        TX_DETECT_RX_CFG_1          =>       x"1832",
        TX_IDLE_DELAY_1             =>       "010",
        ------------------ TX Pipe Control for PCI Express/SATA ---------------
        COM_BURST_VAL_0             =>       "1111",
        COM_BURST_VAL_1             =>       "1111",

        --Receive Interface Attributes _________________
        ------------ RX Driver,OOB signalling,Coupling and Eq,CDR -------------
        AC_CAP_DIS_0                =>       TRUE,
```

```
OOBDETECT_THRESHOLD_0       =>       "111",
PMA_CDR_SCAN_0              =>       x"640403a",
PMA_RX_CFG_0                =>       x"0f44088",
RCV_TERM_GND_0              =>       FALSE,
RCV_TERM_VTTRX_0            =>       TRUE,
TERMINATION_IMP_0           =>       50,
AC_CAP_DIS_1                =>       TRUE,
OOBDETECT_THRESHOLD_1       =>       "111",
PMA_CDR_SCAN_1              =>       x"640403a",
PMA_RX_CFG_1                =>       x"0f44088",
RCV_TERM_GND_1              =>       FALSE,
RCV_TERM_VTTRX_1            =>       TRUE,
TERMINATION_IMP_1           =>       50,
TERMINATION_CTRL            =>       "10100",
TERMINATION_OVRD            =>       FALSE,
---------------- RX Decision Feedback Equalizer(DFE)  ----------------
DFE_CFG_0                   =>       "1001111011",
DFE_CFG_1                   =>       "1001111011",
DFE_CAL_TIME                =>       "00110",
--------------------- RX Serial Line Rate Attributes ------------------
PLL_RXDIVSEL_OUT_0          =>       1,
PLL_SATA_0                  =>       FALSE,
PLL_RXDIVSEL_OUT_1          =>       1,
PLL_SATA_1                  =>       FALSE,
------------------------ PRBS Detection Attributes ---------------------
PRBS_ERR_THRESHOLD_0        =>       x"00000001",
PRBS_ERR_THRESHOLD_1        =>       x"00000001",
---------------- Comma Detection and Alignment Attributes -------------
ALIGN_COMMA_WORD_0          =>       2,
COMMA_10B_ENABLE_0          =>       "1111111111",
COMMA_DOUBLE_0              =>       FALSE,
DEC_MCOMMA_DETECT_0         =>       TRUE,
DEC_PCOMMA_DETECT_0         =>       TRUE,
DEC_VALID_COMMA_ONLY_0      =>       TRUE,
MCOMMA_10B_VALUE_0          =>       "1010000011",-- ~K28.5 (RD +)
MCOMMA_DETECT_0             =>       TRUE,
PCOMMA_10B_VALUE_0          =>       "0101111100",-- ~K28.5 (RD -)
PCOMMA_DETECT_0             =>       TRUE,
RX_SLIDE_MODE_0             =>       "PCS",
ALIGN_COMMA_WORD_1          =>       2,
COMMA_10B_ENABLE_1          =>       "1111111111",
COMMA_DOUBLE_1              =>       FALSE,
DEC_MCOMMA_DETECT_1         =>       TRUE,
DEC_PCOMMA_DETECT_1         =>       TRUE,
DEC_VALID_COMMA_ONLY_1      =>       TRUE,
MCOMMA_10B_VALUE_1          =>       "1010000011",-- ~K28.5 (RD +)
MCOMMA_DETECT_1             =>       TRUE,
PCOMMA_10B_VALUE_1          =>       "0101111100",-- ~K28.5 (RD -)
PCOMMA_DETECT_1             =>       TRUE,
RX_SLIDE_MODE_1             =>       "PCS",
------------------ RX Loss-of-sync State Machine Attributes -----------
RX_LOSS_OF_SYNC_FSM_0       =>       FALSE,
RX_LOS_INVALID_INCR_0       =>       1,
RX_LOS_THRESHOLD_0          =>       4,
RX_LOSS_OF_SYNC_FSM_1       =>       FALSE,
RX_LOS_INVALID_INCR_1       =>       1,
RX_LOS_THRESHOLD_1          =>       4,
--------------------- RX Gearbox Settings ----------------------------
RXGEARBOX_USE_0             =>       FALSE,
RXGEARBOX_USE_1             =>       FALSE,
-------------- RX Elastic Buffer and Phase alignment Attributes -------
PMA_RXSYNC_CFG_0            =>       x"00",
RX_BUFFER_USE_0             =>       TRUE,
RX_XCLK_SEL_0               =>       "RXREC",
PMA_RXSYNC_CFG_1            =>       x"00",
RX_BUFFER_USE_1             =>       TRUE,
RX_XCLK_SEL_1               =>       "RXREC",
```

```
------------------------ Clock Correction Attributes ------------------
CLK_CORRECT_USE_0           =>       FALSE,
CLK_COR_ADJ_LEN_0           =>       1,
CLK_COR_DET_LEN_0           =>       1,
CLK_COR_INSERT_IDLE_FLAG_0  =>       FALSE,
CLK_COR_KEEP_IDLE_0         =>       FALSE,
CLK_COR_MAX_LAT_0           =>       30,
CLK_COR_MIN_LAT_0           =>       28,
CLK_COR_PRECEDENCE_0        =>       TRUE,
CLK_COR_REPEAT_WAIT_0       =>       0,
CLK_COR_SEQ_1_1_0           =>       "0100011100",
CLK_COR_SEQ_1_2_0           =>       "0000000000",
CLK_COR_SEQ_1_3_0           =>       "0000000000",
CLK_COR_SEQ_1_4_0           =>       "0000000000",
CLK_COR_SEQ_1_ENABLE_0      =>       "0000",
CLK_COR_SEQ_2_1_0           =>       "0000000000",
CLK_COR_SEQ_2_2_0           =>       "0000000000",
CLK_COR_SEQ_2_3_0           =>       "0000000000",
CLK_COR_SEQ_2_4_0           =>       "0000000000",
CLK_COR_SEQ_2_ENABLE_0      =>       "0000",
CLK_COR_SEQ_2_USE_0         =>       FALSE,
RX_DECODE_SEQ_MATCH_0       =>       TRUE,
CLK_CORRECT_USE_1           =>       FALSE,
CLK_COR_ADJ_LEN_1           =>       1,
CLK_COR_DET_LEN_1           =>       1,
CLK_COR_INSERT_IDLE_FLAG_1  =>       FALSE,
CLK_COR_KEEP_IDLE_1         =>       FALSE,
CLK_COR_MAX_LAT_1           =>       30,
CLK_COR_MIN_LAT_1           =>       28,
CLK_COR_PRECEDENCE_1        =>       TRUE,
CLK_COR_REPEAT_WAIT_1       =>       0,
CLK_COR_SEQ_1_1_1           =>       "0100011100",
CLK_COR_SEQ_1_2_1           =>       "0000000000",
CLK_COR_SEQ_1_3_1           =>       "0000000000",
CLK_COR_SEQ_1_4_1           =>       "0000000000",
CLK_COR_SEQ_1_ENABLE_1      =>       "0000",
CLK_COR_SEQ_2_1_1           =>       "0000000000",
CLK_COR_SEQ_2_2_1           =>       "0000000000",
CLK_COR_SEQ_2_3_1           =>       "0000000000",
CLK_COR_SEQ_2_4_1           =>       "0000000000",
CLK_COR_SEQ_2_ENABLE_1      =>       "0000",
CLK_COR_SEQ_2_USE_1         =>       FALSE,
RX_DECODE_SEQ_MATCH_1       =>       TRUE,
------------------------ Channel Bonding Attributes -------------------
CB2_INH_CC_PERIOD_0         =>       8,
CHAN_BOND_1_MAX_SKEW_0      =>       1,
CHAN_BOND_2_MAX_SKEW_0      =>       1,
CHAN_BOND_KEEP_ALIGN_0      =>       FALSE,
CHAN_BOND_LEVEL_0           =>       TILE_CHAN_BOND_LEVEL_0,
CHAN_BOND_MODE_0            =>       TILE_CHAN_BOND_MODE_0,
CHAN_BOND_SEQ_1_1_0         =>       "0101111100",
CHAN_BOND_SEQ_1_2_0         =>       "0000000000",
CHAN_BOND_SEQ_1_3_0         =>       "0000000000",
CHAN_BOND_SEQ_1_4_0         =>       "0000000000",
CHAN_BOND_SEQ_1_ENABLE_0    =>       "0000",
CHAN_BOND_SEQ_2_1_0         =>       "0000000000",
CHAN_BOND_SEQ_2_2_0         =>       "0000000000",
CHAN_BOND_SEQ_2_3_0         =>       "0000000000",
CHAN_BOND_SEQ_2_4_0         =>       "0000000000",
CHAN_BOND_SEQ_2_ENABLE_0    =>       "0000",
CHAN_BOND_SEQ_2_USE_0       =>       FALSE,
CHAN_BOND_SEQ_LEN_0         =>       1,
PCI_EXPRESS_MODE_0          =>       FALSE,
CB2_INH_CC_PERIOD_1         =>       8,
CHAN_BOND_1_MAX_SKEW_1      =>       1,
CHAN_BOND_2_MAX_SKEW_1      =>       1,
CHAN_BOND_KEEP_ALIGN_1      =>       FALSE,
```

```
      CHAN_BOND_LEVEL_1           =>       TILE_CHAN_BOND_LEVEL_1,
      CHAN_BOND_MODE_1            =>       TILE_CHAN_BOND_MODE_1,
      CHAN_BOND_SEQ_1_1_1         =>       "0101111100",
      CHAN_BOND_SEQ_1_2_1         =>       "0000000000",
      CHAN_BOND_SEQ_1_3_1         =>       "0000000000",
      CHAN_BOND_SEQ_1_4_1         =>       "0000000000",
      CHAN_BOND_SEQ_1_ENABLE_1    =>       "0000",
      CHAN_BOND_SEQ_2_1_1         =>       "0000000000",
      CHAN_BOND_SEQ_2_2_1         =>       "0000000000",
      CHAN_BOND_SEQ_2_3_1         =>       "0000000000",
      CHAN_BOND_SEQ_2_4_1         =>       "0000000000",
      CHAN_BOND_SEQ_2_ENABLE_1    =>       "0000",
      CHAN_BOND_SEQ_2_USE_1       =>       FALSE,
      CHAN_BOND_SEQ_LEN_1         =>       1,
      PCI_EXPRESS_MODE_1          =>       FALSE,
      -------- RX Attributes to Control Reset after Electrical Idle  ------
      RX_EN_IDLE_HOLD_DFE_0       =>       TRUE,
      RX_EN_IDLE_RESET_BUF_0      =>       TRUE,
      RX_IDLE_HI_CNT_0            =>       "1000",
      RX_IDLE_LO_CNT_0            =>       "0000",
      RX_EN_IDLE_HOLD_DFE_1       =>       TRUE,
      RX_EN_IDLE_RESET_BUF_1      =>       TRUE,
      RX_IDLE_HI_CNT_1            =>       "1000",
      RX_IDLE_LO_CNT_1            =>       "0000",
      CDR_PH_ADJ_TIME             =>       "01010",
      RX_EN_IDLE_RESET_FR         =>       TRUE,
      RX_EN_IDLE_HOLD_CDR         =>       FALSE,
      RX_EN_IDLE_RESET_PH         =>       TRUE,
      ------------------ RX Attributes for PCI Express/SATA ---------------
      RX_STATUS_FMT_0             =>       "PCIE",
      SATA_BURST_VAL_0            =>       "100",
      SATA_IDLE_VAL_0             =>       "100",
      SATA_MAX_BURST_0            =>       7,
      SATA_MAX_INIT_0             =>       22,
      SATA_MAX_WAKE_0             =>       7,
      SATA_MIN_BURST_0            =>       4,
      SATA_MIN_INIT_0             =>       12,
      SATA_MIN_WAKE_0             =>       4,
      TRANS_TIME_FROM_P2_0        =>       x"003c",
      TRANS_TIME_NON_P2_0         =>       x"0019",
      TRANS_TIME_TO_P2_0          =>       x"0064",
      RX_STATUS_FMT_1             =>       "PCIE",
      SATA_BURST_VAL_1            =>       "100",
      SATA_IDLE_VAL_1             =>       "100",
      SATA_MAX_BURST_1            =>       7,
      SATA_MAX_INIT_1             =>       22,
      SATA_MAX_WAKE_1             =>       7,
      SATA_MIN_BURST_1            =>       4,
      SATA_MIN_INIT_1             =>       12,
      SATA_MIN_WAKE_1             =>       4,
      TRANS_TIME_FROM_P2_1        =>       x"003c",
      TRANS_TIME_NON_P2_1         =>       x"0019",
      TRANS_TIME_TO_P2_1          =>       x"0064")

  port map(
      ------------------------ Loopback and Power-down Ports ----------------------
      LOOPBACK0                       =>     "000",
      LOOPBACK1                       =>     "000",
      RXPOWERDOWN0                    =>      gtx_pwrdown_vec,
      RXPOWERDOWN1                    =>      gtx_pwrdown_vec,
      TXPOWERDOWN0                    =>      gtx_pwrdown_vec,
      TXPOWERDOWN1                    =>      gtx_pwrdown_vec,
      -------------- Receive Ports - 64b66b and 64b67b Gearbox Ports -------------
      RXDATAVALID0                    =>      open,
      RXDATAVALID1                    =>      open,
      RXGEARBOXSLIP0                  =>      tied_to_ground_i,
      RXGEARBOXSLIP1                  =>      tied_to_ground_i,
```

```
RXHEADER0                       =>      open,
RXHEADER1                       =>      open,
RXHEADERVALID0                  =>      open,
RXHEADERVALID1                  =>      open,
RXSTARTOFSEQ0                   =>      open,
RXSTARTOFSEQ1                   =>      open,
----------------------- Receive Ports - 8b10b Decoder ----------------------
RXCHARISCOMMA0                  =>      RXCHARISCOMMA0_OUT,
RXCHARISCOMMA1                  =>      RXCHARISCOMMA1_OUT,
RXCHARISK0                      =>      RXCHARISK0_OUT,
RXCHARISK1                      =>      RXCHARISK1_OUT,
RXDEC8B10BUSE0                  =>      tied_to_vcc_i,
RXDEC8B10BUSE1                  =>      tied_to_vcc_i,
RXDISPERR0                      =>      open,
RXDISPERR1                      =>      open,
RXNOTINTABLE0                   =>      open,
RXNOTINTABLE1                   =>      open,
RXRUNDISP0                      =>      open,
RXRUNDISP1                      =>      open,
------------------- Receive Ports - Channel Bonding Ports ------------------
RXCHANBONDSEQ0                  =>      open,
RXCHANBONDSEQ1                  =>      open,
RXCHBONDI0                      =>      tied_to_ground_vec_i(3 downto 0),
RXCHBONDI1                      =>      tied_to_ground_vec_i(3 downto 0),
RXCHBONDO0                      =>      open,
RXCHBONDO1                      =>      open,
RXENCHANSYNC0                   =>      tied_to_ground_i,
RXENCHANSYNC1                   =>      tied_to_ground_i,
------------------- Receive Ports - Clock Correction Ports -----------------
RXCLKCORCNT0                    =>      open,
RXCLKCORCNT1                    =>      open,
--------------- Receive Ports - Comma Detection and Alignment --------------
RXBYTEISALIGNED0                =>      open,
RXBYTEISALIGNED1                =>      open,
RXBYTEREALIGN0                  =>      open,
RXBYTEREALIGN1                  =>      open,
RXCOMMADET0                     =>      open,
RXCOMMADET1                     =>      open,
RXCOMMADETUSE0                  =>      tied_to_vcc_i,
RXCOMMADETUSE1                  =>      tied_to_vcc_i,
RXENMCOMMAALIGN0                =>      '1',
RXENMCOMMAALIGN1                =>      '1',
RXENPCOMMAALIGN0                =>      '1',
RXENPCOMMAALIGN1                =>      '1',
RXSLIDE0                        =>      tied_to_ground_i,
RXSLIDE1                        =>      tied_to_ground_i,
----------------------- Receive Ports - PRBS Detection ---------------------
PRBSCNTRESET0                   =>      tied_to_ground_i,
PRBSCNTRESET1                   =>      tied_to_ground_i,
RXENPRBSTST0                    =>      tied_to_ground_vec_i(1 downto 0),
RXENPRBSTST1                    =>      tied_to_ground_vec_i(1 downto 0),
RXPRBSERR0                      =>      open,
RXPRBSERR1                      =>      open,
------------------- Receive Ports - RX Data Path interface -----------------
RXDATA0                         =>      rxdata0_i,
RXDATA1                         =>      rxdata1_i,
RXDATAWIDTH0                    =>      "10",
RXDATAWIDTH1                    =>      "10",
RXRECCLK0                       =>      open,
RXRECCLK1                       =>      open,
RXRESET0                        =>      RXRESET0_IN,
RXRESET1                        =>      RXRESET1_IN,
RXUSRCLK0                       =>      slow_user_clk,,
RXUSRCLK1                       =>      slow_user_clk,,
RXUSRCLK20                      =>      fast_user_clk,,
RXUSRCLK21                      =>      fast_user_clk,,
------------ Receive Ports - RX Decision Feedback Equalizer(DFE) -----------
```

```
DFECLKDLYADJ0                   =>      tied_to_ground_vec_i(5 downto 0),
DFECLKDLYADJ1                   =>      tied_to_ground_vec_i(5 downto 0),
DFECLKDLYADJMONITOR0            =>      open,
DFECLKDLYADJMONITOR1            =>      open,
DFEEYEDACMONITOR0               =>      open,
DFEEYEDACMONITOR1               =>      open,
DFESENSCAL0                     =>      open,
DFESENSCAL1                     =>      open,
DFETAP10                        =>      tied_to_ground_vec_i(4 downto 0),
DFETAP11                        =>      tied_to_ground_vec_i(4 downto 0),
DFETAP1MONITOR0                 =>      open,
DFETAP1MONITOR1                 =>      open,
DFETAP20                        =>      tied_to_ground_vec_i(4 downto 0),
DFETAP21                        =>      tied_to_ground_vec_i(4 downto 0),
DFETAP2MONITOR0                 =>      open,
DFETAP2MONITOR1                 =>      open,
DFETAP30                        =>      tied_to_ground_vec_i(3 downto 0),
DFETAP31                        =>      tied_to_ground_vec_i(3 downto 0),
DFETAP3MONITOR0                 =>      open,
DFETAP3MONITOR1                 =>      open,
DFETAP40                        =>      tied_to_ground_vec_i(3 downto 0),
DFETAP41                        =>      tied_to_ground_vec_i(3 downto 0),
DFETAP4MONITOR0                 =>      open,
DFETAP4MONITOR1                 =>      open,
------- Receive Ports - RX Driver,OOB signalling,Coupling and Eq.,CDR ------
RXCDRRESET0                     =>      RXCDRRESET0_IN,
RXCDRRESET1                     =>      RXCDRRESET1_IN,
RXELECIDLE0                     =>      open,
RXELECIDLE1                     =>      open,
RXENEQB0                        =>      tied_to_ground_i,
RXENEQB1                        =>      tied_to_ground_i,
RXEQMIX0                        =>      "11",
RXEQMIX1                        =>      "11",
RXEQPOLE0                       =>      "0000",
RXEQPOLE1                       =>      "0000",
RXN0                            =>      RXN0_IN,
RXN1                            =>      RXN1_IN,
RXP0                            =>      RXP0_IN,
RXP1                            =>      RXP1_IN,
-------- Receive Ports - RX Elastic Buffer and Phase Alignment Ports -------
RXBUFRESET0                     =>      RXBUFRESET0_IN,
RXBUFRESET1                     =>      RXBUFRESET1_IN,
RXBUFSTATUS0                    =>      RXBUFSTATUS0_OUT,
RXBUFSTATUS1                    =>      RXBUFSTATUS1_OUT,
RXCHANISALIGNED0                =>      open,
RXCHANISALIGNED1                =>      open,
RXCHANREALIGN0                  =>      open,
RXCHANREALIGN1                  =>      open,
RXENPMAPHASEALIGN0              =>      tied_to_ground_i,
RXENPMAPHASEALIGN1              =>      tied_to_ground_i,
RXPMASETPHASE0                  =>      tied_to_ground_i,
RXPMASETPHASE1                  =>      tied_to_ground_i,
RXSTATUS0                       =>      open,
RXSTATUS1                       =>      open,
--------------- Receive Ports - RX Loss-of-sync State Machine --------------
RXLOSSOFSYNC0                   =>      RXLOSSOFSYNC0_OUT,
RXLOSSOFSYNC1                   =>      RXLOSSOFSYNC1_OUT,
---------------------- Receive Ports - RX Oversampling ---------------------
RXENSAMPLEALIGN0                =>      tied_to_ground_i,
RXENSAMPLEALIGN1                =>      tied_to_ground_i,
RXOVERSAMPLEERR0                =>      open,
RXOVERSAMPLEERR1                =>      open,
-------------- Receive Ports - RX Pipe Control for PCI Express -------------
PHYSTATUS0                      =>      open,
PHYSTATUS1                      =>      open,
RXVALID0                        =>      open,
RXVALID1                        =>      open,
```

```
---------------- Receive Ports - RX Polarity Control Ports ----------------
RXPOLARITY0                     =>      tied_to_ground_i,
RXPOLARITY1                     =>      tied_to_ground_i,
------------- Shared Ports - Dynamic Reconfiguration Port (DRP) ------------
DADDR                           =>      tied_to_ground_vec_i(6 downto 0),
DCLK                            =>      tied_to_ground_i,
DEN                             =>      tied_to_ground_i,
DI                              =>      tied_to_ground_vec_i(15 downto 0),
DO                              =>      open,
DRDY                            =>      open,
DWE                             =>      tied_to_ground_i,
--------------------- Shared Ports - Tile and PLL Ports --------------------
CLKIN                           =>      CLKIN_IN,
GTXRESET                        =>      GTXRESET_IN,
GTXTEST                         =>      "10000000000000",
INTDATAWIDTH                    =>      tied_to_vcc_i,
PLLLKDET                        =>      PLLLKDET_OUT,
PLLLKDETEN                      =>      tied_to_vcc_i,
PLLPOWERDOWN                    =>      pll_pwrdown_cmd,
REFCLKOUT                       =>      REFCLKOUT_OUT,
REFCLKPWRDNB                    =>      gtx_pwrdownf,
RESETDONE0                      =>      RESETDONE0_OUT,
RESETDONE1                      =>      RESETDONE1_OUT,
-------------- Transmit Ports - 64b66b and 64b67b Gearbox Ports ------------
TXGEARBOXREADY0                 =>      open,
TXGEARBOXREADY1                 =>      open,
TXHEADER0                       =>      tied_to_ground_vec_i(2 downto 0),
TXHEADER1                       =>      tied_to_ground_vec_i(2 downto 0),
TXSEQUENCE0                     =>      tied_to_ground_vec_i(6 downto 0),
TXSEQUENCE1                     =>      tied_to_ground_vec_i(6 downto 0),
TXSTARTSEQ0                     =>      tied_to_ground_i,
TXSTARTSEQ1                     =>      tied_to_ground_i,
---------------- Transmit Ports - 8b10b Encoder Control Ports --------------
TXBYPASS8B10B0                  =>      tied_to_ground_vec_i(3 downto 0),
TXBYPASS8B10B1                  =>      tied_to_ground_vec_i(3 downto 0),
TXCHARDISPMODE0                 =>      tied_to_ground_vec_i(3 downto 0),
TXCHARDISPMODE1                 =>      tied_to_ground_vec_i(3 downto 0),
TXCHARDISPVAL0                  =>      tied_to_ground_vec_i(3 downto 0),
TXCHARDISPVAL1                  =>      tied_to_ground_vec_i(3 downto 0),
TXCHARISK0                      =>      TXCHARISK0_IN,
TXCHARISK1                      =>      TXCHARISK1_IN,
TXENC8B10BUSE0                  =>      tied_to_vcc_i,
TXENC8B10BUSE1                  =>      tied_to_vcc_i,
TXKERR0                         =>      open,
TXKERR1                         =>      open,
TXRUNDISP0                      =>      open,
TXRUNDISP1                      =>      open,
------------- Transmit Ports - TX Buffering and Phase Alignment ------------
TXBUFSTATUS0                    =>      TXBUFSTATUS0_OUT,
TXBUFSTATUS1                    =>      TXBUFSTATUS1_OUT,
------------------ Transmit Ports - TX Data Path interface -----------------
TXDATA0                         =>      txdata0_i,
TXDATA1                         =>      txdata1_i,
TXDATAWIDTH0                    =>      "10",
TXDATAWIDTH1                    =>      "10",
TXOUTCLK0                       =>      open,
TXOUTCLK1                       =>      open,
TXRESET0                        =>      dut_lane_txreset_cmd(0),
TXRESET1                        =>      dut_lane_txreset_cmd(1),
TXUSRCLK0                       =>      slow_user_clk,
TXUSRCLK1                       =>      slow_user_clk,
TXUSRCLK20                      =>      fast_user_clk,
TXUSRCLK21                      =>      fast_user_clk,
--------------- Transmit Ports - TX Driver and OOB signalling --------------
TXBUFDIFFCTRL0                  =>      "101",
TXBUFDIFFCTRL1                  =>      "101",
TXDIFFCTRL0                     =>      "011",
```

```
TXDIFFCTRL1                     =>      "011",
TXINHIBIT0                      =>      tied_to_ground_i,
TXINHIBIT1                      =>      tied_to_ground_i,
TXN0                            =>      TXN0_OUT,
TXN1                            =>      TXN1_OUT,
TXP0                            =>      TXP0_OUT,
TXP1                            =>      TXP1_OUT,
TXPREEMPHASIS0                  =>      "0011",
TXPREEMPHASIS1                  =>      "0011",
-------- Transmit Ports - TX Elastic Buffer and Phase Alignment Ports ------
TXENPMAPHASEALIGN0              =>      tied_to_ground_i,
TXENPMAPHASEALIGN1              =>      tied_to_ground_i,
TXPMASETPHASE0                  =>      tied_to_ground_i,
TXPMASETPHASE1                  =>      tied_to_ground_i,
--------------------- Transmit Ports - TX PRBS Generator -------------------
TXENPRBSTST0                    =>      tied_to_ground_vec_i(1 downto 0),
TXENPRBSTST1                    =>      tied_to_ground_vec_i(1 downto 0),
-------------------- Transmit Ports - TX Polarity Control ------------------
TXPOLARITY0                     =>      tied_to_ground_i,
TXPOLARITY1                     =>      tied_to_ground_i,
----------------- Transmit Ports - TX Ports for PCI Express ----------------
TXDETECTRX0                     =>      tied_to_ground_i,
TXDETECTRX1                     =>      tied_to_ground_i,
TXELECIDLE0                     =>      tied_to_ground_i,
TXELECIDLE1                     =>      tied_to_ground_i,
--------------------- Transmit Ports - TX Ports for SATA -------------------
TXCOMSTART0                     =>      tied_to_ground_i,
TXCOMSTART1                     =>      tied_to_ground_i,
TXCOMTYPE0                      =>      tied_to_ground_i,
TXCOMTYPE1                      =>      tied_to_ground_i);
```