Radiation Test Report, Single Event Effects, Virtex-5QV Field Programmable Gate Array, Digital Signal Processors

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1. SCOPE

This document describes the execution and results of the investigative effort to characterize and define the Single Event Effect (SEE) symptoms that are experienced by the Digital Signal Processor (DSP) elements embedded in the Virtex-5QV Xilinx Field Programmable Gate Array (FPGA) device.

2. REPORT SUMMARY

Device Tested .....Virtex-5QV FX130T Prototype

SEE Tests.....Static DSP Registers test, and Dynamic test of basic DSP operations, at 25.0, 12.5 and 6.25 MHz.

Radiation Type.....15, 25-MeV/amu Heavy Ions (TAMU)
16-MeV/nuc Heavy Ions (LBNL)

Test Facilities:.....Texas A&M K500 Cyclotron, College Station, TX (TAMU)
Lawrence-Berkeley NL 88" Cyclotron, Berkeley, CA (LBNL)

Test Dates .....July and November 2009, May 2010 and October and December 2011 (TAMU); May and August 2009 (LBNL)

Principal Investigator....Roberto Monreal (Southwest Research Institute)

XRTC Participation .....G. Madias (Boeing), G. Allen (JPL), G. Swift, C. Carmichael, Y.C. Wang, C.W. Tseng, L. Sanders, D. Ellington (Xilinx)

The Single Event Effect (SEE) characterization tests were performed on the DSP48E instances embedded in the Virtex-5QV FPGA. Static register tests were carried out to reveal the SEU cross-sections of the internal registers that make up the embedded DSP, and Dynamic tests were carried out for Multiplication, Addition and Accumulation operations at 25.0, 12.5 and 6.25MHz. No other operating frequencies were used for the dynamic tests. Three types of dynamic upset event signatures were identified, based on the duration; 1) random duration upsets, interpreted as test design configuration upsets; 2) single clock-cycle upsets, representing direct register upsets (SEU) or erroneous captures by the register of Single Event Transients (SET); and 3), repeatable, longer than one clock-cycle, short duration events (< 5µs), which at the time of this write up are believed to be induced by SETs in the clock mechanisms of the DSP test design(1)(2).

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4. ACRONYMS AND DEFINITIONS

ALU	Arithmetic Logic Unit
BiE	Bits in Error; total number of bits in error..
ConfigMon	Configuration Monitor, part of the generic Xilinx test vehicle.
DCM	Digital Clock Manager; FPGA Macro found in Virtex FPGA devices.
DSP	Digital Signal Processor.
FPGA	Field-Programmable Gate Array.
FuncMon	Functional Monitor FPGA, part of the generic Xilinx test vehicle.

FX-1	Viretx-5QV Prototype.
GLUT Mask	Generic Look-Up Table mask
GND	Ground (electrical potential)
GUI	Graphical User Interface.
LBNL	Lawrence-Berkeley National Laboratory.
LET	Linear Energy Transfer; always in units of MeV·mg/cm^2 unless otherwise noted.
LUT	Look-Up Table; logic function implementation in the FPGA configuration block.
MEU	Multiple Element Upset
PCB	Printed Circuit Board.
PROG	Re-program pin of the configuration controller in the Virtex FPGA devices.
PROM	Programmable Read-Only Memory.
SEE	Single-Event Effects.
SEFI	Single Event Functional Interrupt.
SIMD	Same Instruction Multiple Data
SRV	Service FPGA
SW	Software.
SwRI	Southwest Research Institute.
TAMU	Texas A&M University.
XRTC	Xilinx Radiation Test Consortium.

5. BACKGROUND

The DSP48Es of the Virtex-5 FPGA basically consist of a two-input multiplier unit, and a 3-input adder/subtracter unit, in series, as is shown in Figure 5.1. The adder's input operators are selected by the DSP Operational Mode inputs or *OpMode*, and these operators can be a combination of the DSP inputs, the cascaded inputs, the multiplier outputs, the carry-in input (CIN), as well as the DSP's output register value (P-Reg). The OpMode also has the ability to do select bit-shifted values of the cascaded inputs and of the P-Reg output. The OpModes or operations available in the DSP48 are shown in Table 5.1. In addition to the adder/subtracter stage, the DSP48E of the Virtex-5 also adds a secondary stage or logic unit, which can perform bit-wise logic functions to the selected operators by the OpMode. The Arithmetic Logic Unit (ALU) is a feature available in the Viretx-5 architecture DSP48Es which was not available in the Virtex-4 architecture DSP48s.

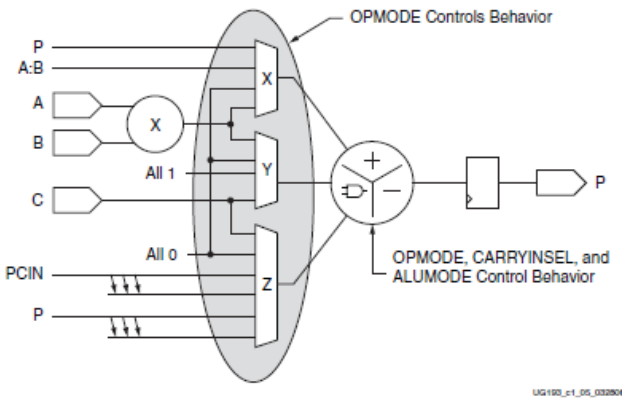


Figure 5.1. DSP48E Basic functions.

Table 5.1. DSP48E Operational Modes.

OP MODE	DSP48 CELL OUTPUT	OP MODE	DSP48 CELL OUTPUT
0x00	± CIN	0x30	C ± CIN
0x02	± (P + CIN)	0x32	C ± (P + CIN)
0x03	± (A:B + CIN)	0x33	C ± (A:B + CIN)
0x05	± (AxB + CIN)	0x35	C ± (AxB + CIN)
0x0C	± (C + CIN)	0x3C	C ± (C + CIN)
0x0E	± (C + P + CIN)	0x3E	C ± (C + P + CIN)
0x0F	± (A:B + C + CIN)	0x3F	C ± (A:B + C + CIN)
0x10	PCIN ± CIN	0x50	PCIN-shift ± CIN
0x12	PCIN ± (P + CIN)	0x52	PCIN-shift ± (P + CIN)
0x13	PCIN ± (A:B + CIN)	0x53	PCIN-shift ± (A:B + CIN)
0x15	PCIN ± (AxB + CIN)	0x55	PCIN-shift ± (AxB + CIN)
0x1C	PCIN ± (C + CIN)	0x5C	PCIN-shift ± (C + CIN)
0x1E	PCIN ± (C + P + CIN)	0x5E	PCIN-shift ± (C + P + CIN)
0x1F	PCIN ± (A:B + C + CIN)	0x5F	PCIN-shift ± (A:B + C + CIN)
0x20	P ± CIN	0x60	PCIN-shift ± CIN
0x22	P ± (P + CIN)	0x62	P-shift ± (P + CIN)
0x23	P ± (A:B + CIN)	0x63	P-shift ± (A:B + CIN)
0x25	P ± (AxB + CIN)	0x65	P-shift ± (AxB + CIN)
0x2C	P ± (C + CIN)	0x6C	P-shift ± (C + CIN)
0x2E	P ± (C + P + CIN)	0x6E	P-shift ± (C + P + CIN)
0x2F	P ± (A:B + C + CIN)	0x6F	P-shift ± (A:B + C + CIN)

There are several sets of registers in the DSP48E that can be implemented by the user for pipe-lining the input operators (A-Reg, B-Reg and C-Reg), the Multiplier output (M-Reg), the output register (P-Reg), and for the control, secondary features, and cascaded signals. These registers allow for the designs that use DSPs to operate in a highly synchronized fashion, enabling operation frequencies up to 550MHz (3). Figure 5.2 illustrates the register locations for the input operators, multiplier and output in the DSP48E Tile. Besides the Arithmetic Logic Unit (ALU) stage in the adder/subtracter, two new interesting features have been added to the Virtex-5 DSP48E architecture. The DSP48s boast a dynamically programmable pattern detect feature, with complete mechanisms for different pattern detect necessities. The Virtex-5 DSP also has the ability to effectively convert each DSP cell into two or four DSP cells, that share the same instruction and control set, but whose input and output operators have been split into 2 or 4 in bit size. The aptly name of this feature is Same Instruction Multiple Data (SIMD) mode.

DSPs in the Virtex-5 series FPGAs are arranged by two cells per DSP site, and there are numerous sites in each dedicated DSP column of the FPGA. Each DSP48E cell has unique operator and control inputs and outputs. Each cell also has unique cascading interfaces to the cells above or below it in the column. Each cell can provide it's A and B-input operators and P-output (ACOUT, BCOUT and PCOUT) to the next DSP cell in the cascade chain, and can receive cascaded operators ACIN, BCIN and PCIN from the

upstream cascaded DSP cell. The multiplier sign, as well as the carry of the operation, can also be forwarded to the next DSP cell in the cascade chain. This is also illustrated in Figure 5.2.

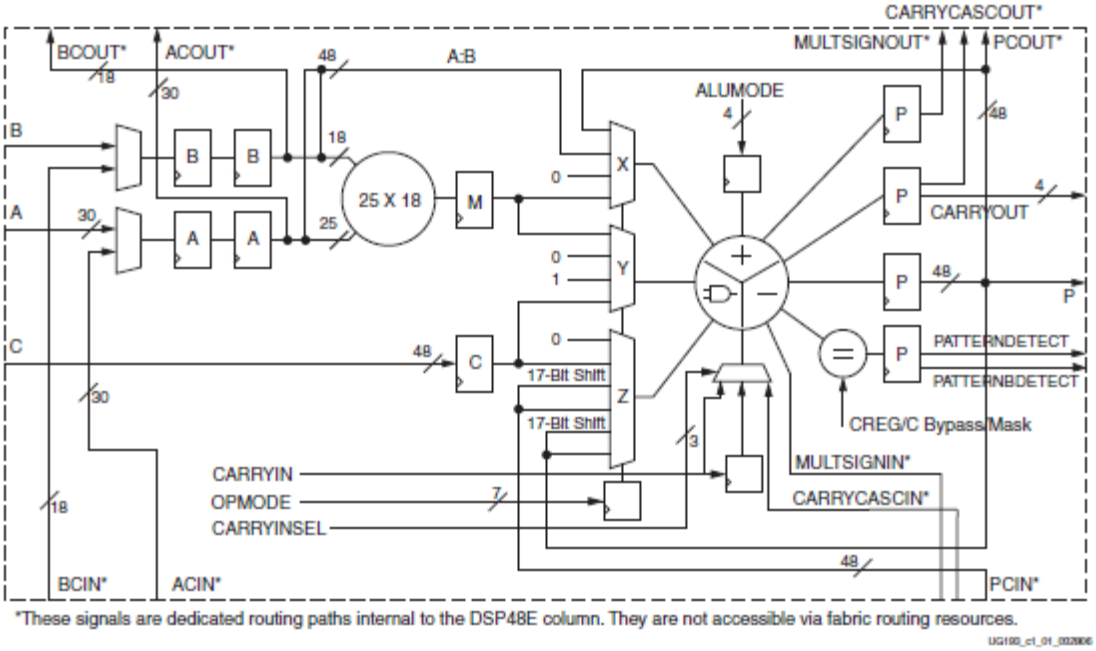


Figure 5.2. DSP48E Block Diagram

6. TEST DESCRIPTION

6.1 Methodology

To test the SEE susceptibility of digital devices like DSPs, which posses combinatorial, storage and control elements; the accepted approach is to segregate the static and dynamic effects. Static effects are errors caused by upsets to the bit-value being stored in any storage element (e.g. user Flip-Flops, configuration cells, etc.), while dynamic effects are upsets that result from inadvertent latching of transitory or Single Event Transients (SET) in the control, clocking and access circuitry of a storage cell. For dynamic tests, how the function is instrumented, the operational duty cycles and the frequency rate are all fundamental variables in determining the upset rate.

6.1.1 Static Testing

The static test approach consisted in filling each of the registers of the DSP48E cell with known values, irradiating them, and counting the number of errors in them. The register set tested includes: the 5 input operator registers, *A1*, *A2*,(30-bit), *B1*, *B2* (18-bit), and *C* (48-bit) registers, the multiplier *M* register (36-bit), and the output *P* register (48-bit). Once each register was loaded with known values, they would be irradiated with the clock disabled. When the irradiation was complete, the values of each register were shifted out of the DSP one at a time and verified. To verify the existence of other elements susceptible to static effects, each available OpMode value was cycled though and the value of each verified. To reduce the effects of configuration upsets, the configuration FPGA design image with the DSP-instantiations was scrubbed continuously at a rate of several times per second. The sequence of the static test is shown in Figure 6.1.

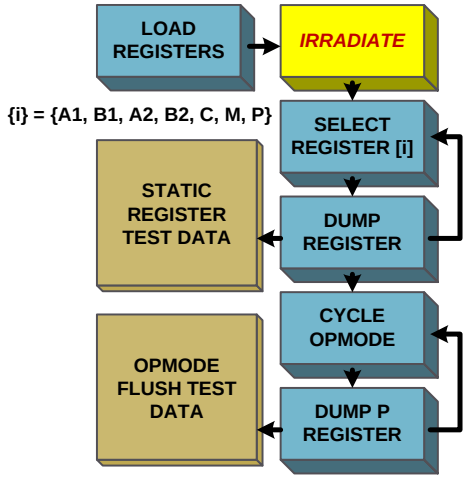


Figure 6.1. Static Register Test Sequence Concept.

6.1.2 Dynamic Testing

Dynamic testing was carried out by simply executing DSP operations with DSP48E cells while irradiating and counting the data errors observed during operation. This dynamic test concept is applied to test structures containing a single DSP48E cell. To limit the number of test iterations the operation spectrum of the DSP was limited into three basic types, listed below. Also, none of the Virtex-5-specific DSP features were tested (Pattern-Detect, and ALU and SIMD modes).

1. Addition, where only the adder/subtracter portion is exercised.
2. Multiplication, where the multiplier is exercised in the operation.
3. Accumulation, where the internal feedback aspect of the DSP is exercised.

The timing diagrams in Figure 6.2 show the OpModes used, operator input states and the expected outputs of the DSP for each test type. In order to maintain variably in the operator outputs, Multiplication and additions tests altered operations or operators every other clock cycle to maintain variability in the operation investigated. The output of Accumulative tests varied continuously.

6.1.2.1 Addition Operations

Addition tests involved operating the DSP without including any feedback or multiplication elements. During the test, the OpMode setting was alternated every clock cycle to select between two different in put parameters to use in the sum. This resulted in two different DSP output values every clock cycle.

6.1.2.2 Multiplication Operations

Multiplication tests were executed by alternating an input operator value between /hex ‘1’ and /hex ‘0’ for every clock cycle. This resulted in a DSP output of zero every other clock cycle.

6.1.2.3 Accumulative Operations

Accumulation operations make use of the feed-back paths internal to the DSP cell. For the test, the DSP was set up to sum the current output value, or the P-register value, to the DSP Carry-in operator value, which in our test was fixed at ‘1’. This resulted in the creation of a counter that is 48-bits wide. When a binary counter is upset, the count must be re-initialized to a known count state to resume predictable operation; in our case, the counter was re-initialized manually back to zero when the DSP output was observed to remain in error indefinitely.

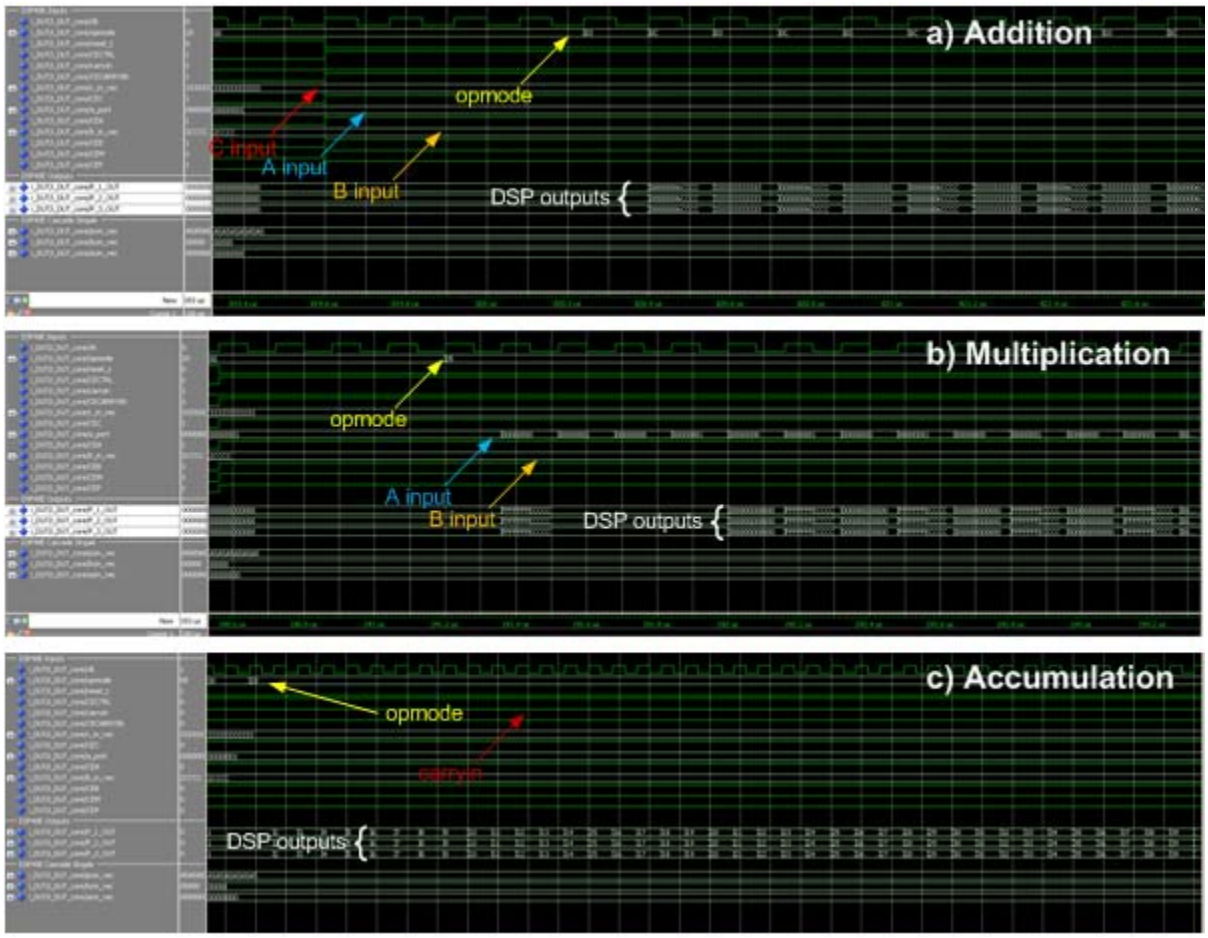


Figure 6.2. Simulation Screenshots of Dynamic DSP test operations; a) Addition, b) Multiplication, and c) Accumulation.

6.2 Instrumentation

The FPGA with the DSP cells under test was assembled on to a PCB, which interfaced to another PCB via high-fidelity connections in a mezzanine-like fashion. The outputs and inputs of the DSPs under test, and the configuration port of the host FPGA, interfaced to a set of FPGAs on the second PCB intended to control and monitor the functionality and the configuration of the FPGA and design tested. All test and DSP control, stimulus and operators were generated through the Functional Monitor (FuncMon) FPGA, which also interfaced to the DUT DSP outputs. The DSP functional verification system and error collection was also performed in the FuncMon FPGA.

6.2.1 Static Register Tests

For static tests, all of the 320 DSP cells available in the DUT FPGA were connected to global operators and controls, and each of the outputs of all the test cells were multiplexed into a single 48-bit vector with a 320-to-1, 48-bit wide structure whose control was controlled by the external FPGA. All control and input operators to the static DSP structures and the output multiplexer were generated by the FuncMon FPGA. The output of the 320-to-1 mux was captured for each of the 320 cells and verified by the FuncMon FPGA for each DSP register type after each irradiation period.

6.2.2 Dynamic Tests

For Dynamic tests, the DSP test clock used was 25.0, 12.5 and 6.25MHz for all operations. Verification FPGA interface provided band-width for 3 DSP cells to be monitored real-time. Each DSP cell's data output was verified for error at the given test frequency used.

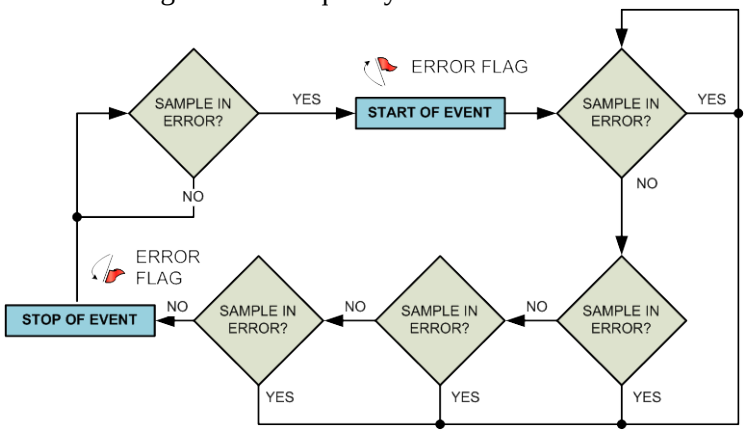


Figure 6.3. DSP Output Error Detection and Validation State Machine.

In the DSP error detection mechanism, upon detection of an erroneous sample, an error flag is activated, latching timers and DSP data and initiating counters. This error flag is maintained until four continuous valid samples are detected by verification engine. This provides a "clutch-like" mechanism in order to only observe full test clock cycle effects. The state machine depicting this mechanism is shown in Figure 6.3.

6.3 Devices Tested

Xilinx Inc. provided several Virtex-5 FX130T "FX-1" prototype devices for these experiments. The devices had previously undergone processing to reduce the thickness of the substrate. Since the Xilinx Virtex series of FPGAs use flip-chip architecture, the accelerator's energetic ions must travel the thickness of the back-substrate to reach the sensitive integrated circuits. The thickness of the substrate was reduced by JPL to allow particles with lower energy to make it through to the sensitive area. Three devices were utilized for the entire testing; they are listed in Table 6.1. The devices were mounted on two different daughter card designs. Figure 6.4 shows a photograph of the DUT device utilized.

Table 6.1. DUT Devices utilized in the tests.

FX-1 SN	Substrate Thickness	PCB Serial No	Test
n/a	82.3µm^	FX130T-002	TAMU APR09, LBNL MAY09
A4438	200µm	0928-010 Rev. B	TAMU JUL09, LBNL AUG09, TAMU NOV09
A4464	85µm	0928-009Rev. B	TAMU AUG10, TAMU NOV10

^Determined experimentally

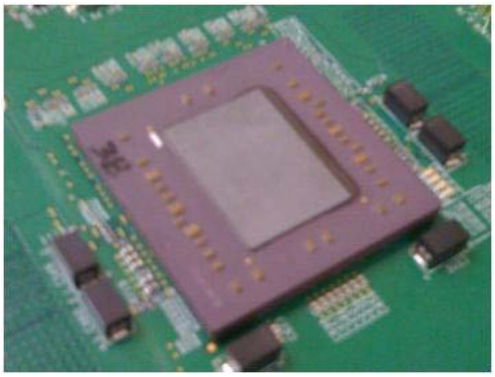
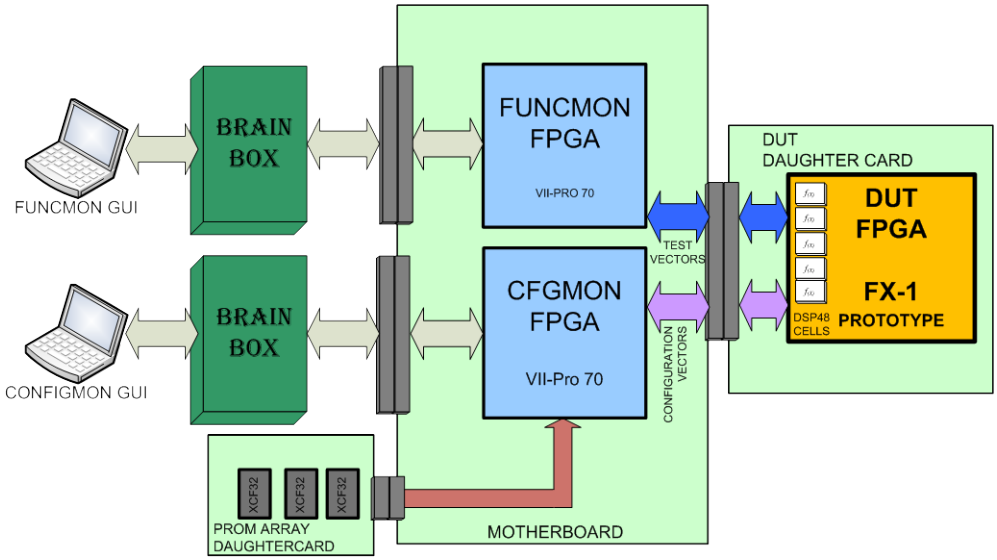


Figure 6.4. Photograph of the FX-130T FX-1 Prototype FPGA used in the tests.

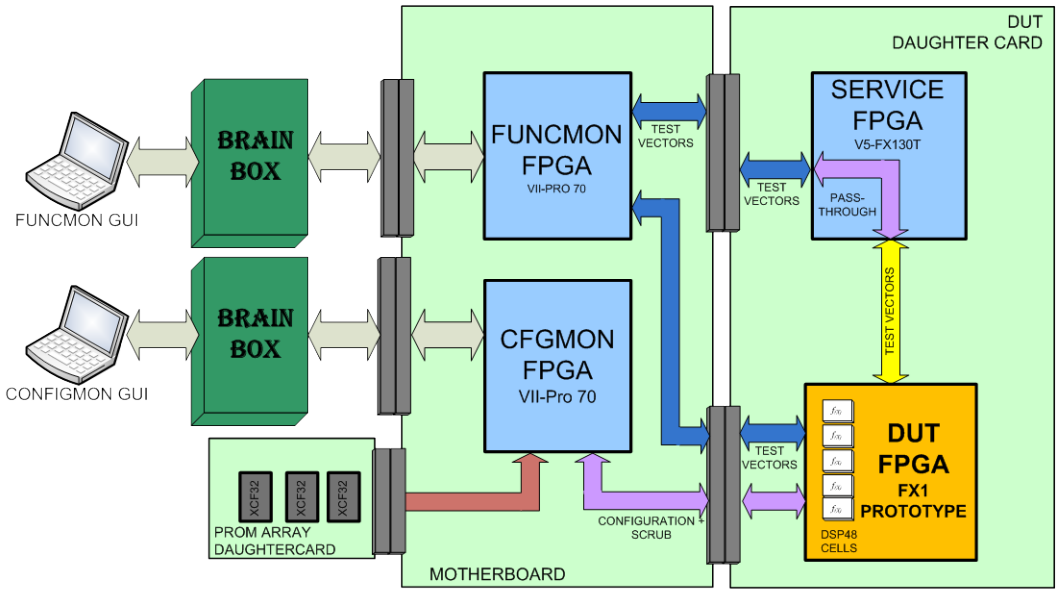
6.4 Test Setup

6.4.1 Test System Hardware

The test system devised for these experiments was based on the XRTCs test platform, which has been employed by Xilinx Inc. and their customers for several generations of Xilinx FPGAs.



(a)



(b)

Figure 6.5. Test System top-level diagrams, for the simple DUT daughter card configuration (a), and for a Service-DUT FPGA daughter card configuration. (b).

6.4.1.1 XRTC Motherboard

The principal building-block of the XRTC test platform is the XRTC Motherboard, which has been upgraded through the years to the current design, in use since 2005. The XRTC motherboard hosts a Functional Monitor FPGA (FuncMon), a Configuration Monitor FPGA (ConfigMon), and a multitude of interfaces. The primary interfaces are: to a DUT daughter-card, to host-computers for control and data logging of the FuncMon and ConfigMon FPGAs, to a PROM array daughter-card, and to power supplies. The XRTC ConfigMon and FuncMon external interfaces employ hardware modules commonly known as "Brain Boxes", which format the data being read into log files to be stored in a corresponding laptop; each Brain Box also provides user interface commands to the ConfigMon and FuncMon FPGAs from the host laptops. The PROM array daughter card hosts 12 Xilinx XCF32 Flash-PROM devices that allow the ConfigMon FPGA to access a collection of DUT FPGA designs to be uploaded to the DUT very efficiently while testing. The diagrams shown in Figure 6.5 display the system, showing two types of daughter card configurations. For these experiments, two system configurations were developed, the system in Figure 6.5 (a), with a simple daughter card containing one DUT FPGA; and the one shown in Figure 6.5 (b), with a DUT and Service FPGAs. In this latter case, the Service FPGA was programmed as a pipe-lined pass-through device for the DSP data. The simple daughter card implementation was only undertaken for one testing session.

As each of the motherboard's FPGA names imply, the FuncMon and ConfigMon FPGAs are used to monitor the particular functionality being tested in the DUT FPGA, and used to monitor the configuration of the DUT FPGA. Thus for each different experiment, a new FuncMon design is generated, while the ConfigMon FPGA design is shared from experiment to experiment within the XRTC. The ConfigMon code is maintained and kept by Xilinx Inc. To carry out the testing, hardware designs were generated for a FuncMon FPGA and a DUT FPGA.

6.4.1.2 FPGAs

6.4.1.2.1 FPGA Clocking and DSP Clock rates

The clocking for the FPGAs was generated by two oscillators on the XRTC Motherboard, of 100MHz and 33MHz. The oscillators interface to the ConfigMon FPGA directly, which then forward both of the clock signals to the FuncMon FPGA. This is the typical XRTC experimental setup. For the DSP experiments, the FuncMon FPGA design only utilized the 100MHz clock, and with a DCM divided down to the test frequency (25.0, 12.5 or 6.25MHz), and 6.25MHz, using the first as the DSP test frequency, and the latter as the interface frequency to the Brain-Box hardware system. The FuncMon data verification system utilized the 100MHz clock to measure the SEE duration on the output test data from the DSPs under test. The diagram in Figure 6.6 illustrates the clocking concept.

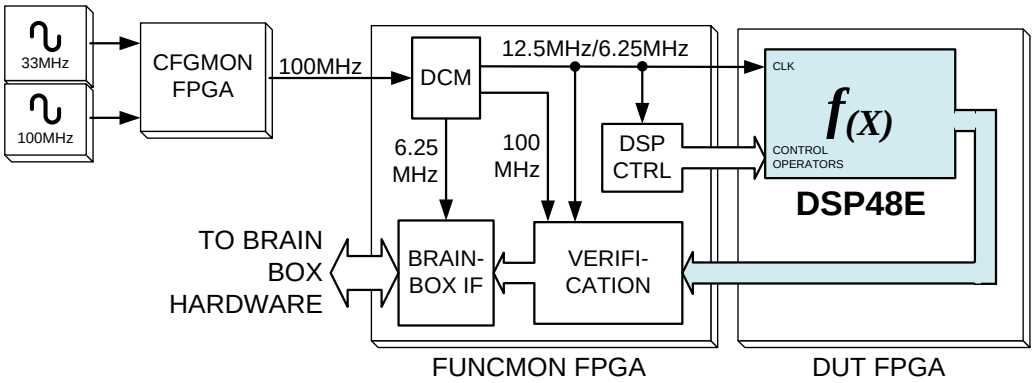


Figure 6.6. Diagram showing the clock frequencies and distribution in the dynamic test system.

6.4.1.2.2 DUT FPGA Design

Two DUT FPGA designs were developed, in order to instantiate the test structures. One design was generated for the Static Register test design, and the other for the Dynamic Operator design.

6.4.1.2.2.1 Static DSP Register Test Design

The Static Register Test Design FPGA is illustrated in Figure 6.7. The user-controlled DSP controls and the fixed operators and their values are shown in Figure 6.7. The DUT FPGA was instantiated to force all the fixed operators to "hard" ones and zeros by tying off the signals to $V_{CC\text{-}CORE}$ and Ground posts. The configuration of the DSP cells for the static register test is shown in detail in Appendix E.

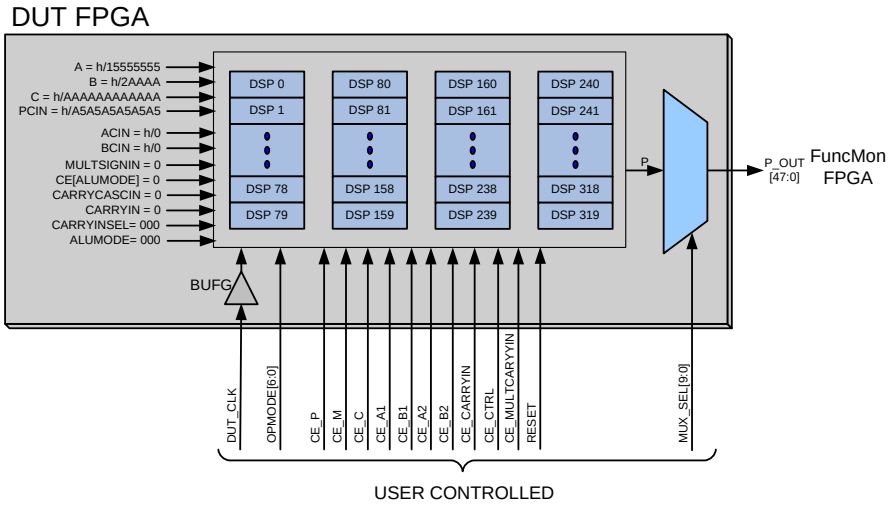


Figure 6.7. Static Register Test FPGA Design Block Diagram.

6.4.1.2.2.2 Dynamic Test Design

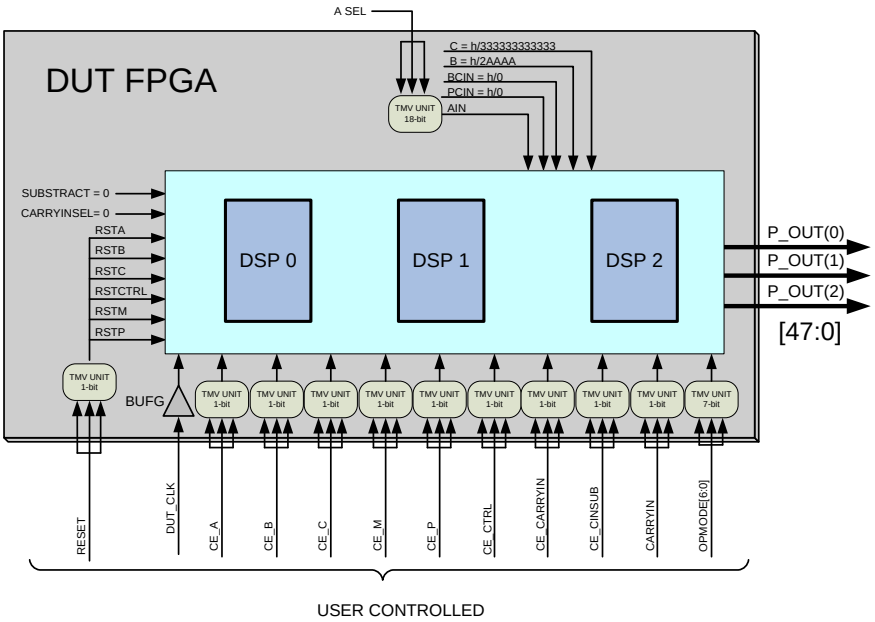


Figure 6.8. Dynamic Operations Test FPGA Design Block Diagram.

The dynamic design connected the 48-bit outputs of three distinct DSP cells, which were ported out directly out of the FPGA. Each of these DSPs output ports were monitored real time for error. These are noted (0), (1) and (2) in Figure 6.8. The various DSP48E cell locations for each of the DUT FPGA design iterations are listed in Table 6.2 below.

Table 6.2. DSP48E cell locations used for dynamic tests.

DSP Dynamic Iteration	DSP (0)	DSP (1)	DSP (2)
May, July 2009 Test (I)	DSP48 X1Y71	DSP48 X0Y28	DSP48 X1Y15
November 2009 Tests (II)	DSP48 X3Y35	DSP48 X3Y39	DSP48 X3Y25
November 2009 Tests (III)	DSP48 X3Y38	DSP48 X2Y34	DSP48 X3Y27

I. Implemented in simple daughter card configuration with pipeline registers only
II. Implemented in MGT daughter card configuration with DSP pipeline registers only
III. Implemented in MGT daughter card configuration with DSP pipeline and control registers

All control inputs to the DUT, except for the test clock, were driven into the FPGA with triplicated inputs. The triple-input signal was then voted with logic before accessing the DSP cell array. The triplicated DSP array multiplexer was voted and ported through a single set of outputs, and DSP output busses used for real-time monitoring were not triplicated at all.

6.4.1.2.3 Functional Monitor (FuncMon) FPGA Design

The a design was need for the FuncMon FPGA in order to collect and assemble the DSP data from the DUT, and to provide a user interface to the DUT. Test user signals, and test output data were driven to and from the Brain-Box hardware that attached to the FuncMon FPGA. Figure 6.9 shows the block diagram of the FuncMon design template shared across XRTC experiments. Each specific experiment customizes the core to fit the specific functions required.

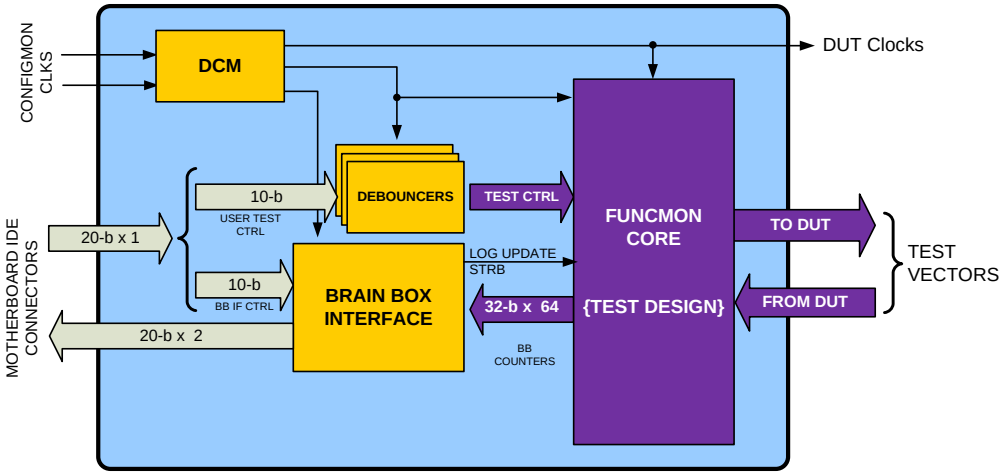


Figure 6.9. XRTC FuncMon FPGA Design Template.

6.4.1.2.3.1 Static Test Design

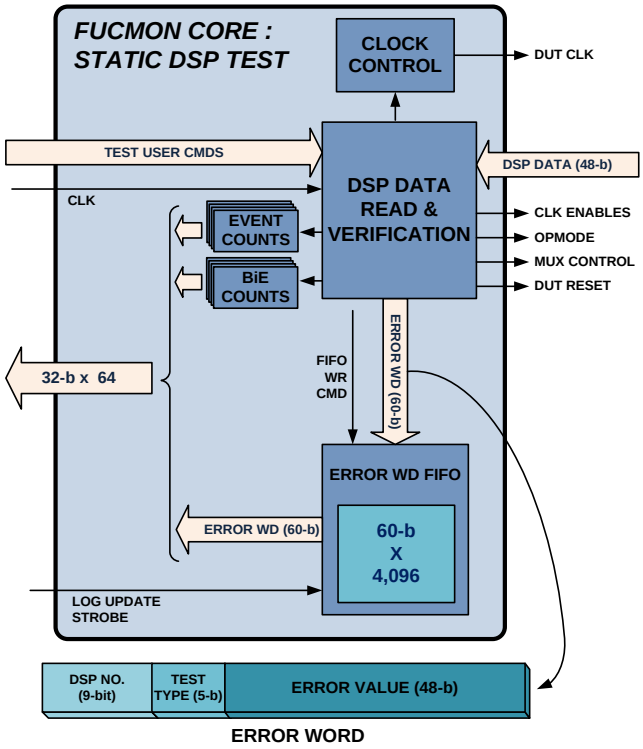


Figure 6.10. Design block diagram of the FuncMon Test Core for the DSP Static Tests.

The FuncMon FPGA core design developed for this test is shown in Figure 6.10. The main element of the design pivots around the *DSP Data Read & Verification* block, which fills the DUT DSP registers with known values, and extracts the contents of each once irradiated. For each read and verify operation, the state machine cycles through all of the 512 DSP cells by selecting each through the multiplexer in the DUT. Error counters tracked the number of cells with errors and the number of bits in error (BiE) for each register type, and for each OpMode selection. For each error detected, an Error Word was assembled and forwarded to the test log via a FIFO interface. The make-up of the Error Word is shown in Figure 6.10. The governing state-machine of the Read & Verification block was shown in Figure 6.1. The Read & Verification block state machine controlled the clock signal, clock enables, OpModes and reset to the DUT and the DSPs instantiated.

6.4.1.2.3.2 Dynamic Test Design

The FuncMon dynamic test design received 3, 48-bit words in parallel from the DUT FPGA, which are direct outputs from the selected DSPs and test structures for real-time monitoring. Each of the 48-bit input vectors was continuously compared against a “golden” DSP output value; generated and synchronized to the test data inputs by the DSP Test Control block. DSP outputs were considered in error when they differed from the expected value.

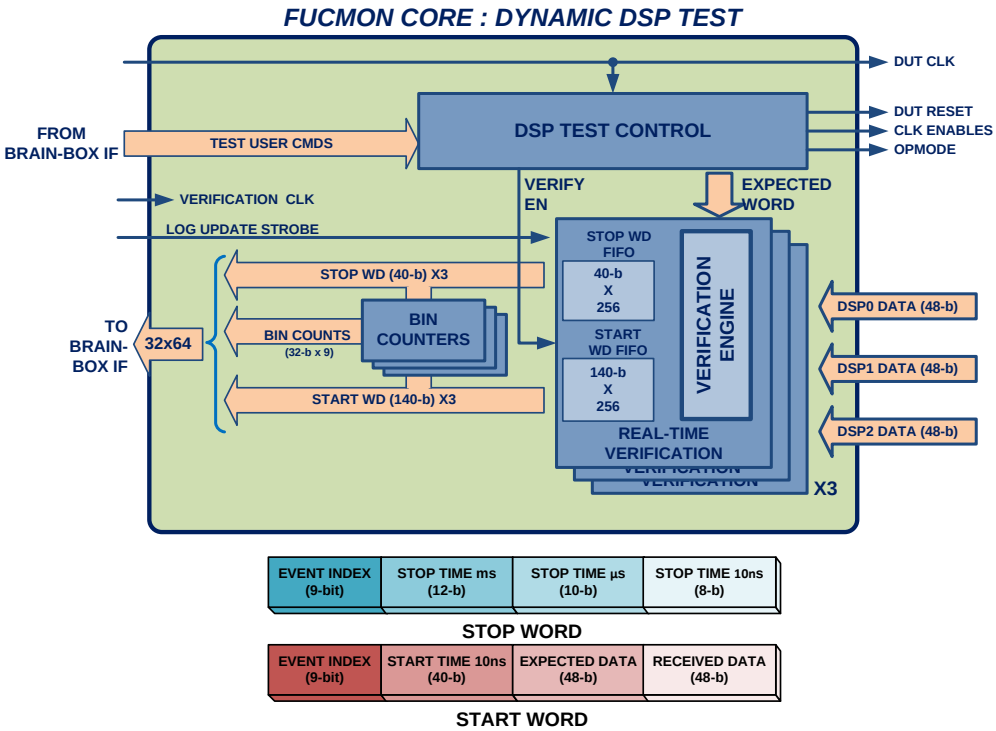


Figure 6.11. Design block diagram of the FuncMon Test Core for the DSP Dynamic Tests.

Upon error detection, the Real-Time verification block captured the expected and received data values, as well as the time when the error was detected. These values are then stored in a local FIFO. When the data is considered valid again, the time of duration of the error is captured and stored in a corresponding FIFO. The Start and Stop data words are shown in Figure 6.11. A global FIFO would then arbitrate each intermediate Start and Stop FIFO and move the contents from them onto it. The Brain-box logging system would then fetch the global FIFOs data and log the information. Bin counters were setup to sample the data being read form the FIFO in order to perform real-time analysis during the test.

6.4.2 Test GUIs

6.4.2.1 FuncMon User Interface

6.4.2.1.1 Static Test Design

The Static Test employed the GUI shown in Figure 6.12. The Test User was provided with the ability to Load, Train (exercise one level of the register dump), and extract the resisters (Register Test). Commands for initiating the Flush tests (cycle through OpModes); as well as Resetting the FuncMon and DUT DSPs were also available to the user. After each test the number of bit errors and register errors was displayed for each register and flush cycle. The stack with the error data was displayed and logged one every 10msecs by the Brain-Box HW.

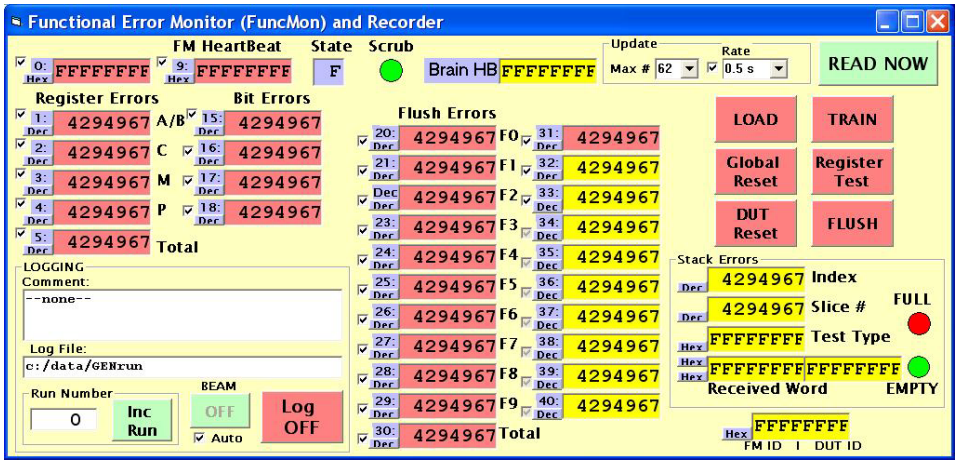


Figure 6.12. DSP Static Register Test FuncMon GUI.

6.4.2.1.2 Dynamic Test Design

The Dynamic Test employed the GUI shown in Figure 6.13. The Test User had the ability, thought this GUI, the select the operations via a pull-down menu, Enable and Re-Initialize the dynamic tests, and reset the FuncMon and DUT DSPs. Indicators showing the status of the 3 real-time monitored DSPs for in-situ assessment.

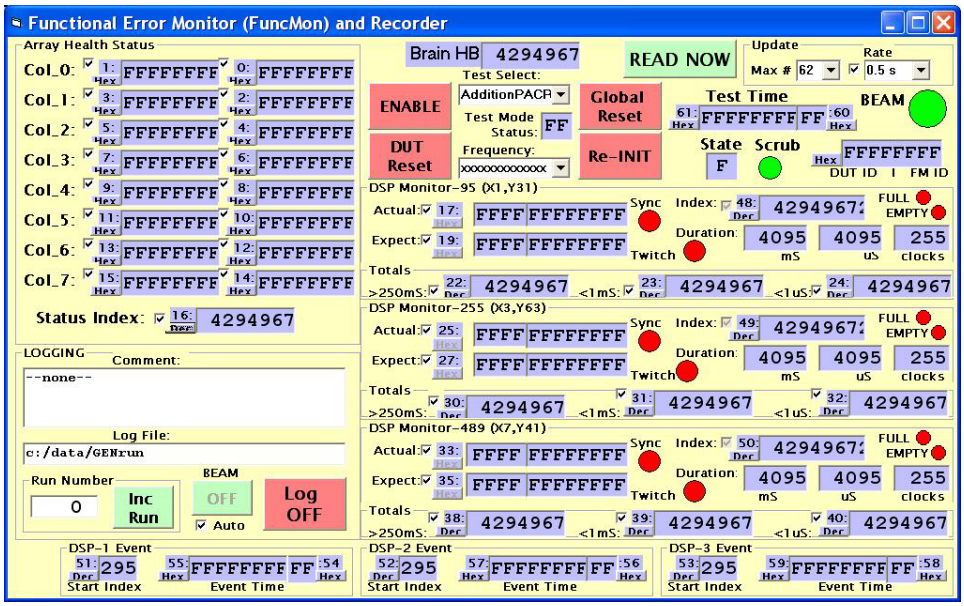


Figure 6.13. DSP Dynamic Operations Test FuncMon GUI.

6.4.2.2 ConfigMon User Interface

The Configuration Monitor GUI is shown in Figure 6.14, and is the same one exercised by all the XRTC experiments. In summary, through this GUI, the test user was able to select different configuration monitoring modes, such as read-back only, scrub only, or read-back/scrub alterations, the user can instantiate a GLUT mask in the DUT FPGA Configuration engine, which masks LUT RAM bits and SRL16 bits from the read-back. Also, through the ConfigMon GUI, the user can select different DUT and FuncMon configuration files, different DUT design mask files, and implement non-essential bit-stream

bit masks on top of those. A detailed description of the Configuration Monitor functionality is beyond the scope of this document

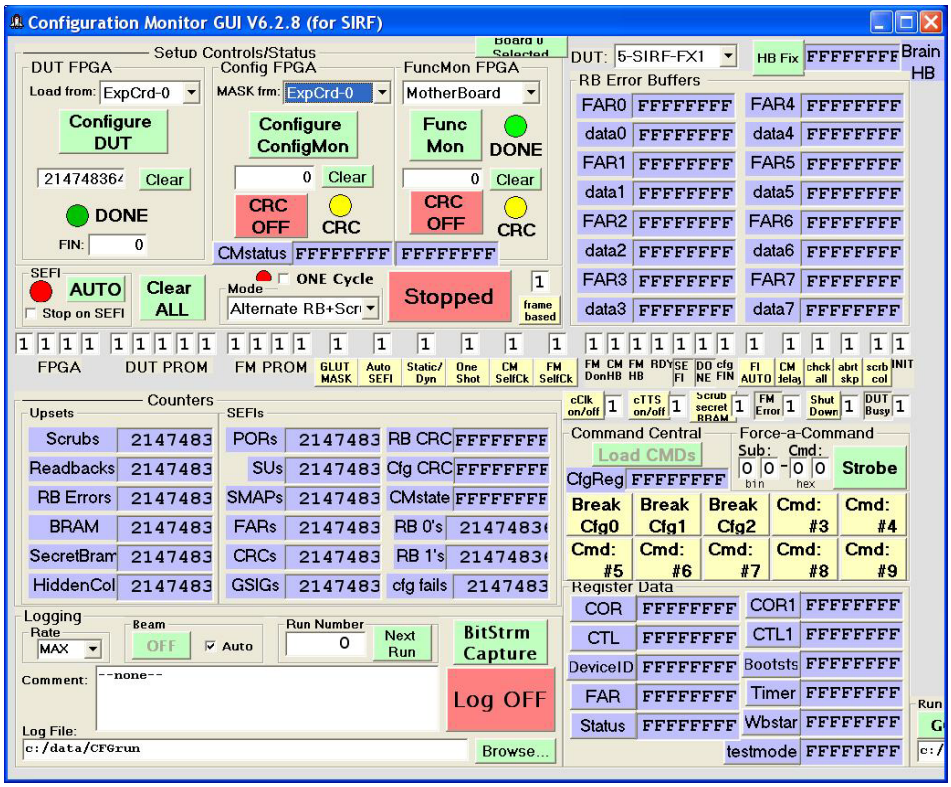


Figure 6.14. Configuration Monitor Brain-box GUI.

6.4.3 DUT Configuration

The DUT FPGA design was being verified for configuration integrity during the irradiation runs. A full-design configuration read-back cycle was performed and followed by a full-design scrub cycle. The read-back and scrub cycles were driven by the ConfigMon FPGA. Each scrub cycle was broken up into individual frames, where the ConfigMon would verify the status of the DUT FPGA's configuration engine before proceeding to scrub the next frame of the design. If the DUT FPGA configuration engine status was unexpected, or failed to respond, the ConfigMon would initiate a reconfiguration process of the DUT FPGA. These configuration engine events are referred to as SEFIs, and have received much attention by the industry(4). The ConfigMon functionality also allows for particular masking of the bit-stream being read-back; for instance, the state of the LUT register bit values, the state of the DRP configuration bits can all be read-back and scrubbed. During the testing, a mask was implemented that masked these bits from being scrutinized in the read-back.

6.5 Test Procedure

6.5.1 Static Register Tests

The static register test procedure flow-chart is shown in Figure 6.15. Static Register Test Procedure Flow-chart.Figure 6.15. After the loading of the DSP registers, the DUT DSP clock was disabled for the irradiation period. Configuration scrubbing mechanisms were being driven by the ConfigMon FPGA and thus were referenced to a different clock system. Irradiation periods were based on an amount of total fluence, typically around 1E+04 to 1E+05 particles per cm^2, depending on the particle's deposited Linear

Energy Transfer. After the irradiation period was complete, the DSP register contents were dumped and compared and cataloged. After the DSP registers were dumped, the DSP outputs were captured for each of a series of OpModes on the existing register contents. Since the OpMode flush function was exercised with the same register contents, which were corrupt by the irradiation, a live comparison upon DSP output collection was not possible and had to be extracted during analysis.

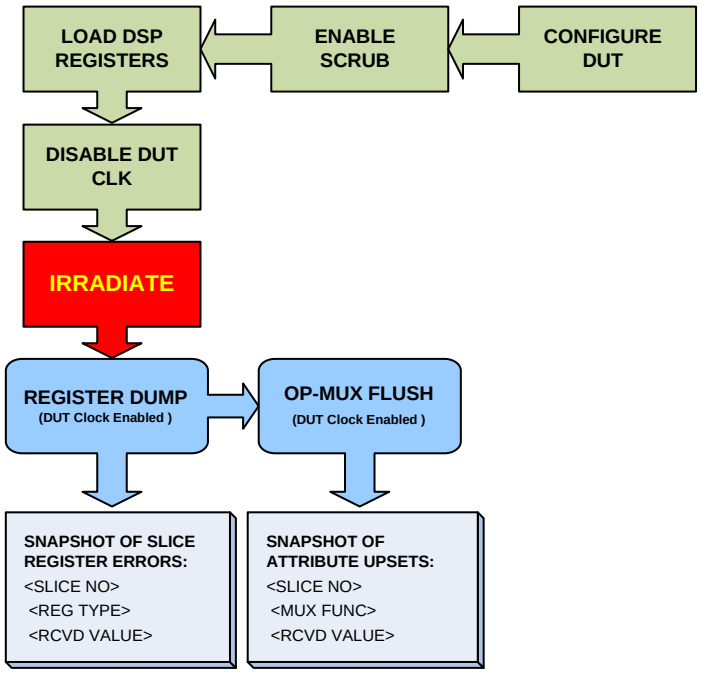


Figure 6.15. Static Register Test Procedure Flow-chart.

6.5.2 Dynamic Operation Tests

The dynamic test procedure went as follows; first, the DUT would be configured with the DSP test, then the configuration manager was setup to read back the configuration image and scrub on error; finally, the data generation and verification would be enabled. If the device was detected to be experiencing a SEFI manifestation on the configuration engine, the ConfigMon would command a device reprogram. Once the test was running, the device was irradiated. The dynamic test procedure's flow-chart is shown in Figure 6.16.

Upon enabling of the test, the verification mechanisms would capture, upon error detection, the start time and the expected and received data words of the event. Once the error would cease, the amount of error duration was cataloged. If the DSP being monitored was observed to not recover, manual stimulus like an operation re-initialization, DSP reset and device reconfiguration would be attempted.

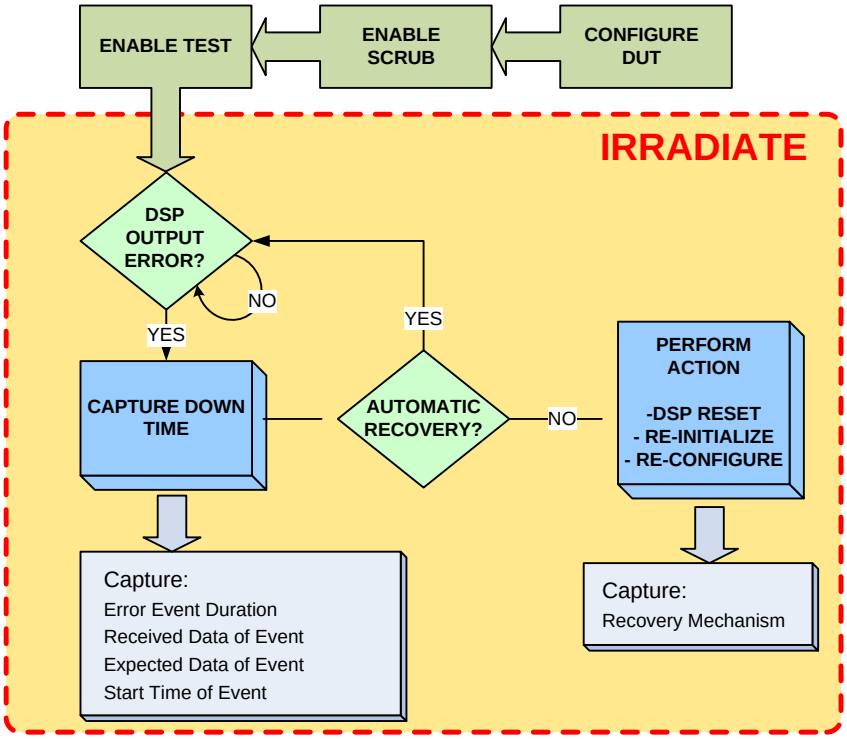


Figure 6.16. Dynamic Operations Test Procedure Flow-chart.

7. TEST RESULTS

7.1 Static Tests

Static tests provided static SEU cross-sections for the internal operator-path registers of the DSP48E that are fundamental for high performance operations. The testing campaigns that provided the data took place in April 2009, and in October and December of 2011 at the Texas A&M Cyclotron, and in May 2009 at the LBNL cyclotron. The concise listing of all the experimental runs that resulted in valid data is shown in Table 7.1. Shown in Table 7.2 are the results from data captured for each DSP slice from which the number of bits in error (BiE) per static register event was extracted. The BiE counts were analyzed post-factum from the logged register dumps. Several data sets appeared to have been corrupted by functional bugs in the data capture system. Omitted is the OpMode Flush test data that was captured. In this case, a functional issue with the FuncMon GUI flush-test controls resulted in the loss of this data in many of the test runs. The captured flush-test data is not analyzed at this time.

Table 7.1. Accelerator Run Log for the DSP48E Static Registers Test.

RUN	FACILITY	LET (MeV/cm²·mg)	RUN TIME (S)	FLUENCE (p/cm²)	FLUX (p·s/cm²)	P REG	C REG	M REG	1A REG	1B REG	2A REG	2B REG	CELLS AFFECTED (%)	NOTE
44	LBNL MAY09	25.10	50.4	5.030E+06	2.00E+05	145	141	143	134	124	142	131	42.9	
45	LBNL MAY09	25.10	12.0	1.040E+06	4.14E+04	132	118	139	101	76	101	69	32.9	
46	LBNL MAY09	25.10	10.6	1.030E+06	4.10E+04	115	90	127	93	57	97	57	28.4	
47	LBNL MAY09	25.10	11.7	1.030E+06	4.10E+04	117	98	131	89	60	85	64	28.8	
48	LBNL MAY09	16.50	32.0	1.010E+06	6.12E+04	89	88	109	-	-	-	-	29.8	1
49	LBNL MAY09	16.50	31.7	1.010E+06	6.12E+04	86	82	115	72	40	77	42	22.9	
50	LBNL MAY09	16.50	31.3	1.010E+06	6.12E+04	96	75	102	64	44	57	47	21.7	
51	LBNL MAY09	16.50	31.0	1.010E+06	6.12E+04	88	80	108	61	44	59	47	21.7	
52	LBNL MAY09	16.50	29.9	1.010E+06	6.12E+04	95	82	109	70	51	62	34	22.5	
53	LBNL MAY09	7.27	29.4	1.010E+06	1.39E+05	33	36	59	29	22	24	19	9.9	
54	LBNL MAY09	7.27	795.3	5.020E+05	6.91E+04	21	19	38	-	-	-	-	8.1	1
55	LBNL MAY09	2.39	65.0	1.000E+06	4.18E+05	15	12	20	-	-	-	-	4.9	1
56	LBNL MAY09	2.39	69.2	1.000E+06	4.18E+05	11	14	24	-	-	-	-	5.1	1
57	LBNL MAY09	2.39	72.4	1.000E+06	4.18E+05	19	10	15	-	-	-	-	4.6	1
58	LBNL MAY09	1.16	230.0	5.010E+06	4.32E+06	6	25	46	-	-	-	-	8.0	1
59	LBNL MAY09	1.16	229.4	5.010E+06	4.32E+06	9	22	44	-	-	-	-	7.8	1
60	LBNL MAY09	1.16	229.0	5.010E+06	4.32E+06	6	27	34	-	-	-	-	7.0	1
1404	TAMU APR09	4.00	172.9	1.001E+06	5.79E+03	56	-	57	23	19	27	17	10.4	2
1405	TAMU APR09	3.90	177.4	9.993E+05	5.63E+03	59	-	60	24	13	23	14	10.1	2
1406	TAMU APR09	3.90	187.4	1.003E+06	3.53E+03	58	-	64	21	15	28	14	10.4	2
1427	TAMU APR09	15.70	459.1	1.000E+06	2.18E+03	112	-	153	72	49	61	49	25.8	2
1431	TAMU APR09	12.00	420.6	1.001E+06	2.38E+03	86	-	129	64	40	62	34	21.6	2
49	TAMU OCT11	1.80	10.0	5.196E+06	5.21E+05	-	110	104	-	-	-	-	33.4	1,3
53	TAMU OCT11	1.80	24.4	4.900E+05	2.01E+04	-	14	26	7	10	7	8	3.8	3
55	TAMU OCT11	1.80	27.4	4.500E+06	1.83E+04	-	12	17	4	8	14	16	3.7	3
56	TAMU OCT11	1.80	24.9	5.060E+05	2.06E+04	-	11	21	12	17	7	9	4.0	3
61	TAMU OCT11	1.80	2.2	4.580E+04	2.07E+04	-	1	1	0	0	1	0	0.2	3
63	TAMU OCT11	1.80	9.8	9.170E+05	5.10E+03	-	2	7	3	2	3	1	0.9	3
85	TAMU DEC11	27.00	2.8	7.230E+04	2.58E+04	37	30	49	26	16	25	17	8.9	
86	TAMU DEC11	27.00	2.9	6.970E+04	2.40E+04	38	25	55	24	15	29	12	8.8	
87	TAMU DEC11	27.00	1.8	3.990E+04	2.26E+04	31	25	37	21	14	14	5	6.6	
88	TAMU DEC11	27.00	8.5	1.250E+05	1.47E+04	35	59	85	32	22	29	31	13.1	
89	TAMU DEC11	27.00	2.0	3.000E+04	1.47E+04	14	14	24	11	5	8	8	3.8	
90	TAMU DEC11	27.00	2.7	5.260E+04	1.95E+04	22	21	32	16	5	14	15	5.6	
92	TAMU DEC11	1.90	3.6	5.820E+05	1.66E+05	17	12	22	7	4	8	7	3.4	
94	TAMU DEC11	1.90	4.6	7.730E+05	1.70E+05	14	24	35	10	7	17	13	5.4	
96	TAMU DEC11	1.90	9.0	1.600E+06	1.80E+05	18	31	43	19	6	7	7	5.8	
97	TAMU DEC11	1.90	10.5	1.880E+06	1.80E+05	34	40	52	20	23	31	21	9.9	
98	TAMU DEC11	1.90	12.0	2.360E+06	1.98E+05	43	50	78	37	19	30	18	12.3	

Table 7.2. Accelerator Run Log for the DSP48E Static Register Bits Test

RUN	FACILITY	LET (MeV/cm ^{2}·mg)	RUN TIME (S)	FLUENCE (p/cm^2)	FLUX (p·s/cm^2)	P REG BITS	C REG BITS	M REG BITS	1A REG BITS	1B REG BITS	2A REG BITS	2B REG BITS	CELLS AFFECTED (%)	NOTE
44	LBNL MAY09	25.10	50.4	5.030E+06	2.00E+05	1012	764	1947	404	314	430	316	42.9	
45	LBNL MAY09	25.10	12.0	1.040E+06	4.14E+04	336	254	808	150	102	148	94	32.9	
46	LBNL MAY09	25.10	10.6	1.030E+06	4.10E+04	238	147	624	126	71	134	73	28.4	
47	LBNL MAY09	25.10	11.7	1.030E+06	4.10E+04	250	188	644	132	82	124	81	28.8	
48	LBNL MAY09	16.50	32.0	1.010E+06	6.12E+04	-	-	-	-	-	-	-	29.8	1
49	LBNL MAY09	16.50	31.7	1.010E+06	6.12E+04	129	122	422	90	50	93	49	22.9	
50	LBNL MAY09	16.50	31.3	1.010E+06	6.12E+04	154	116	358	82	52	65	53	21.7	
51	LBNL MAY09	16.50	31.0	1.010E+06	6.12E+04	173	118	420	71	51	70	55	21.7	
52	LBNL MAY09	16.50	29.9	1.010E+06	6.12E+04	128	116	361	91	60	76	44	22.5	
53	LBNL MAY09	7.27	29.4	1.010E+06	1.39E+05	-	39	152	32	23	30	21	9.9	
54	LBNL MAY09	7.27	795.3	5.020E+05	6.91E+04	-	-	-	-	-	-	-	8.1	1
55	LBNL MAY09	2.39	65.0	1.000E+06	4.18E+05	-	-	-	-	-	-	-	4.9	1
56	LBNL MAY09	2.39	69.2	1.000E+06	4.18E+05	-	-	-	-	-	-	-	5.1	1
57	LBNL MAY09	2.39	72.4	1.000E+06	4.18E+05	-	-	-	-	-	-	-	4.6	1
58	LBNL MAY09	1.16	230.0	5.010E+06	4.32E+06	-	-	-	-	-	-	-	8.0	1
59	LBNL MAY09	1.16	229.4	5.010E+06	4.32E+06	-	-	-	-	-	-	-	7.8	1
60	LBNL MAY09	1.16	229.0	5.010E+06	4.32E+06	-	-	-	-	-	-	-	7.0	1
1404	TAMU APR09	4.00	172.9	1.001E+06	5.79E+03	65	-	133	25	19	28	19	10.4	2
1405	TAMU APR09	3.90	177.4	9.993E+05	5.63E+03	69	-	132	25	13	24	14	10.1	2
1406	TAMU APR09	3.90	187.4	1.003E+06	3.53E+03	61	-	155	22	16	30	15	10.4	2
1427	TAMU APR09	15.70	459.1	1.000E+06	2.18E+03	145	-	357	76	54	58	51	25.8	2
1431	TAMU APR09	12.00	420.6	1.001E+06	2.38E+03	101	-	340	71	40	68	35	21.6	2
49	TAMU OCT11	1.80	10.0	5.196E+06	5.21E+05	-	134	244	-	-	-	-	33.4	1, 3
53	TAMU OCT11	1.80	24.4	4.900E+05	2.01E+04	-	14	46	7	16	7	10	3.8	3
55	TAMU OCT11	1.80	27.4	4.500E+06	1.83E+04	-	12	27	4	12	14	19	3.7	3
56	TAMU OCT11	1.80	24.9	5.060E+05	2.06E+04	-	11	50	12	26	7	12	4.0	3
61	TAMU OCT11	1.80	2.2	4.580E+04	2.07E+04	-	1	2	0	0	1	0	0.2	3
63	TAMU OCT11	1.80	9.8	9.170E+05	5.10E+03	-	2	13	3	2	4	1	0.9	3
85	TAMU DEC11	27.00	2.8	7.230E+04	2.58E+04	38	32	100	26	16	26	17	8.9	
86	TAMU DEC11	27.00	2.9	6.970E+04	2.40E+04	50	26	103	26	16	29	12	8.8	
87	TAMU DEC11	27.00	1.8	3.990E+04	2.26E+04	33	26	77	22	15	14	5	6.6	
88	TAMU DEC11	27.00	8.5	1.250E+05	1.47E+04	38	61	200	33	22	30	31	13.1	
89	TAMU DEC11	27.00	2.0	3.000E+04	1.47E+04	37	14	41	12	5	8	9	3.8	
90	TAMU DEC11	27.00	2.7	5.260E+04	1.95E+04	23	21	72	16	5	14	15	5.6	
92	TAMU DEC11	1.90	3.6	5.820E+05	1.66E+05	17	12	40	7	4	8	7	3.4	
94	TAMU DEC11	1.90	4.6	7.730E+05	1.70E+05	14	26	71	10	7	17	13	5.4	
96	TAMU DEC11	1.90	9.0	1.600E+06	1.80E+05	18	33	94	20	6	7	7	5.8	
97	TAMU DEC11	1.90	10.5	1.880E+06	1.80E+05	36	43	108	21	23	31	21	9.9	
98	TAMU DEC11	1.90	12.0	2.360E+06	1.98E+05	47	52	161	37	20	32	19	12.3	

(1) Register Bit data corrupt, AB Register separation corrupt.
(2) C Register Error data not recorded due to HW bug.
(3) P Register Bit data corrupt.

7.1.1 P Output Register

A static upset cross-section was captured; a plot vs. LET and a Weibull fit it is shown in Figure 7.1, and the bit cross-section is shown in Figure 7.2. Triangular data points were obtained at the Texas A&M cyclotron, while the circular points are from the Berkeley cyclotron.

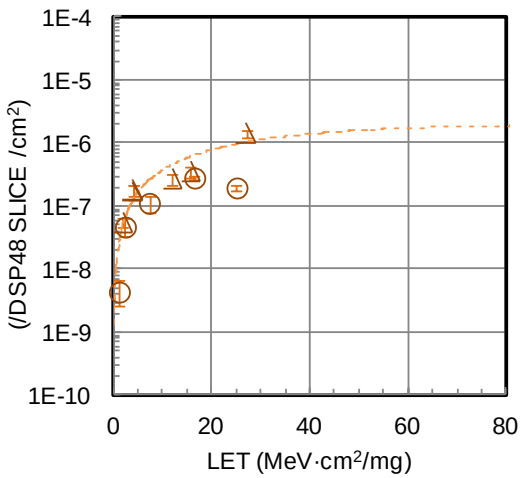


Figure 7.1. P Output Register Static Cross-Section vs. LET.

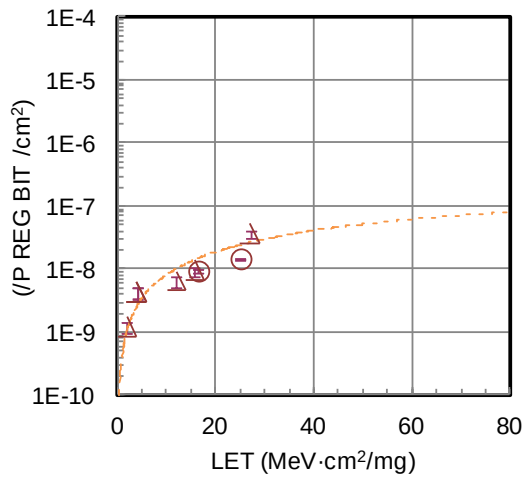


Figure 7.2. P Output Register Bit Static Cross-Section vs. LET.

7.1.2 M Multiplier Register

A static upset cross-section was captured; a plot vs. LET and a Weibull fit is shown in Figure 7.3, and the bit cross-section is shown in Figure 7.4. Triangular data points were obtained at the Texas A&M cyclotron, while the circular points are from the Berkeley cyclotron.

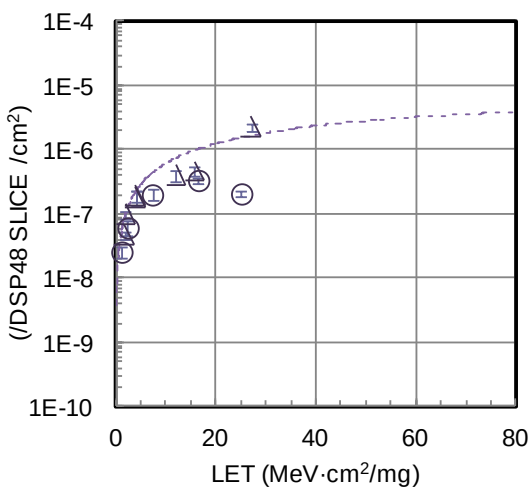


Figure 7.3. M Multiplier Output Register Static Cross-Section vs. LET.

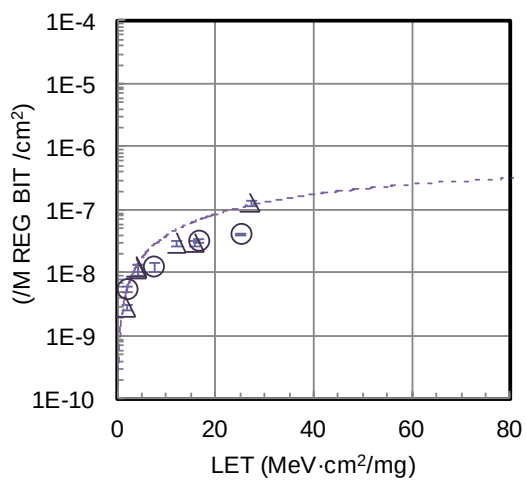


Figure 7.4. M Multiplier Output Register Bit Static Cross-Section vs. LET.

7.1.3 C Input Register

A static upset cross-section was captured; a plot vs. LET and a Weibull fit it is shown in Figure 7.5, and the bit cross-section is shown in Figure 7.6. As only circular points are shown, all the data is from the Berkeley cyclotron. The tests at Texas A&M were executed with a flawed data capture system and all C register static error data was lost, thus only LBNL testing data is shown.

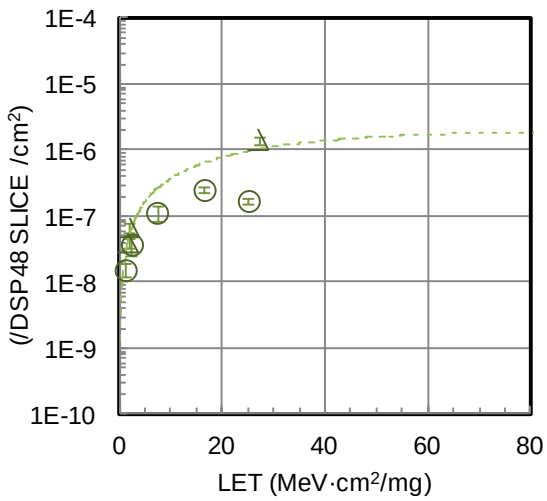


Figure 7.5. C Operator Input Register Set Static Cross-Section vs. LET.

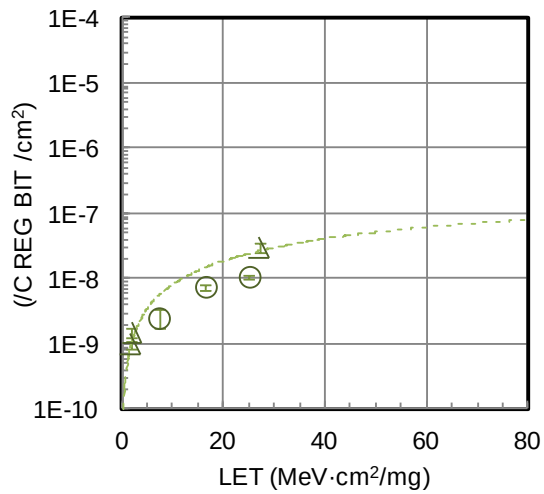


Figure 7.6. C Operator Input Register Set Static Cross-Section vs. LET.

7.1.4 A1, A2, B1 and B2 Input Register

A static upset cross-section for the concatenated value of the A1, B1 set, and of the A2, B2 set were captured; plots vs. LET and a Weibull fit it are shown in Figure 7.7 through Figure 7.10. Triangular data points were obtained at the Texas A&M cyclotron, while the circular points are from the Berkeley cyclotron. The cross-sections in for the 1 and 2 register sets are observed to be exactly the same for the registers and bit sensitivity. The A registers appear to have a slight increase in cross-section compared to the B registers, as can be seen in Figure 7.7 and Figure 7.9, while the A and B register bit cross-sections are essentially the same (Figure 7.8 and Figure 7.10).

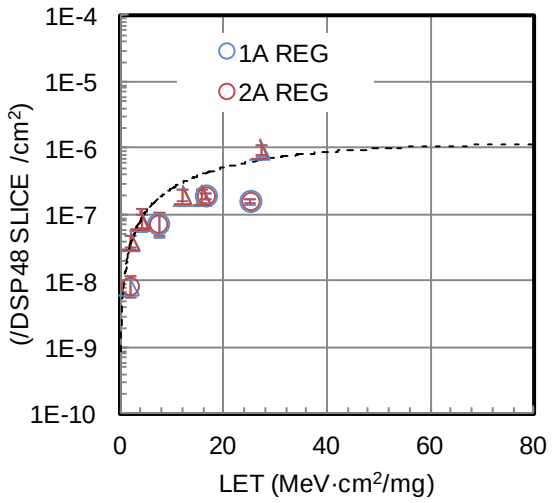


Figure 7.7. A1 and A2 Operator Input Registers Static Cross-Section vs. LET.

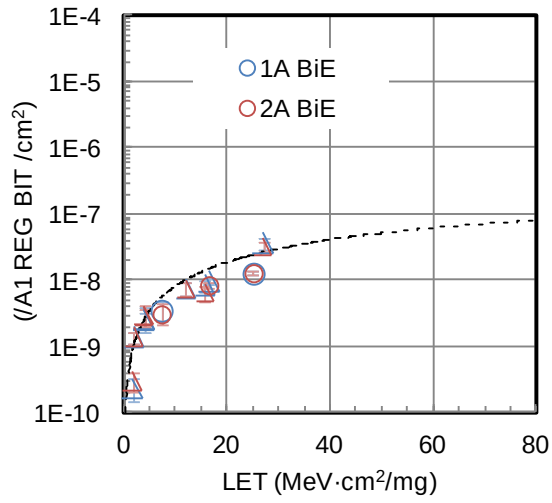


Figure 7.8. A1 and A2 Operator Input Registers Bit Static Cross-Section vs. LET.

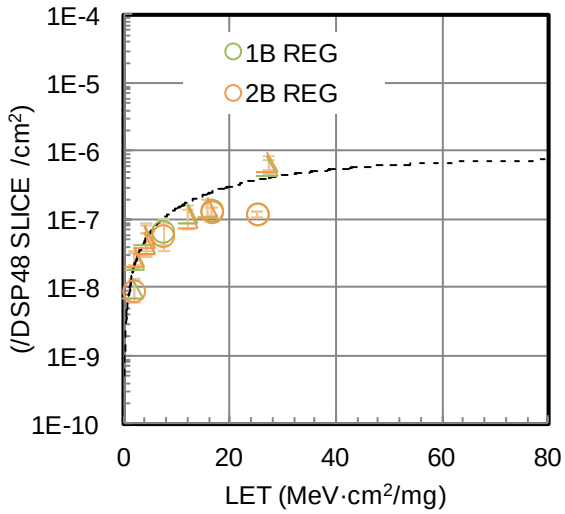


Figure 7.9. B1 and B2 Operator Input Register Set Static Cross-Section vs. LET.

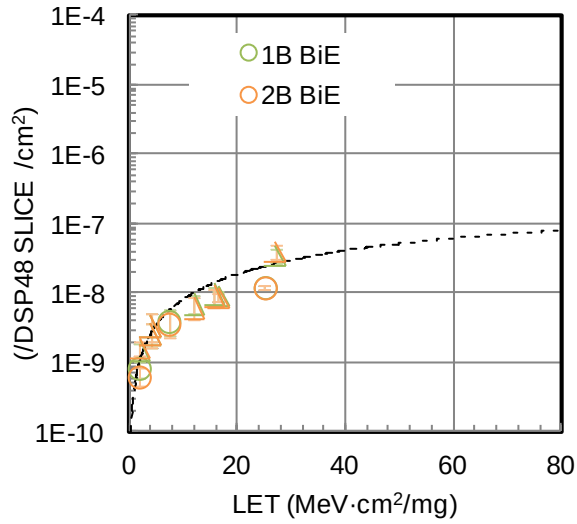


Figure 7.10. B1 and B2 Operator Input Registers Bit Static Cross-Section vs. LET

7.1.5 Static Test Summary

Static cross-sections were obtained for all the data-path registers; each of the register's saturated cross-section varied slightly, in between 8E-7/cm^2 and 5.5E-6/cm^2; with sharper knees for the internal DSP M registers, than for the P register and input operator registers (A, B and C). The bit susceptibility of the registers was observed to also be effectively the same, with a saturated cross-section of 1.5E-7/cm^2; excepting the Multiplier register, which was observed to suffer events with more than one bit in error per register significantly more often than the other registers. This is corroborated by the higher saturated cross-section of the M register bits, which is about a factor of 3 higher than the other registers. The Weibull parameters for all the static cross-sections are shown in Table 7.3.

Table 7.3. Static Test Results Weibull Parameters.

		WEIBULL PARAMETERS				
REGISTER	UNIT	LET th (MeV-cm^2/mg)	W (MeV-cm^2/mg)	S	SAT X-SEC (/cm2)	SAT X-SEC (/µm2)
P REG	/DSP48E CELL	0.1	35	1.25	2.00E-06	200
M REG	/DSP48E CELL	0.1	67	1.12	5.50E-06	550
C REG	/DSP48E CELL	0.1	35	1.25	2.00E-06	200
A REG	/DSP48E CELL	0.1	32	1.25	1.20E-06	120
B REG	/DSP48E CELL	0.1	36	1.25	8.00E-07	80
P REG BIT	/BIT	0.1	100	1.25	1.50E-07	15
M REG BIT	/BIT	0.1	80	1.20	5.00E-07	50
C REG BIT	/BIT	0.1	100	1.25	1.50E-07	15
A REG BIT	/BIT	0.1	100	1.25	1.50E-07	15
B REG BIT	/BIT	0.1	100	1.25	1.50E-07	15

7.2 Dynamic Tests

As discussed in Section 6, the three basic types of operations available from the DSP48E were tested, which are multiplication, addition/subtraction and accumulation. These tests took place at the LBNL cyclotron in May of 2009 and at the TAMU cyclotron in July and November 2009. The experimental log tables for the Accumulate, Addition/Subtraction and Multiplication tests are each respectively shown in Tables A.1, A.2 and A.3 in Appendix A. For the tests, each event that resulted in a DSP output error was counted and cataloged in to one of 4 categories depending on the events duration. They are listed below:

- *Category 1*: events of 1 to 3 test clock-cycles in duration.
- *Category 2*: events of 4 test clock-cycles to 50µs in duration.
- *Category 3*: events of 50µs to 800ms in duration.
- *Category 4*: events larger than 800ms in duration.

From these 4 categories, each event can be counted accordingly, and translated into meaning for each tests. For the accumulative tests, persistent, and non-persistent dynamic error SEUs are separated with confidence. For the multiplier and addition tests, separation of configuration-induced vs. intrinsically-induced (dynamic) SEUs is also feasible. Repeatable duration events are assumed to be a real indicator of a particular susceptible mechanism.

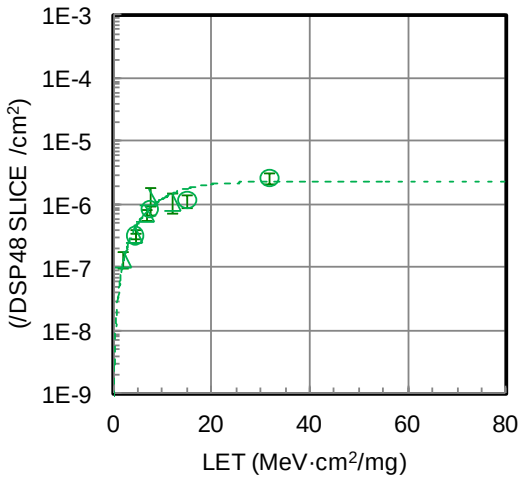


Figure 7.11. Cross-Section vs. LET for DSP Accumulative Operations.

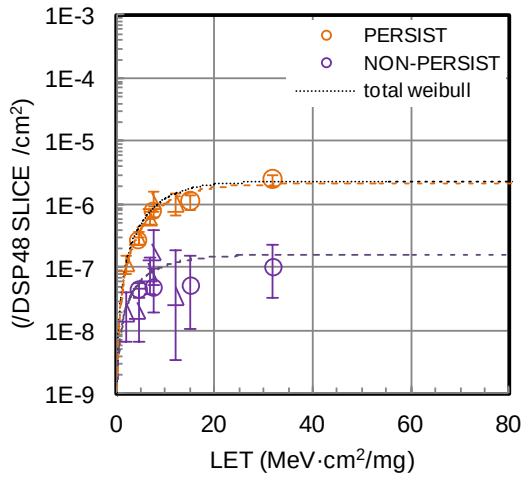


Figure 7.12. Persist and Non-Persist SEU Cross-Section vs. LET for DSP Accumulative Operations.

7.2.1 Accumulative Operations

The manual re-initialization required for persistent error correction was always engaged several seconds into the event, making for obvious separation of long lasting, persistent events from non-persistent, repeatable events. After binning across all possible ranges, the only repeatable events observed lasted less than 50µs, too quick of a time to be a result of the manual experimenter's intervention. Persistent SEUs include any events larger than 50µs, (categories 3 and 4), adjusting the sum with the SEFI count captured by the configuration manager. Non-persistent SEUs are obtained by summing counts from categories 1 and 2.

Cross-sections were obtained for all the events that resulted in an error of the accumulative operation, as shown in Figure 7.11. Figure 7.12 shows the persistent and non-persistent SEU cross-sections and fitted Weibull curves. Triangle markers indicated points obtained at 12.5MHz in the July 2009 tests, while the

circular markers are for data obtained at 6.25MHz in the November 2009 tests. As can be seen, under the conditions tested, the cross-section of non-persistent errors decreases by about an order of magnitude with respect to the persistent errors. Thus the large majority all of the SEUs induced by the DSP48E while doing an accumulative operation will more than likely cause the accumulation operation sequence to be in error until re-initiated.

7.2.2 Addition Test

The DSP addition test exercised the adder/subtractor element of the DSP48E. All SEU events observed during this test showed to recover by 800ms, well within the configuration manager's re-configuration, read-back and scrub expected timelines. The DUT FPGA was irradiated under continuous read-back and scrub cycles by the configuration manager, thus any upset to a critical configuration bit would result in a random duration event within the system's read-back and scrub execution timelines. As for the accumulation tests, event duration repetition was observed only below 50µs. Configuration upsets are then the sum of category 3 and 4 counts, subtracting the SEFI counts as well, while dynamic or intrinsic SEU events are provided by categories 1 and 2.

The cross-section is showed in Figure 7.13. As for the accumulation tests, triangle markers indicated points obtained at 12.5MHz in July 2009, circular markers are for data obtained at 6.25MHz in November 2009, and the square marker are for the data obtained a LBNL in May of 2009. The LBNL data point demonstrates some type of inconsistency in the experiment rendering a very small cross-section. The data point is ignored in the Weibull curve fit.

7.2.3 Multiplication Test

The DSP multiplication tests exercised the multiplier element of the DSP48E. As with the addition tests, dynamic vs. configuration source event separation is possible, and all SEU events showed to either recover within 50us, or within an amount of time in accord with the configuration manager's re-configuration and scrub timelines. The cross-section is showed in Figure 7.14. Triangle markers indicated points obtained at 12.5MHz in July 2009, circular markers are for data obtained at 6.25MHz in November 2009, and the square marker are for the data obtained a LBNL in May of 2009. The LBNL data points demonstrate some type of inconsistency in the experiment rendering a very small cross-section. The data point is ignored in the Weibull curve fit.

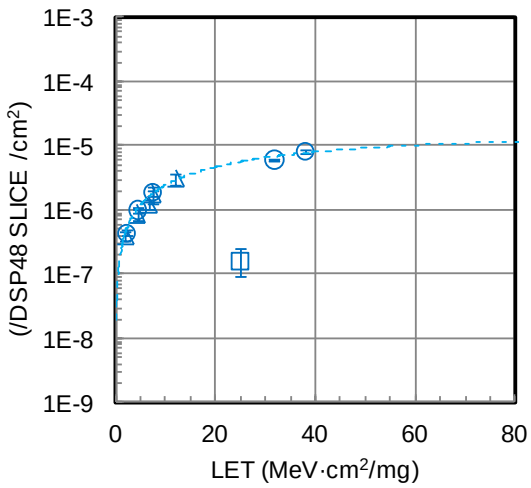


Figure 7.13. Cross-Section vs. LET for DSP Addition Operations.

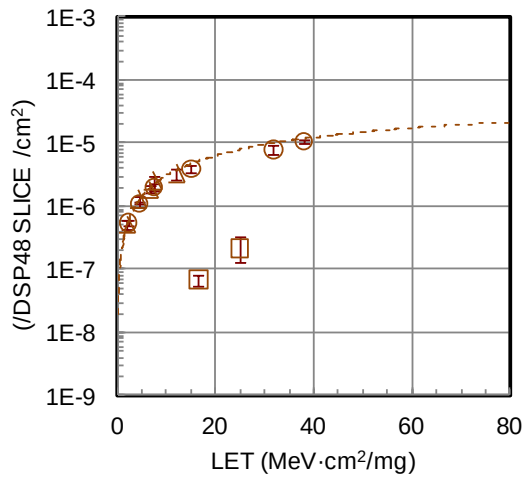


Figure 7.14. Cross-Section vs. LET for DSP Multiplication Operations.

7.2.4 Dynamic Test Summary

Dynamic cross-sections were obtained for the fundamental dynamic operations of the DSP, which are multiplication, addition and accumulation. Multiplication operations demonstrated the largest cross-section, closely followed by the addition operations, and both have a significantly higher cross-section than observed for the accumulative tests, by approximately an order of magnitude. This is expected since from the static experiments the multiplier registers are the most sensitive, and are only used by the multiplication test, which also makes use of input operator registers. The accumulative tests, on the other hand, only one DSP register is employed, the P output register. The addition test makes use of P and input operator registers (A, B and C). The cross-section Weibull parameters extracted for each test are shown in Table 7.4.

Table 7.4. Dynamic Test Results Weibull Parameters

	BASIC DSP OPERATON TYPE:		
	MULTIPLY	ADD/ SUBSTRACT	ACCUMULATE
	[*a* x *b*]	[*a* ± *b*]	[Σ (*p*)]
WEIBULL PARAMETERS	/DSP48E CELL	/DSP48E CELL	/DSP48E CELL
LET th (MeV-cm²/mg)	0.1	0.1	0.1
W (MeV-cm²/mg)	89	44	11.5
S	1.11	1.08	1.09
SAT X-SEC (/cm²)	3.65E-05	1.35E-05	2.28E-06
SAT X-SEC (/µm²)	3650	1350	228

8. DATA ANALYSIS

8.1 SEE Duration

SEEs with highly repeatable durations are assumed to indicate a particularly susceptible SEE source mechanism. All of the events recorded and their duration signatures are summarized in Figure 8.1 and

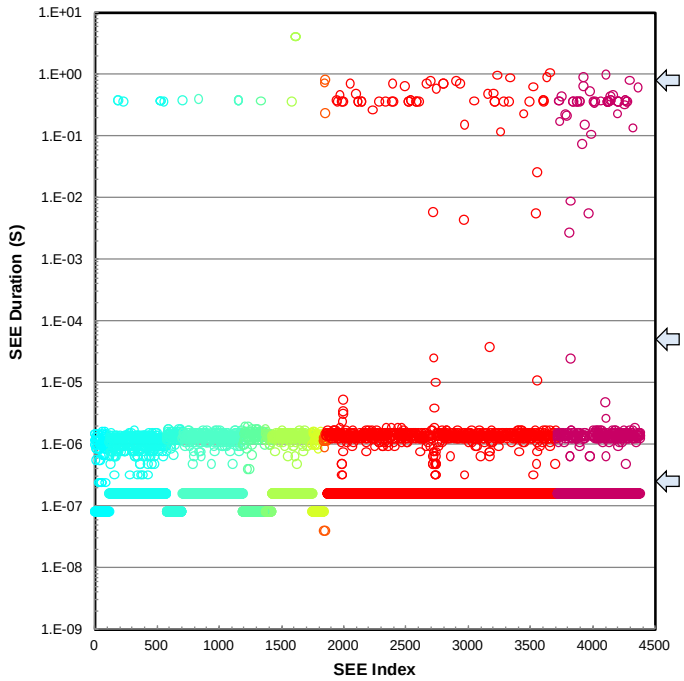
Figure 8.7. In these charts, each event is represented with a circle, and they are ordered by occurrence within each run, and then each run is ordered by the LET used left-to-tight. These plots show every event observed, including SEFI-induced events. The color scale variations illustrate the different LETs utilized; ranging from 2.0 (light blue), to 15.0 (yellow), and 38.0MeV·mg/cm^2 (burgundy). On each plot, several distinct signatures can be clearly identified for each operation, and these are used to define the category time limits. Arrows indicate the limits for each of the duration categories, which were kept the same across operations. They are:

- *Category 1*: events of 1 to 2 test clock-cycles in duration ($2 \times T_{CLK}$).
- *Category 2*: events of 3 test clock-cycles to 50µs in duration.
- *Category 3*: events of 50µs to 800ms in duration (approximately $2 \times T_{ReConfig}$).
- *Category 4*: events larger than 800ms in duration.

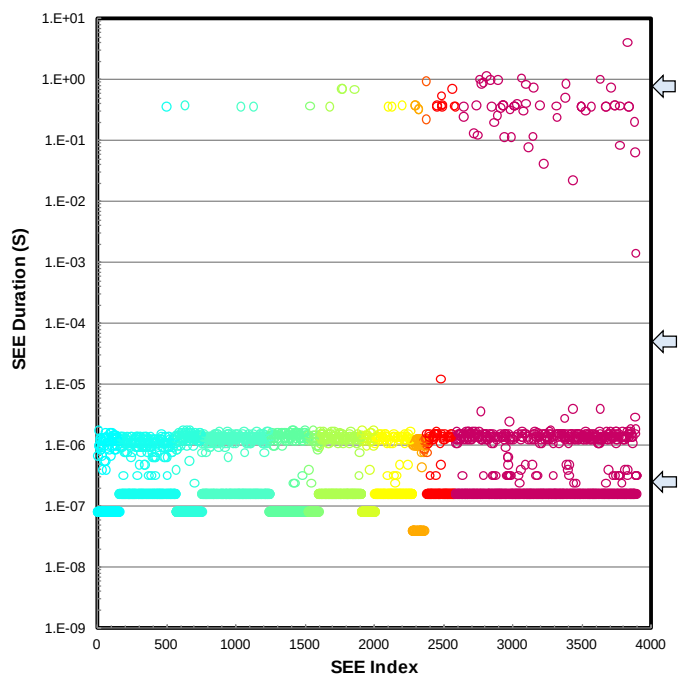
From these four categories, any event can be grouped accordingly, allowing for event separation. For the multiplier and addition tests, separation of configuration-induced vs. intrinsically-induced (dynamic) SEUs is feasible. While for the accumulative tests persistent and non-persistent dynamic error SEUs are believed to be separated with confidence. The counts for each category, for each DSP test structure and each run is shown in Appendix B.

8.1.1 Addition and Multiplication Operations

As can be seen in Figure 8.1, the SEEs for these operations showed much repeatability at the test frequency clock period (40, 80 and 160 ns), and at a time just over 1.0µs. Also showing repeatability are events lasting approximately the device's re-configuration black-out period (~357ms). Two particular events, one for the multiplication and additions tests, were also observed to last much longer than the other events (approximately event no. 1,500 in Figure 8.1 (a) and event no. 3,800 in Figure 8.1 (b)). These events are believed to be due to experimental artifacts, including operator error during experimentation. The singularity and rarity of these lone events deems them worthy of noting but not of any further discussion.



(a) Addition.



(b) Multiplication

Figure 8.1. Event duration charts of the Addition (a) and Multiplication (b) tests.

8.1.1.1 Category 1 Events : $\{T_{Duration} \leq (2 \times T_{CLK})\}$

These events, lasting the duration of the test frequency clock-period, appear to be induced by any one of the registers that make up the test structures critical to the operation. Since the DSP test structures were

continuously being clocked and enabled, these events are more than likely due to a combination of effects that multiple source mechanisms have on a register, and always corrected by the following clock-cycle. The category time limit selected to represent these events included any event that lasted two test clock periods or less, so for 6.25MHz, this includes any event lasting less than 320ns, 160ns for 12.5MHz and 80ns for 25MHz. The cross-sections for these sub-types are shown in Figure 8.2 for the additions tests and in Figure 8.3 for the multiplication tests. The three-dimensional graphs illustrated in Figure 8.4 on page 36, show the high cross-section of these events with respect to the other highly repeatable events observed.

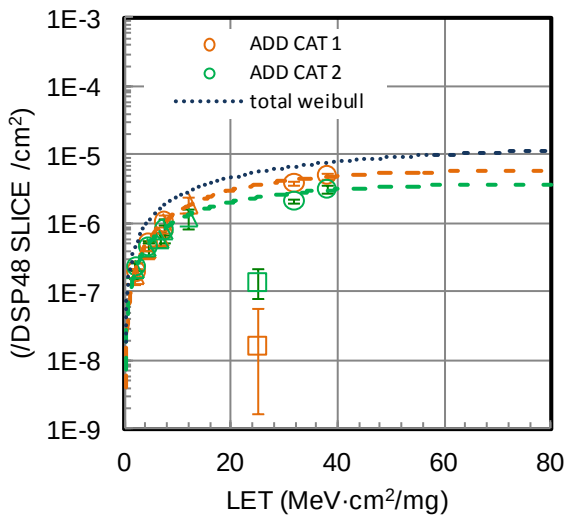


Figure 8.2. Addition Categories 1 and 2 Cross-Sections vs. LET.

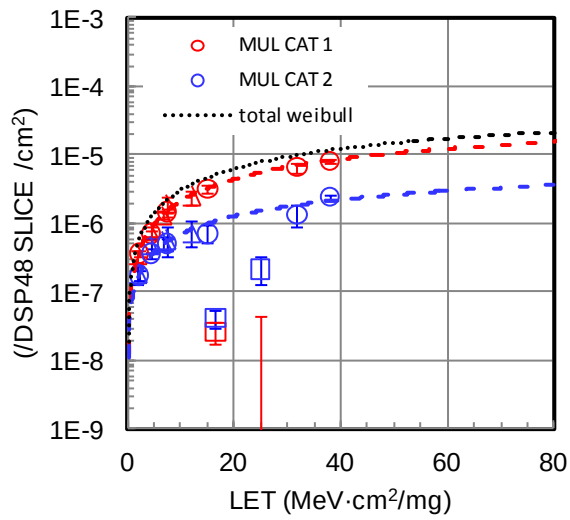
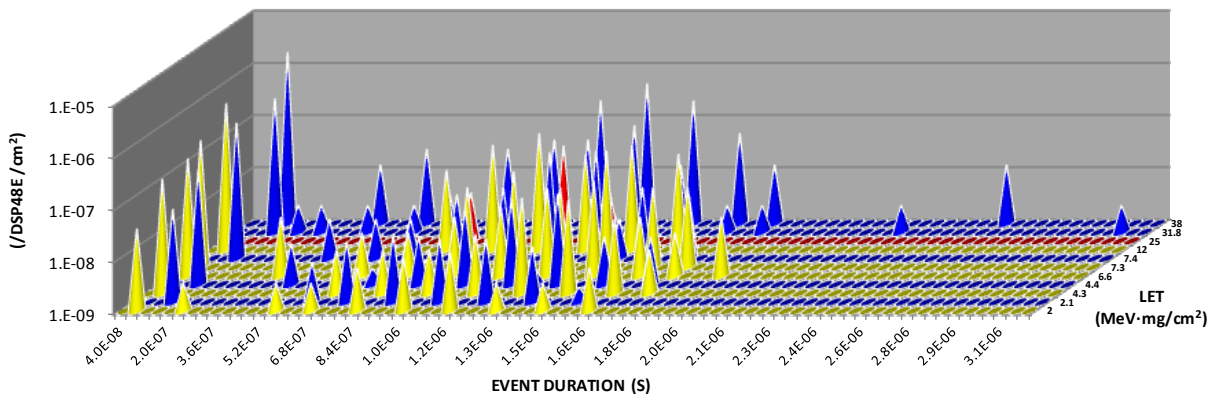


Figure 8.3. Multiplication Categories 1 and 2 Cross-Sections vs. LET.

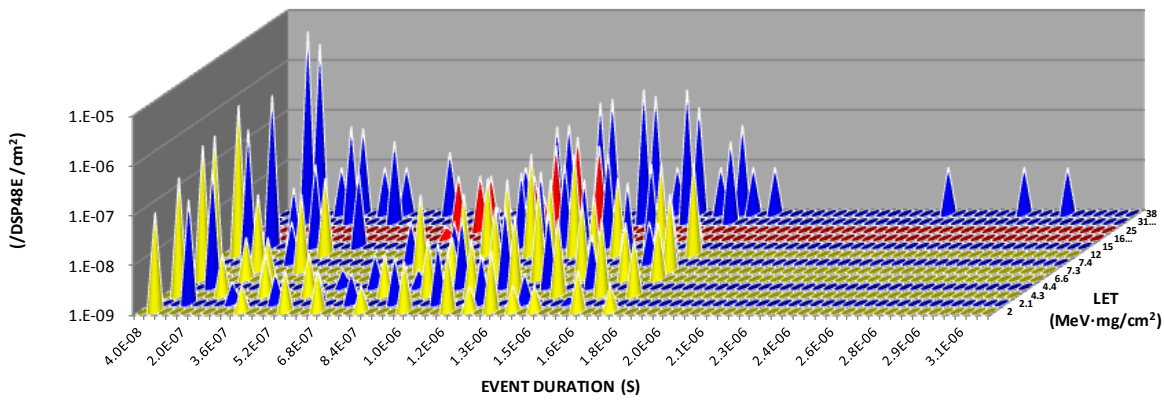
8.1.1.2 Category 2 Events: $\{(3 \times \boldsymbol{T_{CLK}}) \leq \boldsymbol{T_{Duration}} < 50\mu s\}$

All events in between 2 clock-cycles and 50µs were collected into this category. These events do not show much frequency dependence; since as the test frequency was modulated from session to session, the duration times remain consistent (Figure 8.1) and cross-sections do not vary significantly (Figure 8.4). The changes in frequency can be induced in Figure 8.1 from the changes in the single clock-period upset durations. From Figure 8.4, a resemblance of a Gaussian distribution appears, centered near duration times of 1.0 and 1.4µs, with many events demonstrating a worst-case duration variability of 800ns in the negative direction, and up to 2.5µs in the positive direction. It must also be noted, that observing Figure 8.1 closely, the duration center of these events appears to slightly increase from 1.0µs to 1.4µs as the LET is increased. This effect is spotlighted in the plot shown in Figure 8.5 on page 37. The source of these types of events is uncertain at the time of this write-up, but the susceptibility at low LETs and the high repeatability demonstrated, make these phenomena very interesting.

The cross-section of these events are significantly lower than the Category 1 events for specific duration bins, but if all events in the category are counted as such, the overall cross-section is much closer to the one measured for Category 1, as can be seen in the plots of Figure 8.2 and Figure 8.3. Here, it can be observed that for multiplication operations, the increase in Category 1 events is mostly responsible for the increase of the overall cross-section difference in between multiplication and addition operations, but the Category 2 event cross-sections, pending Weibull fit accuracy, are very close for both types of operations.



(a) Addition



(b) Multiplication

Figure 8.4. Event Cross-Section vs. LET vs. Event Duration, in 40ns Bins.

Shown for Addition (a) and Multiplication (b) operations; each cone represents a 40ns event bin, and each color indicates a different test frequency (Blue = 6.25MHz, Yellow = 12.5MHz, and Red = 25MHz).

8.1.1.3 Category 3 and Category 4 Events: {$T_{Duration}$ > 50µs}, and {$T_{Duration}$ > 800ms}

The DUT FPGA was irradiated under continuous read-back and scrub as dictated by the configuration manager; any upset to a critical configuration bit would result in an event of random duration but within the system's read-back and scrub execution timelines. As shown in Figure 8.1, random duration events were observed lasting anywhere in between tens of micro-seconds to hundreds of milliseconds. These random duration events appeared with higher LETs, corroborating with the known hardness of the Virtex-5QV configuration cells (5).

From test-bench measurements, the nominal black-out (down time plus recovery time) time required by a re-configuration cycle ($T_{ReConfig}$) initiated by activating the device's PROG pin was approximately 357ms. It was decided to use approximately twice that re-configuration time as the limit in between normal recovery times, and abnormally long recovery times. Then Category 3 events are made up of the events lasting in between 50µs and 800ms, while Category 4 are made up of any events lasting longer than 800ms.

Almost all of the SEU events observed during these tests were shown to recover by 800ms, or within what is considered a normal recovery time. Curiously though, at LETs higher than 30MeV·mg/cm^2, slightly repeatable events are observed to last nearly ~1,600ms, demonstrating an effect whose outcome

appears to require several re-configuration cycles to recover. This effect is of very low susceptibility and is beyond the scope of this investigation and analysis, but may be useful in supporting configuration recovery investigations.

To obtain the upset rate of configuration image of a DSP48E cell, the sum of the events in both of categories 3 and 4 is used. SEFI events were removed from the data set, and the number of events summed was extracted from the multiplication and addition tests only. The resulting cross-section of these events, deemed configuration upset related, is shown in Figure 8.6. Even though this cross-section is obtained from the particular addition and multiplication tests exercised here, it should be a good representation of the configuration image upset rate for many DSP48E implementations, since they use all fabric input operators and registers, as well as the control and multiplication registers.

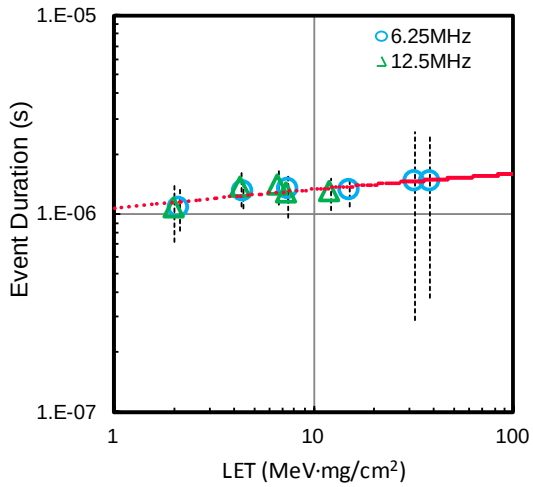


Figure 8.5. Category 2 Event Duration Avg. vs. LET.

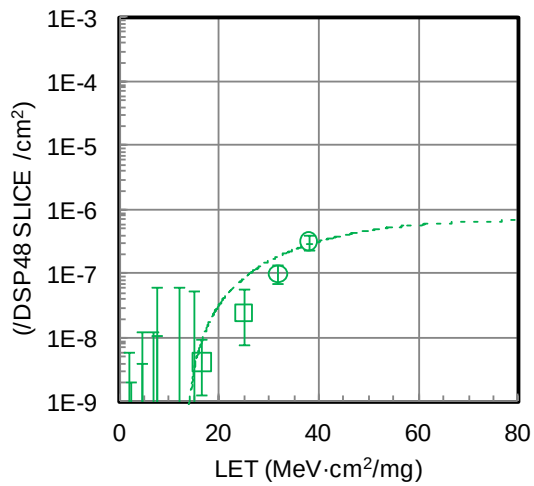


Figure 8.6. Cross-Section vs. LET for DSP48E configuration bit upsets.

8.1.2 Accumulative Operations

Accumulative operations are unique in the fact that each accumulative operation in a sequence depends on the value obtained in previous clock-cycle's operation. Thus, when an accumulative function becomes corrupt, it will continue to be corrupt until the operation is either corrected, re-initialized or re-seeded. The accumulative test system devised here was no different, with manual re-initialization required to correct the accumulative test sequence.

The event duration timers were designed to top-off at 4.096 seconds, and the manual re-initialization was always engaged either just short of this time or beyond this time. This effect can be visualized in Figure 8.7, where event durations are shown to assemble at 4.096 seconds and below. The re-initialization function was common to all the DSP test structures, so when engaged, all test structures were re-initialized simultaneously, whether upset or not. This aspect of the test system was observed to sometimes interfere in the SEU duration times captured. In some occasions, by the time re-initialization was decided to be engaged to recover a test structure deemed corrupt, another test structure that had just become corrupt was also corrected, resulting in an event for that test structure with a shorter duration time than expected. This is shown by the capture of events lasting as little as 100msec.

The relatively larger duration times makes for obvious separation of long lasting, non-self-recovering (*persistent*) events from self-recovering (*non-persistent*) events. As can be seen in Figure 8.7, (non-

persistent) repeatable events can be extracted from Categories 1 and 2, and persistent from events from (Categories 3 and 4).

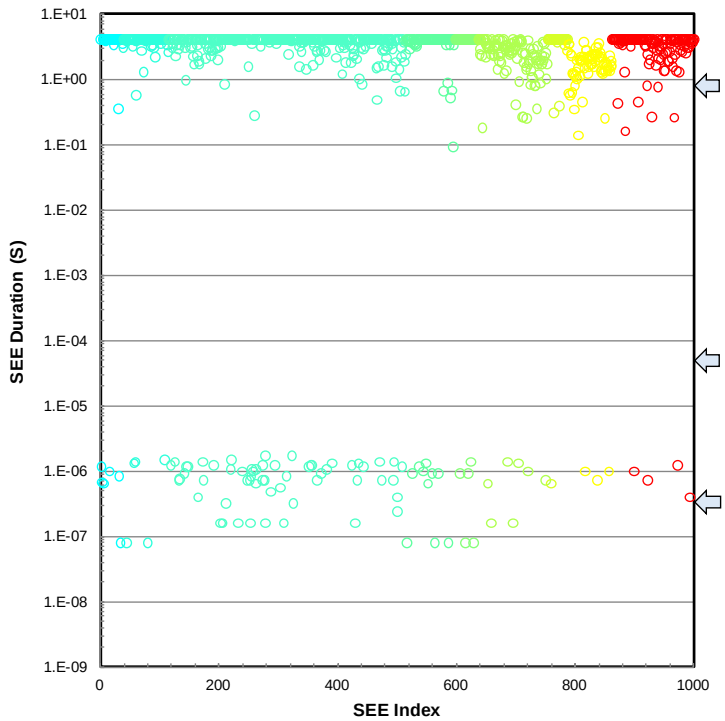


Figure 8.7. Event duration chart of the Accumulation tests.

The sampling system's maximum time recording capability for any event is 4.095s.

8.1.2.1 Categories 1 and 2: {$T_{Duration}$ < 50µs}

These events are too short in duration to be a result of the manual experimenter's intervention, and demonstrate too much repeatability to be a result of the global re-initialization command interference discussed above. Also, their duration appears to center around 1.0µs, in the same fashion as the Category 2 events of the addition and multiplication tests. As with those cases, the source of this effect is uncertain at the time of this write up, but the fact that self-recovering events exist in a feed-back system where the only register utilized is at the center of the feed-back element, is, at first sight, counter-intuitive. Figure 8.8 shows the distribution of each event's duration in 40ns bins; the durations of the events that are self-correcting appear to be centered near 1.0 to 1.4µs, in the same fashion as the addition and multiplication tests.

Figure 7.12 shows the persistent and non-persistent SEU cross-sections and fitted Weibull curves. As can be seen, under the conditions tested, the cross-section of non-persistent errors decreases by about an order of magnitude with respect to the persistent errors. Thus the large majority all of the SEUs induced by the DSP48E while doing an accumulative operation will more than likely cause the accumulation operation sequence to be in error until re-initiated. Figure 8.10 shows the distribution of Category 1 and Category 2 events, and here it is demonstrated that Category 2 events dominate over Category 1 events for the cases where the accumulative operation is only temporarily affected. As in the previous cross-section figures, triangular markers represent data taken at 12.5MHz and circular markers data taken at 6.25MHz.

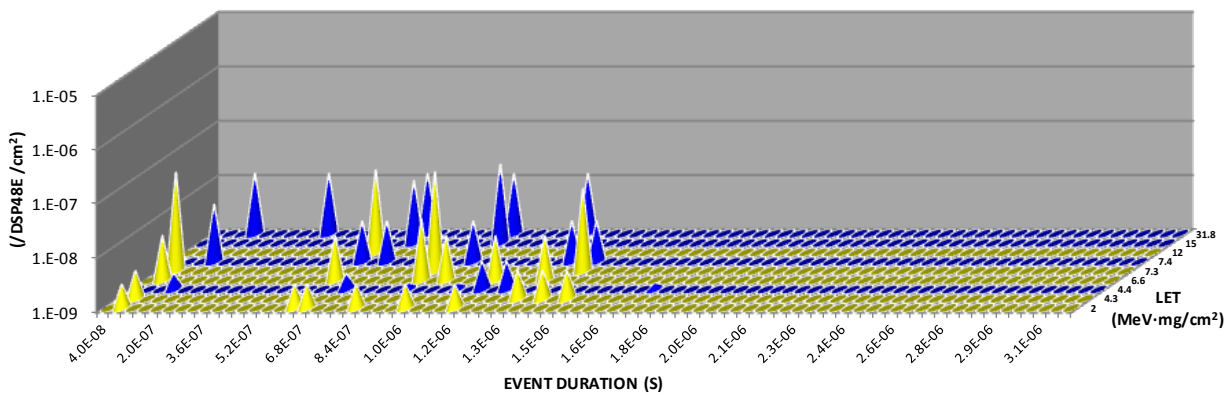


Figure 8.8. Accumulative Tests Event Cross-Section vs. LET vs. Event Duration, in 40ns Bins.

8.1.2.2 Categories 3 and 4: {$T_{Duration}$ > 50µs}

The events measured for the accumulation tests that fall in this category were used to generate the Persist cross-section shown in Figure 7.12. The SEFI counts noted during the experiments were removed from this data set as well.

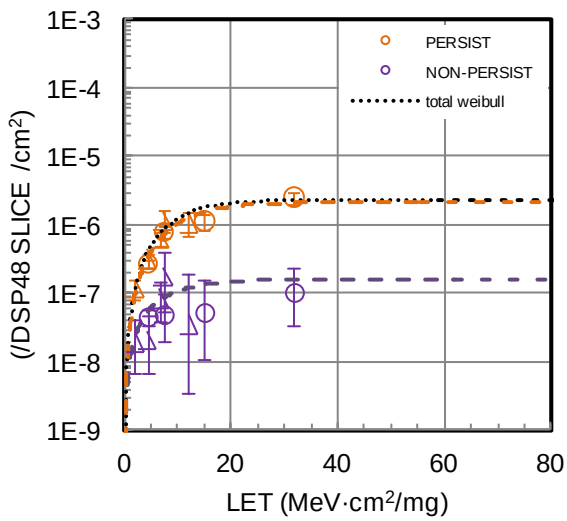


Figure 8.9. Accumulative Persist and Non-Persist SEU Cross-Section vs. LET.

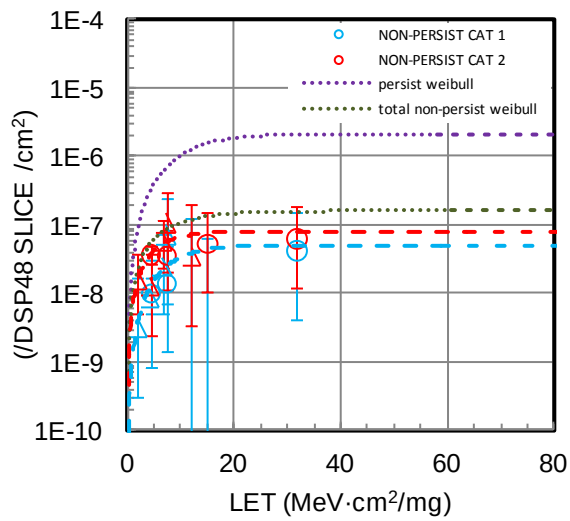


Figure 8.10. Accumulative Non-Persist SEU Cross-Sections vs. LET.

8.2 Multiple Element Upset (MEU) SEEs

Recent work by the authors has demonstrated the existence of SEE source mechanisms in FPGAs that are susceptible to heavy-ions, and whose effects manifest simultaneously in multiple elements of the FPGA(6). These Multiple Element Upsets (MEUs), which in this case affect DSP cells, must be carefully observed, since they can potentially corrupt internal mitigation structures. Systems that depend on an alternate element to correct or detect an erroneous situation are susceptible to this effect since this type of upset can bring down both of the main and reference elements.

Figure 8.11 below indicates the locations of the DSP48E cells tested; in all test cases, non-cascaded DSP cells were utilized. Regardless, measurements were observed during the testing where all test structures in the full design would suffer an error at precisely the same time, and for the same amount of time. Figure 8.12 below reproduces the event duration plots, but each event common to more than one test-structure is now marked with an 'X'. To determine coincident start times across test structures, start times within 1.0µs were considered as coincident. It must be noted that after extracting the coincident data set, all start times were observed to be synchronized to ten nanoseconds.

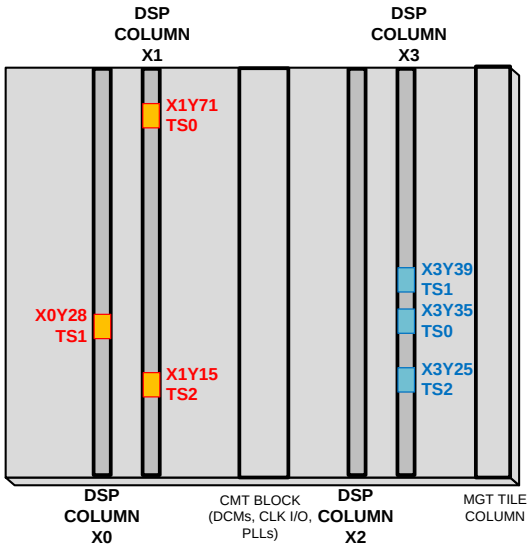


Figure 8.11. Virtex-5QV dice diagram with the approximate locations of DSP48 columns and test structures implemented.

Red indicates locations used for May and July 2009 test structures; blue indicates locations for November 2009 test structures.

As can be observed in the Figure 8.12 (b) and (c), common events are observed to have the signature of the DUT FPGA re-configuration black-out, which may last approximately 357ms or more. The Multiplication and Addition operations also demonstrate common events with a Category 2 SEU signature, which from section 8.1.1.2, are brief, frequency independent effects causing upsets lasting around 1.0µs. A handful of Category 1 (single clock-cycle) events were also counted across all tests. For the Accumulative tests, all of the common events' duration times are either at 4.096 seconds or slightly below, from Figure 8.12 (a). The shorter durations in this case are due to the test operator re-seeding the accumulative string before the counters reached their respective 4.096 second limit. So in the accumulation tests, any common event, regardless of source mechanism, always manifested as a long-lasting event.

The observance of common events in the Multiplication and Addition tests with Category 2 signatures corroborates with the belief that the main source of the frequency independent signatures is due to SETs on the clock tree of the DSP48 registers being used(7). In the test design being used here, the clock to all the test structures is the only known shared element none configuration related. A handful of common, single clock-cycle (i.e., with the frequency-dependant signature) are observed in Figure 8.12 (b) and (c), indicating that these clock-line transients may sometimes manifest as a single clock-cycle corruption. Thus the single-clock cycle upsets discussed in Section 8.1.1.1 may not be only due to frequency dependant mechanisms; but are a result of a combination of frequency and non-frequency dependant effects.

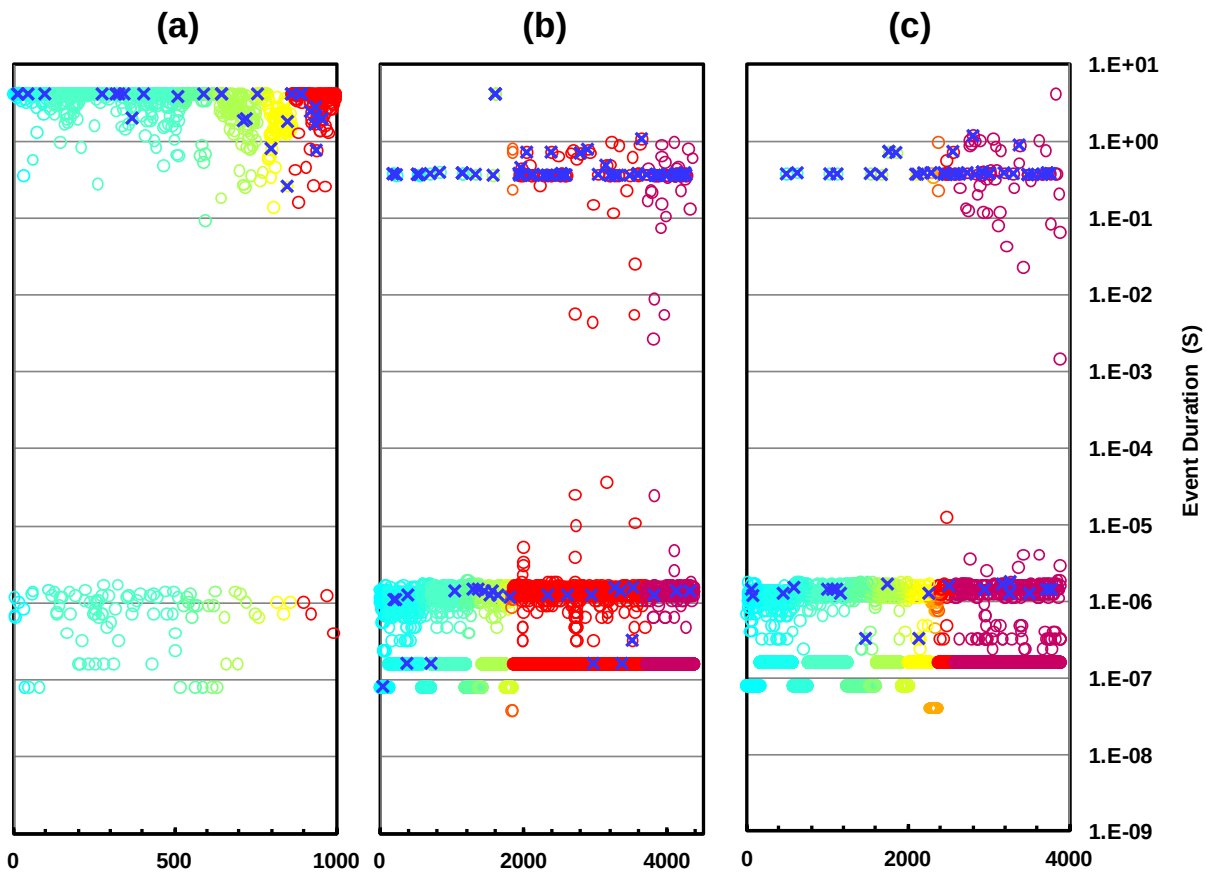


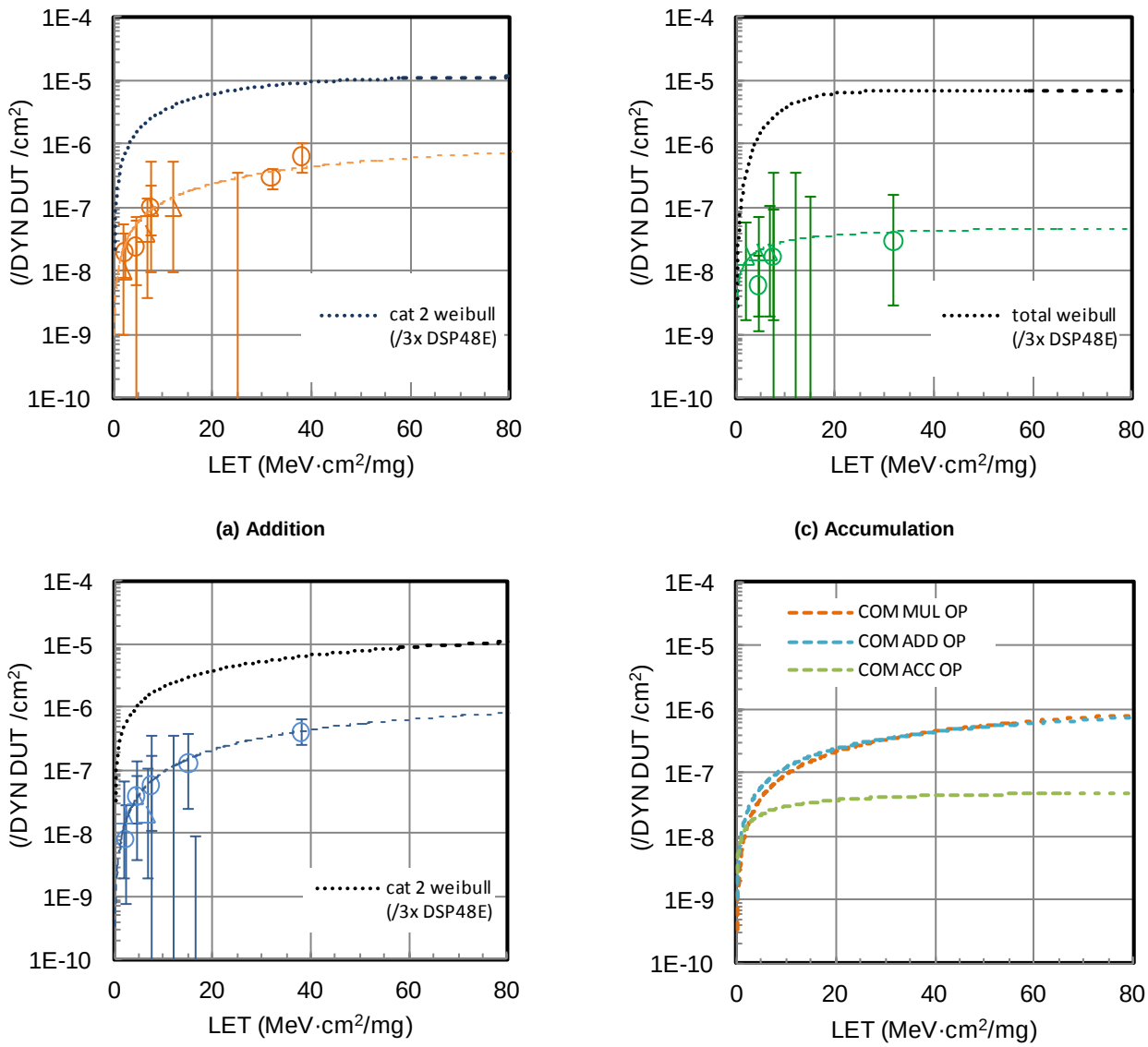
Figure 8.12. Event Duration Charts with MEU events.

Events common to all DSP48E test structures marked with an 'X'; for Accumulation (a), Addition (b) and Multiplication (c) operations.

The cross-sectional plots shown in Figure 8.13 on page 42 are for the all the MEU elements measured, having removed the counts induced by configuration engine SEFIs incurred during the experiment. And on page 43, the 3-dimendional diagram of Figure 8.14 illustrates the low cross-section of the MEUs, and the slightly more pronounced frequency-independent duration signature ($T_{Duration}$ approximately 1.0 to 1.4µs).

From Figure 8.13, for the Multiplication (a) and Addition (b) tests, the nominal SEU cross-section is shown, with units adjusted for 3 DSP test structures (the entire DUT design). Here it can be seen that

MEUs are about an order of magnitude less frequent than single DSP upsets. For the accumulative tests (c), the cross-section of MEUs is several orders of magnitudes less. In the cross-sections of (d), the Weibull fits obtained for each operation are plotted together, showing how the multiplication and addition operations, which effectively utilize the same amount of registers, are equal in the eyes of the MEU source mechanism. The Accumulation tests on the other hand, with only a single 48-bit register, show a significant lower susceptibility.



(a) Addition

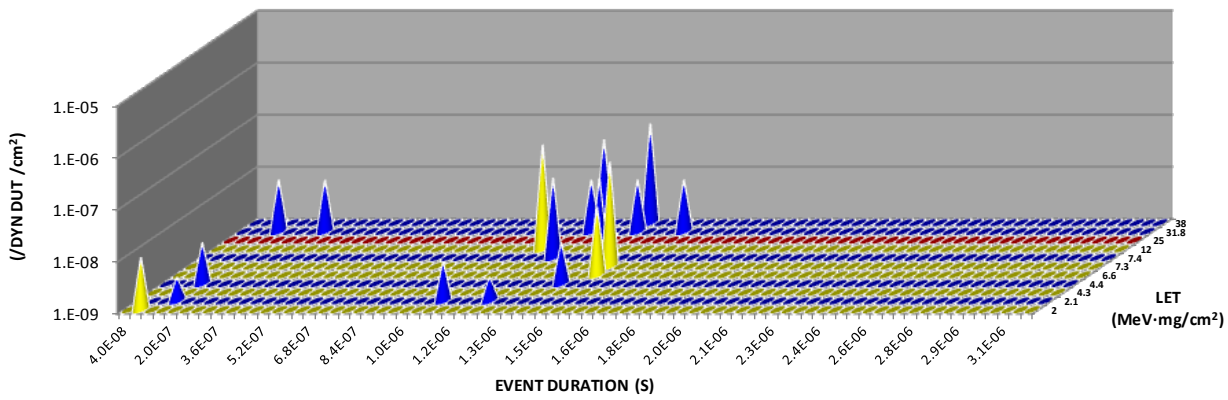
(c) Accumulation

(b) Multiplication

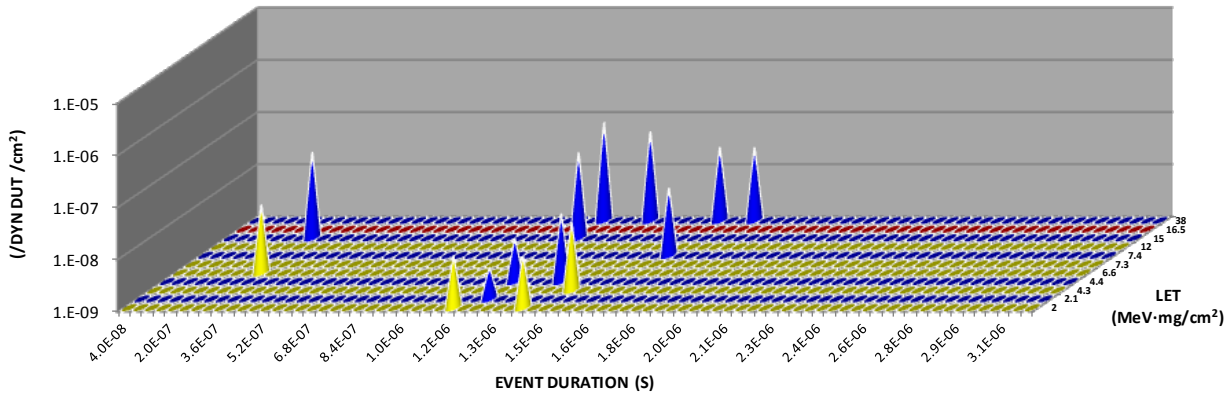
(d) Weibull fits for MEUs all operations.

Figure 8.13. Plots of Cross-Sections vs. LET for Common SEUs.

Reference Weibull curves have been adjusted for units of 3 DSP48E cells (a full DUT design).



(a) Addition



(b) Multiplication

Figure 8.14. MEU Event Cross-Section vs. LET vs. Event Duration, in 40ns Bins.

Shown for Addition (a) and Multiplication (b) operations; each cone represents a 40ns event bin, and each color indicates a different test frequency (Blue = 6.25MHz, Yellow = 12.5MHz, and Red = 25MHz).

8.3 System Impact Analysis

The actual impact of the SEEs measured in the DSP48cells needs to be translated to information that can be applied to an actual FPGA design for analysis in order to understand the impact of the SEE environment. The dynamic results should represent a real application of the DPS48Es, since the features of the DSP48 cells utilized by the test structures are the same features as ones utilized by real applications.

8.3.1 On-orbit Static Upset Predictions

The Weibull parameters of Table 7.3 were applied to the on-orbit prediction tool CRÈME-MC (8), using the method described in Appendix D. The results are shown in Table 8.1 below. All of the static upset probabilities are extremely low, never predicted to occur more than once every 100 years in the case orbit used.

Table 8.1. Orbital upset rates for DSP Static SEUs.
(0.150" Al shielding; Geosynchronous orbit)

REGISTER	UNIT	EVENT RATE /DAY	DAYS FOR UPSET	YEARS FOR UPSET
P REG	/DSP48E CELL	1.73E-05	57,754	158.2
M REG	/DSP48E CELL	3.52E-05	28,373	77.7
C REG	/DSP48E CELL	1.73E-05	57,754	158.2
A REG	/DSP48E CELL	1.23E-05	81,446	223.1
B REG	/DSP48E CELL	1.00E-05	99,889	273.7
P REG BIT	/BIT	3.20E-07	3,125,000	8,561.6
M REG BIT	/BIT	1.83E-06	547,645	1,500.4
C REG BIT	/BIT	3.20E-07	3,125,000	8,561.6
A REG BIT	/BIT	3.20E-07	3,125,000	8,561.6
B REG BIT	/BIT	3.20E-07	3,125,000	8,561.6

As expected form the Weibull parameters, the overall register susceptibility is slightly higher for the M register compared to the others, due to the M register sensitivity. The other register upset rates vary according to register size. For the single bit susceptibility of each register, the higher sensitivity of the Multiplier registers, with an order of magnitude increase in saturated cross-section, is also evident. The upset probability per day for each of the registers and each of their bits is shown in the bar graphs of Figure 8.15.

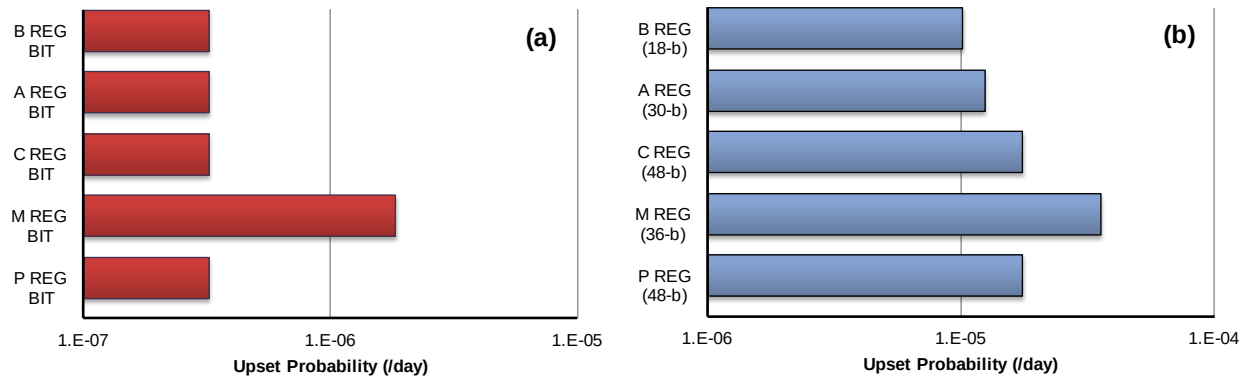


Figure 8.15. On orbit Upset Probability of the DSP48E registers (b), and their bits (a). (0.150" of Al shielding; Geosynchronous orbit)

8.3.2 On-orbit Dynamic Upset Predictions

The Weibull parameters of Table 7.3 were applied to the on-orbit prediction tool CRÈME-MC (8), using the method described in Appendix D. The results are shown in Table 8.2 below. All of the dynamic upset probabilities are moderate never predicted to occur more than once every 10 years in the case orbit used.

Table 8.2. Orbital upset rates of basic DSP Operations. (0.150" Al shielding; Geosynchronous orbit)

	BASIC DSP OPERATON TYPE:		
	MULTIPLY	ADD/ SUBSTRACT	ACCUMULATE
	[*a* x *b*]	[*a* ± *b*]	[Σ (*p*)]
	/DSP48E CELL	/DSP48E CELL	/DSP48E CELL
EVENT RATE /DAY	1.82E-04	1.57E-04	3.78E-05
DAYS	5,480	6,376	26,464
YEARS	15.0	17.5	72.5

As expected, the multiplication operations are the most sensitive, since in the fashioned tested they employ the M register, output register and input operator registers. The addition tests employ the input and output operator registers, so the on-orbit upset rate is slightly less. The accumulation tests employ only the output register, and have the lowest upset rate.

8.3.3 Static SEE susceptibility and Dynamic SEE susceptibly

The static and dynamic susceptibilities can be compared by evaluating the register use of each operation. Each of the registers used in the operation will contribute to the static component of the overall susceptibility.

8.3.3.1 Multiply Operations

Figure 8.16 illustrates the register and logic path of the multiply operation used in the dynamic tests. The registers involved in the operations are the A1, A2, B1, B2, M and P registers, so all of them must included in the static component. The static contribution is summed in Table 8.3. Thus at the frequencies tested, the static upset contribution to the susceptibility of the DSP multiply operation is about half of all the SEE susceptibility.

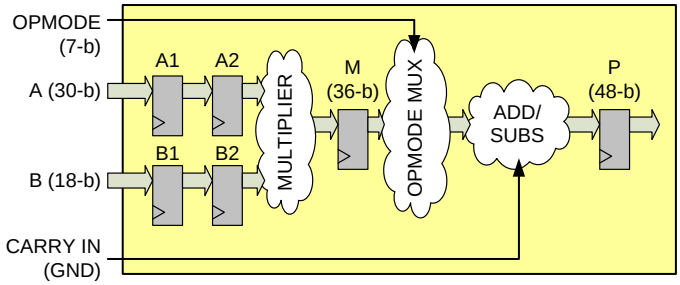


Figure 8.16. DSP48E register path for the multiply operation dynamic tests.

Table 8.3. Multiply Operation Static Register Components.

P_{A1Reg} (/day)	$P_{A2\ Reg}$ (/day)	$P_{B1\ Reg}$ (/day)	$P_{B2\ Reg}$ (/day)	$P_{M\ Reg}$ (/day)	$P_{P\ Reg}$ (/day)	**Total Static (/day)**
1.23e-5	1.23E-5	1.23E-5	1.23E-5	3.52E-5	1.73E-5	**1.01E-4**
					Total Dynamic (/day)	**1.82E-4**
					Static Component of Multiply Operation:	**56%**

8.3.3.2 Addition Operations

Figure 8.17 illustrates the register and logic path of the addition operations used in the dynamic tests. The registers involved in the operations are the A1, A2, B1, B2, and P for one clock cycle and C and P for the other clock-cycle. The addition test alternated input operators every clock cycle to maintain data variability. To estimate the static component contribution in this case, the upset contribution of the registers that are used on very other clock cycle is then halved.

The static contribution is summed in Table 8.3. Thus at the frequencies tested, the static upset contribution to the susceptibility of the DSP addition operations are about half of all the dynamic SEE susceptibility.

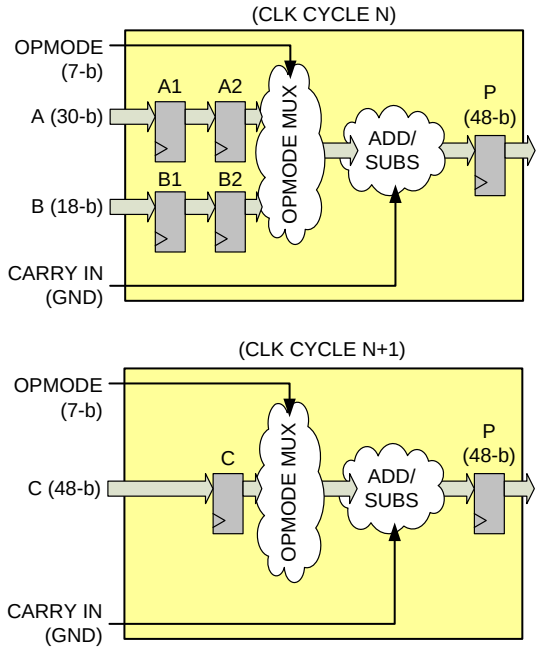


Figure 8.17. DSP48E register path for the addition operation dynamic tests.

Table 8.4. Addition Operation Static Register Components.

P_{A1Reg} (/0.5 day)	$P_{A2\ Reg}$ (/0.5 day)	$P_{B1\ Reg}$ (/0.5 day)	$P_{B2\ Reg}$ (/0.5 day)	$P_{C\ Reg}$ (/0.5 day)	$P_{P\ Reg}$ (/day)	Total Static (/day)
6.15e-6	6.15e-6	6.15e-6	6.15e-6	8.65E-6	1.73E-5	**5.05E-5**
					Total Dynamic (/day)	**1.57E-4**
					Static Component of Addition Operation:	**32%**

8.3.3.3 Accumulative Operations

Figure 8.18 illustrates the register and logic path of the accumulative operations used in the dynamic tests. The only register involved in the operation is the P register, which was incremented by the value Carry-In operator, which was tied to V_{CC}, or one. The DSP is capable of Accumulative operations utilizing the values in the A, B, C or Cascaded operators. To estimate the static component contribution in this case, the upset contribution of the P register is the only one used.

The static contribution is summed in Table 8.5. Thus at the frequencies tested, the static upset contribution to the susceptibility of the DSP addition operations are about half of all the dynamic SEE susceptibility.

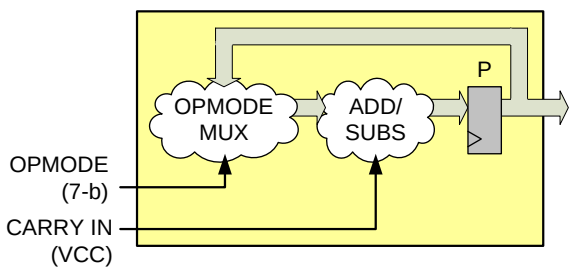


Figure 8.18. DSP48E register path for the accumulative operation dynamic tests.

Table 8.5. Accumulation Operation Static Register Components.

$P_{P\ Reg}$ (/day)	Total Static (/day)
1.73E-5	**1.73E-5**
Total Dynamic (/day)	**3.78E-5**
Static Component of Accumulative Operation:	**45%**

8.3.4 Impact Summary

Summarizing, the DSP static register susceptibility element of the DSP registers is only a fraction of the contribution to the overall sensitivity of the DSP48s. Since this is true even at the relatively low frequencies tested, it indicates that there's a significant contribution from single event transients that are frequency independent, and that are present on the clock tree implemented by the design. This hypothesis is corroborated from the MEUs measured and characterized (pg. 40).

Regardless of the source of the upsets that corrupt the DSPs, the overall response can be considered acceptable for many missions due to the relatively low frequency of occurrence, with a MTTF in the order

of decades in the worst of cases. In addition, DSPs are usually employed as through-put structures (i.e data in→ data out) with no other consequence than an erroneous output for the particular calculation affected. And for most applications, the resulting impact is similar to signal noise.

9. CONCLUSIONS

9.1 Functionality Characterized

The DSPs were tested for static register sensitivity, and for fundamental operation mode dynamic sensitivity. The tests were exercised with continuous altering data, in order to avoid the masking of errors due to inactive data patterns. Due to test setup limitations only low frequencies were employed, but estimates can be made to predict the dynamic response at higher frequencies. XRTC test reports by Boeing, which show the impact of SETs on high-frequency designs, can be used to extrapolate the impact of SETs at higher frequencies(2). Other features of the DSP48, such as ALU mode and SIMD modes, have not been verified with this test.

9.2 SEE Source Mechanisms

The source mechanisms for the upsets observed have been shown to be various. Since the DSP registers are un-hardened, they expected to have a significant contribution to the upset rate, but it has been shown that clock tree SET-induced upsets are also significant. SETs on the data and enable lines feeding the DSPs were expected to significant, but other XRTC experiments at low frequency have shown that this is not the case at the low frequencies tested (1) (2).

9.3 DSP48 Configuration Sensitivity

The configuration upset profile obtained for these tests (Figure 8.6, pg. 37) is considered typical for normal-incidence angles, where a high LET threshold is required for upset(9). The configuration upset cross-sections obtained is directly impacted by the implementation of the DSP48E, and since this data is obtained from the multiplication and addition tests, where all the input operator, output and multiplier registers are used, it should be representative of a typical DSP48E application.

Appendix A : Dynamic Tests Experimental Tables

A.1. DSP Accumulator Dynamic Tests Experimental Log Table.

RUN	FACILITIY	DUT SN	ENERGY (MeV)	ENERGY (MeV/u)	ION	DEGRADER	EFF. LET (MeV mg/cm2)	EFF. RANGE (um)	RUN TIME (S)	FLUX (p/cm2/s)	FLUENCE (p/cm2)	DSP	DATA VALID? (*)	DUT	TEST	FREQ (MHz)	TOTAL DOWN TIME (S)	CORRECTED FLUENCE (p/cm2)	ERROR COUNTS
156	0709-TAMU	A4438	269	24.8	Ar	3 @ 50.8°	**12.0**	256.8	982.32	1.02E+04	1.00E+07	0	YES	PRO	**ACC**	**12.50**	4.95E+01	9.50E+06	**13**
156	0709-TAMU	A4438	269	24.8	Ar	3 @ 50.8°	**12.0**	256.8	982.32	1.02E+04	1.00E+07	1	YES	PRO	**ACC**	**12.50**	3.24E+01	9.67E+06	**10**
156	0709-TAMU	A4438	269	24.8	Ar	3 @ 50.8°	**12.0**	256.8	982.32	1.02E+04	1.00E+07	2	YES	PRO	**ACC**	**12.50**	4.46E+01	9.55E+06	**11**
159	0709-TAMU	A4438	648	24.8	Ar	NONE	**7.3**	256.8	985.22	1.02E+04	1.00E+07	0	YES	PRO	**ACC**	**12.50**	3.28E+01	9.67E+06	**8**
159	0709-TAMU	A4438	648	24.8	Ar	NONE	**7.3**	256.8	985.22	1.02E+04	1.00E+07	1	YES	PRO	**ACC**	**12.50**	6.96E+01	9.29E+06	**20**
159	0709-TAMU	A4438	648	24.8	Ar	NONE	**7.3**	256.8	985.22	1.02E+04	1.00E+07	2	YES	PRO	**ACC**	**12.50**	3.28E+01	9.67E+06	**10**
185	0709-TAMU	A4438	482	24.8	Ne	NONE	**2.0**	561.7	696.86	2.87E+04	2.00E+07	0	YES	PRO	**ACC**	**12.50**	8.19E+00	1.98E+07	**4**
185	0709-TAMU	A4438	482	24.8	Ne	NONE	**2.0**	561.7	696.86	2.87E+04	2.00E+07	1	YES	PRO	**ACC**	**12.50**	1.84E-06	2.00E+07	**2**
185	0709-TAMU	A4438	482	24.8	Ne	NONE	**2.0**	561.7	696.86	2.87E+04	2.00E+07	2	YES	PRO	**ACC**	**12.50**	8.19E+00	1.98E+07	**3**
186	0709-TAMU	A4438	482	24.8	Ne	NONE	**2.0**	561.7	151.52	3.30E+05	5.00E+07	0	YES	PRO	**ACC**	**12.50**	2.87E+01	4.05E+07	**8**
186	0709-TAMU	A4438	482	24.8	Ne	NONE	**2.0**	561.7	151.52	3.30E+05	5.00E+07	1	YES	PRO	**ACC**	**12.50**	2.05E+01	4.32E+07	**5**
186	0709-TAMU	A4438	482	24.8	Ne	NONE	**2.0**	561.7	151.52	3.30E+05	5.00E+07	2	YES	PRO	**ACC**	**12.50**	2.43E+01	4.20E+07	**6**
187	0709-TAMU	A4438	482	24.8	Ne	NONE	**2.0**	561.7	153.37	3.26E+05	5.00E+07	0	YES	PRO	**ACC**	**12.50**	1.67E+01	4.45E+07	**6**
187	0709-TAMU	A4438	482	24.8	Ne	NONE	**2.0**	561.7	153.37	3.26E+05	5.00E+07	1	YES	PRO	**ACC**	**12.50**	1.92E+01	4.37E+07	**5**
187	0709-TAMU	A4438	482	24.8	Ne	NONE	**2.0**	561.7	153.37	3.26E+05	5.00E+07	2	YES	PRO	**ACC**	**12.50**	1.64E+01	4.47E+07	**5**
189	0709-TAMU	A4438	482	24.8	Ne	5 @ 0°	**4.3**	107.3	228.31	2.19E+05	5.00E+07	0	YES	PRO	**ACC**	**12.50**	4.43E+01	4.03E+07	**12**
189	0709-TAMU	A4438	482	24.8	Ne	5 @ 0°	**4.3**	107.3	228.31	2.19E+05	5.00E+07	1	YES	PRO	**ACC**	**12.50**	5.35E+01	3.83E+07	**17**
189	0709-TAMU	A4438	482	24.8	Ne	5 @ 0°	**4.3**	107.3	228.31	2.19E+05	5.00E+07	2	YES	PRO	**ACC**	**12.50**	5.59E+01	3.78E+07	**14**
190	0709-TAMU	A4438	482	24.8	Ne	5 @ 0°	**4.3**	107.3	229.36	2.18E+05	5.00E+07	0	YES	PRO	**ACC**	**12.50**	4.57E+01	4.00E+07	**13**
190	0709-TAMU	A4438	482	24.8	Ne	5 @ 0°	**4.3**	107.3	229.36	2.18E+05	5.00E+07	1	YES	PRO	**ACC**	**12.50**	3.82E+01	4.17E+07	**11**
190	0709-TAMU	A4438	482	24.8	Ne	5 @ 0°	**4.3**	107.3	229.36	2.18E+05	5.00E+07	2	YES	PRO	**ACC**	**12.50**	5.22E+01	3.86E+07	**13**
195	0709-TAMU	A4438	482	24.8	Ne	5 @ 31°	**6.6**	31.6	495.05	1.01E+05	5.00E+07	0	YES	PRO	**ACC**	**12.50**	9.93E+01	4.00E+07	**28**
195	0709-TAMU	A4438	482	24.8	Ne	5 @ 31°	**6.6**	31.6	495.05	1.01E+05	5.00E+07	1	YES	PRO	**ACC**	**12.50**	8.90E+01	4.10E+07	**28**
195	0709-TAMU	A4438	482	24.8	Ne	5 @ 31°	**6.6**	31.6	495.05	1.01E+05	5.00E+07	2	YES	PRO	**ACC**	**12.50**	9.78E+01	4.01E+07	**30**
94	1109-TAMU	A4438	721	24.8	Kr	NONE	**31.8**	89.0	7.77	5.40E+05	4.20E+06	0	NO	PRO	**ACC**	**6.25**	4.10E+00	1.99E+06	**0**
94	1109-TAMU	A4438	721	24.8	Kr	NONE	**31.8**	89.0	7.77	5.40E+05	4.20E+06	1	YES	PRO	**ACC**	**6.25**	1.64E+01	-4.65E+06	**4**
94	1109-TAMU	A4438	721	24.8	Kr	NONE	**31.8**	89.0	7.77	5.40E+05	4.20E+06	2	YES	PRO	**ACC**	**6.25**	2.05E+01	-6.86E+06	**5**
95	1109-TAMU	A4438	721	24.8	Kr	NONE	**31.8**	89.0	276.59	1.97E+04	5.44E+06	0	NO	PRO	**ACC**	**6.25**	4.15E+01	4.62E+06	**13**
95	1109-TAMU	A4438	721	24.8	Kr	NONE	**31.8**	89.0	276.59	1.97E+04	5.44E+06	1	NO	PRO	**ACC**	**6.25**	3.70E+01	4.71E+06	**0**
95	1109-TAMU	A4438	721	24.8	Kr	NONE	**31.8**	89.0	276.59	1.97E+04	5.44E+06	2	YES	PRO	**ACC**	**6.25**	4.89E+01	4.47E+06	**15**
96	1109-TAMU	A4438	721	24.8	Kr	NONE	**31.8**	89.0	1464.22	2.15E+04	3.15E+07	0	YES	PRO	**ACC**	**6.25**	2.11E+02	2.70E+07	**68**
96	1109-TAMU	A4438	721	24.8	Kr	NONE	**31.8**	89.0	1464.22	2.15E+04	3.15E+07	1	NO	PRO	**ACC**	**6.25**	1.22E+02	2.89E+07	**0**
96	1109-TAMU	A4438	721	24.8	Kr	NONE	**31.8**	89.0	1464.22	2.15E+04	3.15E+07	2	YES	PRO	**ACC**	**6.25**	1.78E+02	2.77E+07	**54**
152	1109-TAMU	A4438	639	24.8	Ar	NONE	**7.4**	250.0	507.84	1.16E+05	5.89E+07	0	YES	PRO	**ACC**	**6.25**	1.20E+02	4.50E+07	**49**
152	1109-TAMU	A4438	639	24.8	Ar	NONE	**7.4**	250.0	507.84	1.16E+05	5.89E+07	1	YES	PRO	**ACC**	**6.25**	1.06E+02	4.66E+07	**41**
152	1109-TAMU	A4438	639	24.8	Ar	NONE	**7.4**	250.0	507.84	1.16E+05	5.89E+07	2	YES	PRO	**ACC**	**6.25**	8.43E+01	4.91E+07	**37**
153	1109-TAMU	A4438	639	24.8	Ar	3 @ 57°	**15.0**	250.0	220.41	1.07E+05	2.35E+07	0	YES	PRO	**ACC**	**6.25**	4.81E+01	1.84E+07	**25**
153	1109-TAMU	A4438	639	24.8	Ar	3 @ 57°	**15.0**	250.0	220.41	1.07E+05	2.35E+07	1	YES	PRO	**ACC**	**6.25**	4.39E+01	1.88E+07	**29**
153	1109-TAMU	A4438	639	24.8	Ar	3 @ 57°	**15.0**	250.0	220.41	1.07E+05	2.35E+07	2	YES	PRO	**ACC**	**6.25**	4.41E+01	1.88E+07	**25**
200	1109-TAMU	A4438	145	24.8	Ne	5 @ 0°	**4.4**	100.4	2288.90	2.20E+05	5.03E+08	0	YES	PRO	**ACC**	**6.25**	4.50E+02	4.04E+08	**145**
200	1109-TAMU	A4438	145	24.8	Ne	5 @ 0°	**4.4**	100.4	2288.90	2.20E+05	5.03E+08	1	YES	PRO	**ACC**	**6.25**	3.73E+02	4.21E+08	**123**
200	1109-TAMU	A4438	145	24.8	Ne	5 @ 0°	**4.4**	100.4	2288.90	2.20E+05	5.03E+08	2	YES	PRO	**ACC**	**6.25**	4.53E+02	4.04E+08	**139**

(*) Data from certain runs for particular DSPs was omitted if oscillatory events overflowed event buffers

A.2. DSP Addition Dynamic Tests Experimental Log Table.

RUN	FACILITIY	DUT SN	ENERGY (MeV)	ENERGY (MeV/u)	ION	DEGRADER	EFF. LET (MeV mg/cm2)	EFF. RANGE (um	RUN TIME (S)	FLUX (p/cm2/s)	FLUENCE (p/cm2)	DSP	DATA VALID? (*)	DUT	TEST	FREQ (MHz)	TOTAL DOWN TIME (S)	CORRECTED FLUENCE (p/cm2)	ERROR COUNTS
63	0509-LBNL	PCB SN 02	-	16	Kr	NONE	**25.0**	-	240.56	4.16E+04	1.00E+07	0	YES	PRO	**ADD**	**25.00**	0.00E+00	1.00E+07	**0**
63	0509-LBNL	PCB SN 02	-	16	Kr	NONE	**25.0**	-	240.56	4.16E+04	1.00E+07	1	YES	PRO	**ADD**	**25.00**	2.24E-06	1.00E+07	**2**
63	0509-LBNL	PCB SN 02	-	16	Kr	NONE	**25.0**	-	240.56	4.16E+04	1.00E+07	2	NO	PRO	**ADD**	**25.00**	0.00E+00	1.00E+07	**0**
64	0509-LBNL	PCB SN 02	-	16	Kr	NONE	**25.0**	-	1030.49	9.70E+04	1.00E+08	0	NO	PRO	**ADD**	**25.00**	1.24E-06	1.00E+08	**0**
64	0509-LBNL	PCB SN 02	-	16	Kr	NONE	**25.0**	-	1030.49	9.70E+04	1.00E+08	1	YES	PRO	**ADD**	**25.00**	1.76E+00	9.98E+07	**20**
64	0509-LBNL	PCB SN 02	-	16	Kr	NONE	**25.0**	-	1030.49	9.70E+04	1.00E+08	2	NO	PRO	**ADD**	**25.00**	0.00E+00	1.00E+08	**0**
155	0709-TAMU	A4438	269	24.8	Ar	3 @ 50.8°	**12.0**	256.8	850.94	1.17E+04	9.99E+06	0	YES	PRO	**ADD**	**12.50**	1.76E-05	9.99E+06	**29**
155	0709-TAMU	A4438	269	24.8	Ar	3 @ 50.8°	**12.0**	256.8	850.94	1.17E+04	9.99E+06	1	YES	PRO	**ADD**	**12.50**	1.63E-05	9.99E+06	**33**
155	0709-TAMU	A4438	269	24.8	Ar	3 @ 50.8°	**12.0**	256.8	850.94	1.17E+04	9.99E+06	2	YES	PRO	**ADD**	**12.50**	1.74E-05	9.99E+06	**32**
158	0709-TAMU	A4438	648	24.8	Ar	NONE	**7.3**	256.8	1106.07	9.04E+03	1.00E+07	0	YES	PRO	**ADD**	**12.50**	1.48E-05	1.00E+07	**23**
158	0709-TAMU	A4438	648	24.8	Ar	NONE	**7.3**	256.8	1106.07	9.04E+03	1.00E+07	1	YES	PRO	**ADD**	**12.50**	7.72E-06	1.00E+07	**13**
158	0709-TAMU	A4438	648	24.8	Ar	NONE	**7.3**	256.8	1106.07	9.04E+03	1.00E+07	2	YES	PRO	**ADD**	**12.50**	1.27E-05	1.00E+07	**17**
183	0709-TAMU	A4438	482	24.8	Ne	NONE	**2.0**	561.7	396.83	1.26E+05	5.00E+07	0	YES	PRO	**ADD**	**12.50**	1.38E-05	5.00E+07	**26**
183	0709-TAMU	A4438	482	24.8	Ne	NONE	**2.0**	561.7	396.83	1.26E+05	5.00E+07	1	YES	PRO	**ADD**	**12.50**	8.72E-06	5.00E+07	**18**
183	0709-TAMU	A4438	482	24.8	Ne	NONE	**2.0**	561.7	396.83	1.26E+05	5.00E+07	2	YES	PRO	**ADD**	**12.50**	1.08E-05	5.00E+07	**16**
184	0709-TAMU	A4438	482	24.8	Ne	NONE	**2.0**	561.7	344.14	1.45E+05	4.99E+07	0	YES	PRO	**ADD**	**12.50**	1.24E-05	4.99E+07	**18**
184	0709-TAMU	A4438	482	24.8	Ne	NONE	**2.0**	561.7	344.14	1.45E+05	4.99E+07	1	YES	PRO	**ADD**	**12.50**	1.03E-05	4.99E+07	**17**
184	0709-TAMU	A4438	482	24.8	Ne	NONE	**2.0**	561.7	344.14	1.45E+05	4.99E+07	2	YES	PRO	**ADD**	**12.50**	1.39E-05	4.99E+07	**24**
192	0709-TAMU	A4438	482	24.8	Ne	5 @ 0°	**4.3**	107.3	249.50	2.00E+05	4.99E+07	0	YES	PRO	**ADD**	**12.50**	3.76E-01	4.98E+07	**42**
192	0709-TAMU	A4438	482	24.8	Ne	5 @ 0°	**4.3**	107.3	249.50	2.00E+05	4.99E+07	1	YES	PRO	**ADD**	**12.50**	3.76E-01	4.98E+07	**44**
192	0709-TAMU	A4438	482	24.8	Ne	5 @ 0°	**4.3**	107.3	249.50	2.00E+05	4.99E+07	2	YES	PRO	**ADD**	**12.50**	3.76E-01	4.98E+07	**46**
193	0709-TAMU	A4438	482	24.8	Ne	5 @ 31°	**6.6**	31.6	485.44	1.03E+05	5.00E+07	0	YES	PRO	**ADD**	**12.50**	3.68E-01	5.00E+07	**73**
193	0709-TAMU	A4438	482	24.8	Ne	5 @ 31°	**6.6**	31.6	485.44	1.03E+05	5.00E+07	1	YES	PRO	**ADD**	**12.50**	3.68E-01	5.00E+07	**61**
193	0709-TAMU	A4438	482	24.8	Ne	5 @ 31°	**6.6**	31.6	485.44	1.03E+05	5.00E+07	2	YES	PRO	**ADD**	**12.50**	3.68E-01	5.00E+07	**53**
89	1109-TAMU	A4438	721	24.8	Kr	NONE	**31.8**	89.0	19.01	1.30E+05	2.47E+06	0	YES	PRO	**ADD**	**6.25**	5.48E-06	2.47E+06	**10**
89	1109-TAMU	A4438	721	24.8	Kr	NONE	**31.8**	89.0	19.01	1.30E+05	2.47E+06	1	YES	PRO	**ADD**	**6.25**	7.20E-06	2.47E+06	**11**
89	1109-TAMU	A4438	721	24.8	Kr	NONE	**31.8**	89.0	19.01	1.30E+05	2.47E+06	2	YES	PRO	**ADD**	**6.25**	1.03E-05	2.47E+06	**15**
90	1109-TAMU	A4438	721	24.8	Kr	NONE	**31.8**	89.0	6.98	1.44E+05	1.01E+06	0	YES	PRO	**ADD**	**6.25**	6.72E-06	1.01E+06	**9**
90	1109-TAMU	A4438	721	24.8	Kr	NONE	**31.8**	89.0	6.98	1.44E+05	1.01E+06	1	YES	PRO	**ADD**	**6.25**	6.88E-06	1.01E+06	**9**
90	1109-TAMU	A4438	721	24.8	Kr	NONE	**31.8**	89.0	6.98	1.44E+05	1.01E+06	2	YES	PRO	**ADD**	**6.25**	3.60E-06	1.01E+06	**7**
91	1109-TAMU	A4438	721	24.8	Kr	NONE	**31.8**	89.0	463.11	1.51E+05	6.99E+07	0	YES	PRO	**ADD**	**6.25**	1.25E+01	6.80E+07	**413**
91	1109-TAMU	A4438	721	24.8	Kr	NONE	**31.8**	89.0	463.11	1.51E+05	6.99E+07	1	YES	PRO	**ADD**	**6.25**	1.39E+01	6.78E+07	**471**
91	1109-TAMU	A4438	721	24.8	Kr	NONE	**31.8**	89.0	463.11	1.51E+05	6.99E+07	2	YES	PRO	**ADD**	**6.25**	1.23E+01	6.81E+07	**421**
92	1109-TAMU	A4438	721	24.8	Kr	NONE	**31.8**	89.0	583.52	4.96E+04	2.90E+07	0	YES	PRO	**ADD**	**6.25**	3.98E+00	2.88E+07	**170**
92	1109-TAMU	A4438	721	24.8	Kr	NONE	**31.8**	89.0	583.52	4.96E+04	2.90E+07	1	YES	PRO	**ADD**	**6.25**	6.73E+00	2.86E+07	**208**
92	1109-TAMU	A4438	721	24.8	Kr	NONE	**31.8**	89.0	583.52	4.96E+04	2.90E+07	2	YES	PRO	**ADD**	**6.25**	3.24E+00	2.88E+07	**183**
99	1109-TAMU	A4438	365	24.8	Kr	1 @ 45°	**38.0**	44.7	1259.93	1.99E+04	2.51E+07	0	YES	PRO	**ADD**	**6.25**	8.37E+00	2.49E+07	**213**
99	1109-TAMU	A4438	365	24.8	Kr	1 @ 45°	**38.0**	44.7	1259.93	1.99E+04	2.51E+07	1	YES	PRO	**ADD**	**6.25**	8.76E+00	2.49E+07	**238**
99	1109-TAMU	A4438	365	24.8	Kr	1 @ 45°	**38.0**	44.7	1259.93	1.99E+04	2.51E+07	2	YES	PRO	**ADD**	**6.25**	6.29E+00	2.49E+07	**236**
149	1109-TAMU	A4438	639	24.8	Ar	NONE	**7.4**	250.0	521.48	1.14E+05	5.92E+07	0	YES	PRO	**ADD**	**6.25**	4.45E+00	5.87E+07	**100**
149	1109-TAMU	A4438	639	24.8	Ar	NONE	**7.4**	250.0	521.48	1.14E+05	5.92E+07	1	YES	PRO	**ADD**	**6.25**	4.45E+00	5.87E+07	**114**
149	1109-TAMU	A4438	639	24.8	Ar	NONE	**7.4**	250.0	521.48	1.14E+05	5.92E+07	2	YES	PRO	**ADD**	**6.25**	4.45E+00	5.87E+07	**122**
195	1109-TAMU	A4438	486	24.8	Ne	NONE	**2.1**	554.8	1128.43	3.10E+05	3.50E+08	0	YES	PRO	**ADD**	**6.25**	1.47E+00	3.49E+08	**149**
195	1109-TAMU	A4438	486	24.8	Ne	NONE	**2.1**	554.8	1128.43	3.10E+05	3.50E+08	1	YES	PRO	**ADD**	**6.25**	1.47E+00	3.49E+08	**169**
195	1109-TAMU	A4438	486	24.8	Ne	NONE	**2.1**	554.8	1128.43	3.10E+05	3.50E+08	2	YES	PRO	**ADD**	**6.25**	1.47E+00	3.49E+08	**154**
198	1109-TAMU	A4438	145	24.8	Ne	5 @ 0°	**4.4**	100.4	737.18	2.20E+05	1.62E+08	0	YES	PRO	**ADD**	**6.25**	7.75E-01	1.62E+08	**174**
198	1109-TAMU	A4438	145	24.8	Ne	5 @ 0°	**4.4**	100.4	737.18	2.20E+05	1.62E+08	1	YES	PRO	**ADD**	**6.25**	7.75E-01	1.62E+08	**160**
198	1109-TAMU	A4438	145	24.8	Ne	5 @ 0°	**4.4**	100.4	737.18	2.20E+05	1.62E+08	2	YES	PRO	**ADD**	**6.25**	7.75E-01	1.62E+08	**153**

(*) Data from certain runs for particular DSPs was omitted if oscillatory events overflowed event buffers

A.3. DSP Multiplication Dynamic Tests Experimental Log Table.

RUN	FACILITIY	DUT SN	ENERGY (MeV)	ENERGY (MeV/u)	ION	DEGRADER	EFF. LET (MeV mg/cm2)	EFF. RANGE (um	RUN TIME (S)	FLUX (p/cm2/s)	FLUENCE (p/cm2)	DSP	DATA VALID? (*)	DUT	TEST	FREQ (MHz)	TOTAL DOWN TIME (S)	CORRECTED FLUENCE (p/cm2)	ERROR COUNTS
65	0509-LBNL	PCB SN 02	-	16	Kr	NONE	**25.0**	-	861.50	9.74E+04	8.39E+07	0	NO	PRO	**MUL**	**25.00**	0.00E+00	8.39E+07	**0**
65	0509-LBNL	PCB SN 02	-	16	Kr	NONE	**25.0**	-	861.50	9.74E+04	8.39E+07	1	YES	PRO	**MUL**	**25.00**	1.17E+00	8.38E+07	**20**
65	0509-LBNL	PCB SN 02	-	16	Kr	NONE	**25.0**	-	861.50	9.74E+04	8.39E+07	2	NO	PRO	**MUL**	**25.00**	0.00E+00	8.39E+07	**0**
70	0509-LBNL	PCB SN 02	-	16	Cu	NONE	**16.5**	-	444.35	4.50E+05	2.00E+08	0	YES	PRO	**MUL**	**25.00**	2.44E-06	2.00E+08	**5**
70	0509-LBNL	PCB SN 02	-	16	Cu	NONE	**16.5**	-	444.35	4.50E+05	2.00E+08	1	YES	PRO	**MUL**	**25.00**	3.30E-01	2.00E+08	**32**
70	0509-LBNL	PCB SN 02	-	16	Cu	NONE	**16.5**	-	444.35	4.50E+05	2.00E+08	2	YES	PRO	**MUL**	**25.00**	1.60E-07	2.00E+08	**4**
71	0509-LBNL	PCB SN 02	-	16	Cu	NONE	**16.5**	-	434.64	4.60E+05	2.00E+08	0	YES	PACR	**MUL**	**25.00**	3.76E-01	2.00E+08	**4**
71	0509-LBNL	PCB SN 02	-	16	Cu	NONE	**16.5**	-	434.64	4.60E+05	2.00E+08	1	YES	PACR	**MUL**	**25.00**	7.02E-01	2.00E+08	**28**
71	0509-LBNL	PCB SN 02	-	16	Cu	NONE	**16.5**	-	434.64	4.60E+05	2.00E+08	2	YES	PACR	**MUL**	**25.00**	3.76E-01	2.00E+08	**14**
154	0709-TAMU	A4438	269	24.8	Ar	3 @ 50.8°	**12.0**	256.8	806.05	1.24E+04	1.00E+07	0	YES	PRO	**MUL**	**12.50**	1.24E-05	9.99E+06	**27**
154	0709-TAMU	A4438	269	24.8	Ar	3 @ 50.8°	**12.0**	256.8	806.05	1.24E+04	1.00E+07	1	YES	PRO	**MUL**	**12.50**	6.96E-06	9.99E+06	**31**
154	0709-TAMU	A4438	269	24.8	Ar	3 @ 50.8°	**12.0**	256.8	806.05	1.24E+04	1.00E+07	2	YES	PRO	**MUL**	**12.50**	1.55E-05	9.99E+06	**39**
157	0709-TAMU	A4438	648	24.8	Ar	NONE	**7.3**	256.8	1121.52	8.91E+03	1.00E+07	0	YES	PRO	**MUL**	**12.50**	3.68E-01	9.99E+06	**30**
157	0709-TAMU	A4438	648	24.8	Ar	NONE	**7.3**	256.8	1121.52	8.91E+03	1.00E+07	1	YES	PRO	**MUL**	**12.50**	3.68E-01	9.99E+06	**26**
157	0709-TAMU	A4438	648	24.8	Ar	NONE	**7.3**	256.8	1121.52	8.91E+03	1.00E+07	2	YES	PRO	**MUL**	**12.50**	3.68E-01	9.99E+06	**22**
180	0709-TAMU	A4438	482	24.8	Ne	NONE	**2.0**	561.7	152.44	1.64E+04	2.50E+06	0	YES	PRO	**MUL**	**12.50**	1.60E-07	2.50E+06	**2**
180	0709-TAMU	A4438	482	24.8	Ne	NONE	**2.0**	561.7	152.44	1.64E+04	2.50E+06	1	YES	PRO	**MUL**	**12.50**	8.00E-08	2.50E+06	1
180	0709-TAMU	A4438	482	24.8	Ne	NONE	**2.0**	561.7	152.44	1.64E+04	2.50E+06	2	YES	PRO	**MUL**	**12.50**	8.40E-07	2.50E+06	**3**
182	0709-TAMU	A4438	482	24.8	Ne	NONE	**2.0**	561.7	719.42	1.39E+05	1.00E+08	0	YES	PRO	**MUL**	**12.50**	2.74E-05	1.00E+08	**62**
182	0709-TAMU	A4438	482	24.8	Ne	NONE	**2.0**	561.7	719.42	1.39E+05	1.00E+08	1	YES	PRO	**MUL**	**12.50**	1.62E-05	1.00E+08	**44**
182	0709-TAMU	A4438	482	24.8	Ne	NONE	**2.0**	561.7	719.42	1.39E+05	1.00E+08	2	YES	PRO	**MUL**	**12.50**	2.78E-05	1.00E+08	**50**
191	0709-TAMU	A4438	482	24.8	Ne	5 @ 0°	**4.3**	107.3	238.57	2.10E+05	5.01E+07	0	YES	PRO	**MUL**	**12.50**	3.76E-01	5.00E+07	**60**
191	0709-TAMU	A4438	482	24.8	Ne	5 @ 0°	**4.3**	107.3	238.57	2.10E+05	5.01E+07	1	YES	PRO	**MUL**	**12.50**	3.76E-01	5.00E+07	**76**
191	0709-TAMU	A4438	482	24.8	Ne	5 @ 0°	**4.3**	107.3	238.57	2.10E+05	5.01E+07	2	YES	PRO	**MUL**	**12.50**	3.76E-01	5.00E+07	**58**
194	0709-TAMU	A4438	482	24.8	Ne	5 @ 31°	**6.6**	31.6	495.05	1.01E+05	5.00E+07	0	YES	PRO	**MUL**	**12.50**	4.76E-05	5.00E+07	**91**
194	0709-TAMU	A4438	482	24.8	Ne	5 @ 31°	**6.6**	31.6	495.05	1.01E+05	5.00E+07	1	YES	PRO	**MUL**	**12.50**	3.82E-05	5.00E+07	**95**
194	0709-TAMU	A4438	482	24.8	Ne	5 @ 31°	**6.6**	31.6	495.05	1.01E+05	5.00E+07	2	YES	PRO	**MUL**	**12.50**	3.91E-05	5.00E+07	**95**
93	1109-TAMU	A4438	721	24.8	Kr	NONE	**31.8**	89.0	472.35	5.30E+04	2.50E+07	0	NO	PRO	**MUL**	**6.25**	1.12E+00	2.50E+07	**478**
93	1109-TAMU	A4438	721	24.8	Kr	NONE	**31.8**	89.0	472.35	5.30E+04	2.50E+07	1	YES	PRO	**MUL**	**6.25**	3.84E+00	2.48E+07	**206**
93	1109-TAMU	A4438	721	24.8	Kr	NONE	**31.8**	89.0	472.35	5.30E+04	2.50E+07	2	NO	PRO	**MUL**	**6.25**	7.53E-01	2.50E+07	**451**
98	1109-TAMU	A4438	365	24.8	Kr	1 @ 45°	**38.0**	44.7	2177.02	1.84E+04	4.00E+07	0	YES	PRO	**MUL**	**6.25**	1.44E+01	3.97E+07	**422**
98	1109-TAMU	A4438	365	24.8	Kr	1 @ 45°	**38.0**	44.7	2177.02	1.84E+04	4.00E+07	1	YES	PRO	**MUL**	**6.25**	1.41E+01	3.97E+07	**507**
98	1109-TAMU	A4438	365	24.8	Kr	1 @ 45°	**38.0**	44.7	2177.02	1.84E+04	4.00E+07	2	YES	PRO	**MUL**	**6.25**	9.36E+00	3.98E+07	**410**
151	1109-TAMU	A4438	639	24.8	Ar	NONE	**7.4**	250.0	422.26	1.21E+05	5.12E+07	0	YES	PRO	**MUL**	**6.25**	1.76E+00	5.10E+07	**99**
151	1109-TAMU	A4438	639	24.8	Ar	NONE	**7.4**	250.0	422.26	1.21E+05	5.12E+07	1	YES	PRO	**MUL**	**6.25**	1.76E+00	5.10E+07	**114**
151	1109-TAMU	A4438	639	24.8	Ar	NONE	**7.4**	250.0	422.26	1.21E+05	5.12E+07	2	YES	PRO	**MUL**	**6.25**	1.76E+00	5.10E+07	**103**
154	1109-TAMU	A4438	639	24.8	Ar	3 @ 57°	**15.0**	250.0	217.33	1.06E+05	2.31E+07	0	YES	PRO	**MUL**	**6.25**	1.10E+00	2.30E+07	**99**
154	1109-TAMU	A4438	639	24.8	Ar	3 @ 57°	**15.0**	250.0	217.33	1.06E+05	2.31E+07	1	YES	PRO	**MUL**	**6.25**	1.10E+00	2.30E+07	**88**
154	1109-TAMU	A4438	639	24.8	Ar	3 @ 57°	**15.0**	250.0	217.33	1.06E+05	2.31E+07	2	YES	PRO	**MUL**	**6.25**	1.10E+00	2.30E+07	**93**
196	1109-TAMU	A4438	486	24.8	Ne	NONE	**2.1**	554.8	810.90	3.08E+05	2.50E+08	0	YES	PRO	**MUL**	**6.25**	3.64E-01	2.50E+08	**151**
196	1109-TAMU	A4438	486	24.8	Ne	NONE	**2.1**	554.8	810.90	3.08E+05	2.50E+08	1	YES	PRO	**MUL**	**6.25**	3.64E-01	2.50E+08	**139**
196	1109-TAMU	A4438	486	24.8	Ne	NONE	**2.1**	554.8	810.90	3.08E+05	2.50E+08	2	YES	PRO	**MUL**	**6.25**	3.64E-01	2.50E+08	**120**
199	1109-TAMU	A4438	145	24.8	Ne	5 @ 0°	**4.4**	100.4	678.98	2.25E+05	1.53E+08	0	YES	PRO	**MUL**	**6.25**	7.29E-01	1.52E+08	**142**
199	1109-TAMU	A4438	145	24.8	Ne	5 @ 0°	**4.4**	100.4	678.98	2.25E+05	1.53E+08	1	YES	PRO	**MUL**	**6.25**	7.29E-01	1.52E+08	**203**
199	1109-TAMU	A4438	145	24.8	Ne	5 @ 0°	**4.4**	100.4	678.98	2.25E+05	1.53E+08	2	YES	PRO	**MUL**	**6.25**	7.29E-01	1.52E+08	**155**

(*) Data from certain runs for particular DSPs was omitted if oscillatory events overflowed event buffers

Appendix B : Event Duration Category Breakdown

B.1. Accumulation Tests

RUN	EFF. LET (MeV-cm2/mg)	DSP	DATA VALID? (*)	DUT	TEST	FREQ (MHz)	CORRECTED FLUENCE (p/cm2)	CAT1 SEU	CAT2 SEU	CAT3 SEU	CAT4 SEU	PERSIST SEU	CFG SEU	SEFI COUNTS
156	12.0	0	YES	PRO	ACC	12.50	9.50E+06	**0**	**0**	**1**	**12**	12	n/a	1
156	12.0	1	YES	PRO	ACC	12.50	9.67E+06	**0**	**1**	**1**	**8**	8	n/a	1
156	12.0	2	YES	PRO	ACC	12.50	9.55E+06	**0**	**0**	**0**	**11**	10	n/a	1
159	7.3	0	YES	PRO	ACC	12.50	9.67E+06	**0**	**0**	**0**	**8**	8	n/a	0
159	7.3	1	YES	PRO	ACC	12.50	9.29E+06	**2**	**1**	**0**	**17**	17	n/a	0
159	7.3	2	YES	PRO	ACC	12.50	9.67E+06	**0**	**2**	**0**	**8**	8	n/a	0
185	2.0	0	YES	PRO	ACC	12.50	1.98E+07	**0**	**0**	**2**	**2**	4	n/a	0
185	2.0	1	YES	PRO	ACC	12.50	2.00E+07	**0**	**2**	**0**	**0**	0	n/a	0
185	2.0	2	YES	PRO	ACC	12.50	1.98E+07	**0**	**1**	**0**	**2**	2	n/a	0
186	2.0	0	YES	PRO	ACC	12.50	4.05E+07	**0**	**1**	**0**	**7**	7	n/a	0
186	2.0	1	YES	PRO	ACC	12.50	4.32E+07	**0**	**0**	**0**	**5**	5	n/a	0
186	2.0	2	YES	PRO	ACC	12.50	4.20E+07	**0**	**0**	**0**	**6**	6	n/a	0
187	2.0	0	YES	PRO	ACC	12.50	4.45E+07	**1**	**0**	**1**	**4**	5	n/a	0
187	2.0	1	YES	PRO	ACC	12.50	4.37E+07	**0**	**0**	**0**	**5**	5	n/a	0
187	2.0	2	YES	PRO	ACC	12.50	4.47E+07	**0**	**1**	**0**	**4**	4	n/a	0
189	4.3	0	YES	PRO	ACC	12.50	4.03E+07	**0**	**0**	**0**	**12**	12	n/a	0
189	4.3	1	YES	PRO	ACC	12.50	3.83E+07	**1**	**2**	**1**	**13**	14	n/a	0
189	4.3	2	YES	PRO	ACC	12.50	3.78E+07	**0**	**0**	**0**	**14**	14	n/a	0
190	4.3	0	YES	PRO	ACC	12.50	4.00E+07	**1**	**0**	**0**	**12**	12	n/a	0
190	4.3	1	YES	PRO	ACC	12.50	4.17E+07	**0**	**1**	**0**	**10**	10	n/a	0
190	4.3	2	YES	PRO	ACC	12.50	3.86E+07	**0**	**0**	**0**	**13**	13	n/a	0
195	6.6	0	YES	PRO	ACC	12.50	4.00E+07	**0**	**2**	**1**	**25**	26	n/a	0
195	6.6	1	YES	PRO	ACC	12.50	4.10E+07	**2**	**1**	**2**	**23**	25	n/a	0
195	6.6	2	YES	PRO	ACC	12.50	4.01E+07	**1**	**4**	**1**	**24**	25	n/a	0
94	31.8	0	NO	PRO	ACC	6.25	1.99E+06	**0**	**0**	**0**	**0**	0	n/a	0
94	31.8	1	YES	PRO	ACC	6.25	-4.65E+06	**0**	**0**	**0**	**4**	4	n/a	0
94	31.8	2	YES	PRO	ACC	6.25	-6.86E+06	**0**	**0**	**0**	**5**	5	n/a	0
95	31.8	0	NO	PRO	ACC	6.25	4.62E+06	**0**	**0**	**1**	**12**	13	n/a	0
95	31.8	1	NO	PRO	ACC	6.25	4.71E+06	**0**	**0**	**0**	**0**	0	n/a	0
95	31.8	2	YES	PRO	ACC	6.25	4.47E+06	**0**	**0**	**2**	**13**	15	n/a	0
96	31.8	0	YES	PRO	ACC	6.25	2.70E+07	**2**	**1**	**4**	**61**	55	n/a	10
96	31.8	1	NO	PRO	ACC	6.25	2.89E+07	**0**	**0**	**0**	**0**	-10	n/a	10
96	31.8	2	YES	PRO	ACC	6.25	2.77E+07	**0**	**2**	**2**	**50**	42	n/a	10
152	7.4	0	YES	PRO	ACC	6.25	4.50E+07	**0**	**2**	**3**	**44**	44	n/a	3
152	7.4	1	YES	PRO	ACC	6.25	4.66E+07	**2**	**2**	**0**	**37**	34	n/a	3
152	7.4	2	YES	PRO	ACC	6.25	4.91E+07	**0**	**1**	**3**	**33**	33	n/a	3
153	15.0	0	YES	PRO	ACC	6.25	1.84E+07	**0**	**0**	**2**	**23**	21	n/a	4
153	15.0	1	YES	PRO	ACC	6.25	1.88E+07	**0**	**2**	**5**	**22**	23	n/a	4
153	15.0	2	YES	PRO	ACC	6.25	1.88E+07	**0**	**1**	**3**	**21**	20	n/a	4
200	4.4	0	YES	PRO	ACC	6.25	4.04E+08	**5**	**15**	**3**	**122**	121	n/a	4
200	4.4	1	YES	PRO	ACC	6.25	4.21E+08	**4**	**17**	**1**	**101**	98	n/a	4
200	4.4	2	YES	PRO	ACC	6.25	4.04E+08	**3**	**13**	**0**	**123**	119	n/a	4

B.2. Addition Tests.

RUN	EFF. LET (MeV-cm2/mg)	DSP	DATA VALID? (*)	DUT	TEST	FREQ (MHz)	CORRECTED FLUENCE (p/cm2)	CAT1 SEU	CAT2 SEU	CAT3 SEU	CAT4 SEU	PERSIST SEU	CFG SEU	SEFI COUNTS
63	25.0	0	YES	PRO	ADD	25.00	1.00E+07	0	0	0	0	n/a	0	0
63	25.0	1	YES	PRO	ADD	25.00	1.00E+07	0	2	0	0	n/a	0	0
63	25.0	2	NO	PRO	ADD	25.00	1.00E+07	0	0	0	0	n/a	0	0
64	25.0	0	NO	PRO	ADD	25.00	1.00E+08	0	0	0	0	n/a	0	0
64	25.0	1	YES	PRO	ADD	25.00	9.98E+07	2	15	2	1	n/a	3	0
64	25.0	2	NO	PRO	ADD	25.00	1.00E+08	0	0	0	0	n/a	0	0
155	12.0	0	YES	PRO	ADD	12.50	9.99E+06	16	13	0	0	n/a	0	0
155	12.0	1	YES	PRO	ADD	12.50	9.99E+06	22	11	0	0	n/a	0	0
155	12.0	2	YES	PRO	ADD	12.50	9.99E+06	19	13	0	0	n/a	0	0
158	7.3	0	YES	PRO	ADD	12.50	1.00E+07	13	10	0	0	n/a	0	0
158	7.3	1	YES	PRO	ADD	12.50	1.00E+07	8	5	0	0	n/a	0	0
158	7.3	2	YES	PRO	ADD	12.50	1.00E+07	8	9	0	0	n/a	0	0
183	2.0	0	YES	PRO	ADD	12.50	5.00E+07	12	14	0	0	n/a	0	0
183	2.0	1	YES	PRO	ADD	12.50	5.00E+07	10	8	0	0	n/a	0	0
183	2.0	2	YES	PRO	ADD	12.50	5.00E+07	6	10	0	0	n/a	0	0
184	2.0	0	YES	PRO	ADD	12.50	4.99E+07	7	11	0	0	n/a	0	0
184	2.0	1	YES	PRO	ADD	12.50	4.99E+07	8	9	0	0	n/a	0	0
184	2.0	2	YES	PRO	ADD	12.50	4.99E+07	11	13	0	0	n/a	0	0
192	4.3	0	YES	PRO	ADD	12.50	4.98E+07	17	24	1	0	n/a	0	1
192	4.3	1	YES	PRO	ADD	12.50	4.98E+07	22	21	1	0	n/a	0	1
192	4.3	2	YES	PRO	ADD	12.50	4.98E+07	23	22	1	0	n/a	0	1
193	6.6	0	YES	PRO	ADD	12.50	5.00E+07	35	37	1	0	n/a	0	1
193	6.6	1	YES	PRO	ADD	12.50	5.00E+07	34	26	1	0	n/a	0	1
193	6.6	2	YES	PRO	ADD	12.50	5.00E+07	26	26	1	0	n/a	0	1
89	31.8	0	YES	PRO	ADD	6.25	2.47E+06	7	3	0	0	n/a	0	0
89	31.8	1	YES	PRO	ADD	6.25	2.47E+06	7	4	0	0	n/a	0	0
89	31.8	2	YES	PRO	ADD	6.25	2.47E+06	9	6	0	0	n/a	0	0
90	31.8	0	YES	PRO	ADD	6.25	1.01E+06	5	4	0	0	n/a	0	0
90	31.8	1	YES	PRO	ADD	6.25	1.01E+06	5	4	0	0	n/a	0	0
90	31.8	2	YES	PRO	ADD	6.25	1.01E+06	5	2	0	0	n/a	0	0
91	31.8	0	YES	PRO	ADD	6.25	6.80E+07	240	146	26	1	n/a	9	18
91	31.8	1	YES	PRO	ADD	6.25	6.78E+07	293	149	28	1	n/a	11	18
91	31.8	2	YES	PRO	ADD	6.25	6.81E+07	252	144	23	2	n/a	7	18
92	31.8	0	YES	PRO	ADD	6.25	2.88E+07	100	61	8	1	n/a	0	9
92	31.8	1	YES	PRO	ADD	6.25	2.86E+07	127	67	10	4	n/a	5	9
92	31.8	2	YES	PRO	ADD	6.25	2.88E+07	111	65	6	1	n/a	0	7
99	38.0	0	YES	PRO	ADD	6.25	2.49E+07	108	83	21	1	n/a	8	14
99	38.0	1	YES	PRO	ADD	6.25	2.49E+07	131	83	22	2	n/a	10	14
99	38.0	2	YES	PRO	ADD	6.25	2.49E+07	138	79	19	0	n/a	5	14
149	7.4	0	YES	PRO	ADD	6.25	5.87E+07	61	37	1	1	n/a	0	2
149	7.4	1	YES	PRO	ADD	6.25	5.87E+07	56	56	1	1	n/a	0	2
149	7.4	2	YES	PRO	ADD	6.25	5.87E+07	69	51	1	1	n/a	0	2
195	2.1	0	YES	PRO	ADD	6.25	3.49E+08	62	83	4	0	n/a	0	4
195	2.1	1	YES	PRO	ADD	6.25	3.49E+08	87	78	4	0	n/a	0	4
195	2.1	2	YES	PRO	ADD	6.25	3.49E+08	60	90	4	0	n/a	0	4
198	4.4	0	YES	PRO	ADD	6.25	1.62E+08	94	78	2	0	n/a	0	2
198	4.4	1	YES	PRO	ADD	6.25	1.62E+08	83	75	2	0	n/a	0	2
198	4.4	2	YES	PRO	ADD	6.25	1.62E+08	76	75	2	0	n/a	0	2

B.3. Multiplication Tests.

RUN	EFF. LET (MeV-cm2/mg)	DSP	DATA VALID? (*)	DUT	TEST	FREQ (MHz)	CORRECTED FLUENCE (p/cm2)	CAT1 SEU	CAT2 SEU	CAT3 SEU	CAT4 SEU	PERSIST SEU	CFG SEU	SEFI COUNTS
65	25.0	0	NO	PRO	MUL	25.00	8.39E+07	0	0	0	0	n/a	0	0
65	25.0	1	YES	PRO	MUL	25.00	8.38E+07	0	18	1	1	n/a	2	0
65	25.0	2	NO	PRO	MUL	25.00	8.39E+07	0	0	0	0	n/a	0	0
70	16.5	0	YES	PRO	MUL	25.00	2.00E+08	3	2	0	0	n/a	0	0
70	16.5	1	YES	PRO	MUL	25.00	2.00E+08	8	23	1	0	n/a	1	0
70	16.5	2	YES	PRO	MUL	25.00	2.00E+08	4	0	0	0	n/a	0	0
71	16.5	0	YES	PACR	MUL	25.00	2.00E+08	2	1	1	0	n/a	1	0
71	16.5	1	YES	PACR	MUL	25.00	2.00E+08	1	25	2	0	n/a	2	0
71	16.5	2	YES	PACR	MUL	25.00	2.00E+08	13	0	1	0	n/a	1	0
154	12.0	0	YES	PRO	MUL	12.50	9.99E+06	19	8	0	0	n/a	0	0
154	12.0	1	YES	PRO	MUL	12.50	9.99E+06	27	4	0	0	n/a	0	0
154	12.0	2	YES	PRO	MUL	12.50	9.99E+06	29	10	0	0	n/a	0	0
157	7.3	0	YES	PRO	MUL	12.50	9.99E+06	23	6	1	0	n/a	0	1
157	7.3	1	YES	PRO	MUL	12.50	9.99E+06	20	5	1	0	n/a	0	1
157	7.3	2	YES	PRO	MUL	12.50	9.99E+06	15	6	1	0	n/a	0	1
180	2.0	0	YES	PRO	MUL	12.50	2.50E+06	2	0	0	0	n/a	0	0
180	2.0	1	YES	PRO	MUL	12.50	2.50E+06	1	0	0	0	n/a	0	0
180	2.0	2	YES	PRO	MUL	12.50	2.50E+06	2	1	0	0	n/a	0	0
182	2.0	0	YES	PRO	MUL	12.50	1.00E+08	41	21	0	0	n/a	0	0
182	2.0	1	YES	PRO	MUL	12.50	1.00E+08	31	13	0	0	n/a	0	0
182	2.0	2	YES	PRO	MUL	12.50	1.00E+08	29	21	0	0	n/a	0	0
191	4.3	0	YES	PRO	MUL	12.50	5.00E+07	38	21	1	0	n/a	0	1
191	4.3	1	YES	PRO	MUL	12.50	5.00E+07	45	30	1	0	n/a	0	1
191	4.3	2	YES	PRO	MUL	12.50	5.00E+07	34	23	1	0	n/a	0	1
194	6.6	0	YES	PRO	MUL	12.50	5.00E+07	61	30	0	0	n/a	0	0
194	6.6	1	YES	PRO	MUL	12.50	5.00E+07	71	24	0	0	n/a	0	0
194	6.6	2	YES	PRO	MUL	12.50	5.00E+07	69	26	0	0	n/a	0	0
93	31.8	0	NO	PRO	MUL	6.25	2.50E+07	209	239	30	0	n/a	24	6
93	31.8	1	YES	PRO	MUL	6.25	2.48E+07	164	33	9	0	n/a	3	6
93	31.8	2	NO	PRO	MUL	6.25	2.50E+07	200	224	27	0	n/a	21	6
98	38.0	0	YES	PRO	MUL	6.25	3.97E+07	298	95	21	8	n/a	16	13
98	38.0	1	YES	PRO	MUL	6.25	3.97E+07	373	109	20	5	n/a	12	13
98	38.0	2	YES	PRO	MUL	6.25	3.98E+07	302	84	22	2	n/a	11	13
151	7.4	0	YES	PRO	MUL	6.25	5.10E+07	68	28	3	0	n/a	0	3
151	7.4	1	YES	PRO	MUL	6.25	5.10E+07	91	20	3	0	n/a	0	3
151	7.4	2	YES	PRO	MUL	6.25	5.10E+07	70	30	3	0	n/a	0	3
154	15.0	0	YES	PRO	MUL	6.25	2.30E+07	76	20	3	0	n/a	0	3
154	15.0	1	YES	PRO	MUL	6.25	2.30E+07	69	16	3	0	n/a	0	3
154	15.0	2	YES	PRO	MUL	6.25	2.30E+07	77	13	3	0	n/a	0	3
196	2.1	0	YES	PRO	MUL	6.25	2.50E+08	95	55	1	0	n/a	0	1
196	2.1	1	YES	PRO	MUL	6.25	2.50E+08	96	42	1	0	n/a	0	1
196	2.1	2	YES	PRO	MUL	6.25	2.50E+08	85	34	1	0	n/a	0	1
199	4.4	0	YES	PRO	MUL	6.25	1.52E+08	91	49	2	0	n/a	0	2
199	4.4	1	YES	PRO	MUL	6.25	1.52E+08	134	67	2	0	n/a	0	2
199	4.4	2	YES	PRO	MUL	6.25	1.52E+08	101	52	2	0	n/a	0	2

Appendix C : CRÈME-MC Estimate Procedure

CRÈME-MC is web-based SW tool (8) that generates device upset estimates at different satellite orbits. It utilizes the industry accepted protons, electrons and heavy ion models, as well as modeling the shielding of the earth's geo-magnetic fields, to obtain upset rates. It also generates flux and fluence curves after transport through shielding using simple spherical-shield transport models. CRÈME-MC was used to generate all of the orbit upset rate estimates, and each of the CRÈME routine modules were set up as follows:

- Trapped Proton Fluxes (TRP) – *Not used*
- Geomagnetic Transmission Routine (GTRN) - *Not used*
- Space Ionizing Radiation Motel at Spacecraft Surface (FLUX)

Atomic number of lightest element included	2
Atomic number of heaviest element included	92
Nominal Environment Model GCR	Solar Minimum
Spacecraft Location	Outside Earth's Magnetosphere
Include Trapped Protons	No

- Nuclear Transport Routine Though Space Craft Shielding (TRANS)

Shielding material	Aluminum
Shield thickness	0.150 inches

- Linear Energy Transfer (LET) Spectra (LETSPEC)

Atomic number of lightest element included	2
Atomic number of heaviest element included	92
Minimum Energy value	0.1 MeV/nuc
Device material	Silicon

- Direct-Ionization-Induced Single Event Upset (SEU) Rate User-Supplied Parameters (HUP)

  The Weibull parameters utilized for each event are listed in Sections 7.1.5 and 7.2.4. The HUP routine utilizes the output of LETSPEC routine to obtain the upset rates due to heavy ions. The LETSPEC function uses the output of the TRANS routine. For all events the Rectangular Parallel-Piped model parameters X, Y, Z and funnel depth are 0, 0, 1.0µm and 0, respectively.

Appendix D : Cross-Section vs. LET Calculations

For each run and each DSP, upper and lower errors are extracted depending on count size (σ_i). The XRTC employs a Poisson distribution table with 0.01 statistical significance and 3σ error bars to obtain the positive and negative errors for all the experimental counts obtained.

The cross-section per cm^2 is obtained dividing the event counts by the corrected fluence of each run, which for dynamic tests is shown in Appendix A. Static tests did not require such a corrected fluence.

Appendix E : Test DSP Cell Configuration

- Static Register Tests:

```
UUT : DSP48E
   generic map(
   ACASCREG                          => 1,
   ALUMODEREG                        => 0,
   AREG                              => 2,
   AUTORESET_PATTERN_DETECT          => FALSE,
   AUTORESET_PATTERN_DETECT_OPTINV   => "MATCH",
   A_INPUT                           => "DIRECT",
   BCASCREG                          => 1,
   BREG                              => 2,
   B_INPUT                           => "DIRECT",
   CARRYINREG                        => 0,
   CARRYINSELREG                     => 0,
   CREG                              => 1,
   MASK                              => x"3FFFFFFFFFFF",
   MREG                              => 1,
   MULTCARRYINREG                    => 1,
   OPMODEREG                         => 0,
   PATTERN                           => x"000000000000",
   PREG                              => 1,
   SEL_MASK                          => "MASK",
   SEL_PATTERN                       => "PATTERN",
   SEL_ROUNDING_MASK                 => "SEL_MASK",
   USE_MULT                          => "MULT_S",
   USE_PATTERN_DETECT                => "NO_PATDET",
   USE_SIMD                          => "ONE48")
port map (
   A(29 downto 0)              => a_in_vec,
   ACIN(29 downto 0)           => acin_vec,
   ALUMODE(3 downto 0)         => alu_mode_vec,
   B(17 downto 0)              => b_in_vec,
   BCIN(17 downto 0)           => bcin_vec,
   C(47 downto 0)              => c_in_vec(47 downto 0),
   CARRYCASCIN                 => zero,
   CARRYIN                     => zero,
   CARRYINSEL(2 downto 0)      => carryinsel_vec,
   CEALUMODE                   => zero,
   CEA1                        => CEA1,
   CEA2                        => CEA2,
   CEB1                        => CEB1,
   CEB2                        => CEB2,
   CEC                    => CEC,
   CECARRYIN              => CECARRYIN,
   CECTRL                 => CECTRL,
   CEM                    => CEM,
```

```
CEMULTCARRYIN          => CEMULTCARRYIN,
CEP                    => CEP,
CLK                    => clk,
MULTSIGNIN             => zero,
OPMODE(6)              => opmode(6),
OPMODE(5)              => opmode(5),
OPMODE(4)              => opmode(4),
OPMODE(3)              => opmode(3),
OPMODE(2)              => opmode(2),
OPMODE(1)              => opmode(1),
OPMODE(0)              => opmode(0),
PCIN(47 downto 0)      => pcin_vec,
RSTA                   => reset_t,
RSTALLCARRYIN          => reset_t,
RSTALUMODE             => reset_t,
RSTB                   => reset_t,
RSTC                   => reset_t,
RSTCTRL                => reset_t,
RSTM                   => reset_t,
RSTP                   => reset_t,
ACOUT                  => open,
BCOUT                  => open,
CARRYCASCOUT           => open,
CARRYOUT               => open,
MULTSIGNOUT            => open,
OVERFLOW               => open,
P(47 downto 0)         => P_int(i),
PATTERNBDETECT         => open,
PATTERNDETECT          => open,
PCOUT                  => open,
UNDERFLOW              => open);
```

- Dynamic Operation Tests: Pipe-line Register Only

```
UUT : DSP48E
generic map(
   ACASCREG                          => 1,
   ALUMODEREG                        => 0,
   AREG                              => 2,
   AUTORESET_PATTERN_DETECT          => FALSE,
   AUTORESET_PATTERN_DETECT_OPTINV   => "MATCH",
   A_INPUT                           => "DIRECT",
   BCASCREG                          => 1,
   BREG                              => 2,
   B_INPUT                           => "DIRECT",
   CARRYINREG                        => 0,
   CARRYINSELREG                     => 0,
   CREG                              => 1,
   MASK                              => x"3FFFFFFFFFFF",
   MREG                              => 1,
   MULTCARRYINREG                    => 1,
   OPMODEREG                         => 0,
   PATTERN                           => x"000000000000",
   PREG                              => 1,
   SEL_MASK                          => "MASK",
   SEL_PATTERN                       => "PATTERN",
   SEL_ROUNDING_MASK                 => "SEL_MASK",
   USE_MULT                          => "MULT_S",
   USE_PATTERN_DETECT                => "NO_PATDET",
   USE_SIMD                          => "ONE48")

port map (
   A(29 downto 0)              => a_port,
   ACIN(29 downto 0)           => acin_vec,
   ALUMODE(3 downto 0)         => alu_mode_vec,
   B(17 downto 0)              => b_in_vec,
   BCIN(17 downto 0)           => bcin_vec,
   C(47 downto 0)              => c_in_vec(47 downto 0),
   CARRYCASCIN                 => zero,
   CARRYIN                     => carryin,
   CARRYINSEL(2 downto 0)      => carryinsel_vec,
   CEALUMODE                   => zero,
   CEA1                        => cea,
   CEA2                        => cea,
   CEB1                        => ceb,
   CEB2                        => ceb,
   CEC                         => cec,
   CECARRYIN                   => cecarryin,
   CECTRL                      => cectrl,
   CEM                         => cem,
```

```
CEMULTCARRYIN              => zero,
CEP                        => cep,
CLK                        => clk,
MULTSIGNIN                 => zero,
OPMODE(6)                  => opmode(6),
OPMODE(5)                  => opmode(5),
OPMODE(4)                  => opmode(4),
OPMODE(3)                  => opmode(3),
OPMODE(2)                  => opmode(2),
OPMODE(1)                  => opmode(1),
OPMODE(0)                  => opmode(0),
PCIN(47 downto 0)          => pcin_vec,
RSTA                       => reset_t,
RSTALLCARRYIN              => reset_t,
RSTALUMODE                 => reset_t,
RSTB                       => reset_t,
RSTC                       => reset_t,
RSTCTRL                    => reset_t,
RSTM                       => reset_t,
RSTP                       => reset_t,
ACOUT                      => open,
BCOUT                      => open,
CARRYCASCOUT               => open,
CARRYOUT                   => open,
MULTSIGNOUT                => open,
OVERFLOW                   => open,
P(47 downto 0)             => P_int(i),
PATTERNBDETECT             => open,
PATTERNDETECT              => open,
PCOUT                      => open,
UNDERFLOW                  => open);
```

- Dynamic Operation Tests: Pipe-line and Control Registers

```
UUT : DSP48E
generic map(
   ACASCREG                          => 1,
   ALUMODEREG                        => 2,
   AREG                              => 2,
   AUTORESET_PATTERN_DETECT          => FALSE,
   AUTORESET_PATTERN_DETECT_OPTINV   => "MATCH",
   A_INPUT                           => "DIRECT",
   BCASCREG                          => 1,
   BREG                              => 2,
   B_INPUT                           => "DIRECT",
   CARRYINREG                        => 1,
   CARRYINSELREG                     => 1,
   CREG                              => 1,
   MASK                              => x"3FFFFFFFFFFF",
   MREG                              => 1,
   MULTCARRYINREG                    => 1,
   OPMODEREG                         => 1,
   PATTERN                           => x"000000000000",
   PREG                              => 1,
   SEL_MASK                          => "MASK",
   SEL_PATTERN                       => "PATTERN",
   SEL_ROUNDING_MASK                 => "SEL_MASK",
   USE_MULT                          => "MULT_S",
   USE_PATTERN_DETECT                => "NO_PATDET",
   USE_SIMD                          => "ONE48")

port map (
   A(29 downto 0)              => a_port,
   ACIN(29 downto 0)           => acin_vec,
   ALUMODE(3 downto 0)         => alu_mode_vec,
   B(17 downto 0)              => b_in_vec,
   BCIN(17 downto 0)           => bcin_vec,
   C(47 downto 0)              => c_in_vec(47 downto 0),
   CARRYCASCIN                 => zero,
   CARRYIN                     => carryin,
   CARRYINSEL(2 downto 0)      => carryinsel_vec,
   CEALUMODE                   => zero,
   CEA1                        => cea,
   CEA2                        => cea,
   CEB1                        => ceb,
   CEB2                        => ceb,
   CEC                         => cec,
   CECARRYIN                   => cecarryin,
```

```
CECTRL                      => cectrl,
CEM                         => cem,
CEMULTCARRYIN               => zero,
CEP                         => cep,
CLK                         => clk,
MULTSIGNIN                  => zero,
OPMODE(6)                   => opmode(6),
OPMODE(5)                   => opmode(5),
OPMODE(4)                   => opmode(4),
OPMODE(3)                   => opmode(3),
OPMODE(2)                   => opmode(2),
OPMODE(1)                   => opmode(1),
OPMODE(0)                   => opmode(0),
PCIN(47 downto 0)           => pcin_vec,
RSTA                        => reset_t,
RSTALLCARRYIN               => reset_t,
RSTALUMODE                  => reset_t,
RSTB                        => reset_t,
RSTC                        => reset_t,
RSTCTRL                     => reset_t,
RSTM                        => reset_t,
RSTP                        => reset_t,
ACOUT                       => open,
BCOUT                       => open,
CARRYCASCOUT                => open,
CARRYOUT                    => open,
MULTSIGNOUT                 => open,
OVERFLOW                    => open,
P(47 downto 0)              => P_int(i),
PATTERNBDETECT              => open,
PATTERNDETECT               => open,
PCOUT                       => open,
UNDERFLOW                   => open);
```