

# Single Event Upsets in Xilinx Virtex-4 FPGA Devices

J. George, R. Koga, G. Swift, G. Allen, C. Carmichael, and C. W. Tseng

**Abstract**—We present single event upset sensitivities for three Xilinx Virtex-4 field-programmable-gate-array (FPGA) devices in protons and heavy ions. Upsets are identified in each functional block and results compared with previous device generations.

**Index Terms**—field programmable gate arrays, radiation effects, single event effects

## I. INTRODUCTION

THE Xilinx Virtex-4 field-programmable-gate-array (FPGA) is a recent generation of static random-access-memory (SRAM)-based devices [1]. These devices offer an attractive assortment of logic, clocking, and computational features and are highly programmable and reconfigurable [2]. The memory-based storage of the device configuration provides tremendous flexibility but also is susceptible to single event effects in space applications.

We measured single event upsets (SEUs) due to protons and heavy ions in the configuration bitstream of commercial Xilinx Virtex-4 LX60, SX35, and SX55 FPGAs at the Lawrence Berkeley National Laboratory (LBNL) 88” cyclotron [3].

We have found that the proton and heavy ion upset rates are improved over prior generations. Design considerations to improve the neutron performance also affect the proton response but do not extend to data stored in the Block RAMs.

The Virtex-4 SEFI modes are similar to those seen in earlier generations, again with lower rates. Functional errors in the JTAG and SelectMap interfaces are still being investigated. No SEFI mode requiring a power-cycle has been seen to date and no heavy ion latchup was observed in commercial-grade devices under normal operating conditions.

## II. DEVICE FEATURES

The Virtex-4 product line is marketed in three distinct families (LX, SX, and FX), each implementing a different mix of devices features optimized toward different applications

[2]. The LX family is weighted more heavily toward logic resources, the SX toward signal processing and memory blocks, and the FX family includes embedded microprocessors. Each device is available in a range of sizes. Table 1 summarizes the features of the three tested devices.

TABLE 1  
VIRTEX-4 TEST DEVICE FEATURES.

Functional Block	LX60	SX35	SX55
Configuration Logic Block (row x col)	128x52	96x40	128x48
Block RAM blocks (18kbits each)	160	192	320
Digital Clock Managers	8	8	8
Phase-matched Clock Dividers	4	4	4
Input/Output Blocks	640	448	640
XtremeDSP slices (DSP48)	64	192	512
System Monitor Block	1	1	1

Configuration logic blocks (CLBs) account for by far the largest number of configurable bits in each device. These blocks implement sequential and combinatorial logic and form the basic fabric for user designs. Each CLB contains lookup tables (LUTs) for logic generation, storage elements, multiplexers, and carry logic. They can implement shift registers as well.

Block random-access-memory (RAM) cells make up the next largest portion of the device. Each block provides 1-bit x 18K of memory storage. Configurable interconnect bits control the organization of the block as well as the routing connections to the user logic. The contents of the memory cells are part of the configuration bitstream and can be read back for verification and to test for single event upsets.

Certain critical functions are provided by a small number of specialized blocks. Digital Clock Managers (DCMs) provide phase-locked, skew-corrected clock signals to all parts of the chip. Phase-Matched Clock Dividers (PMCDs) offer additional frequency division options. Input/Output Blocks (IOBs) implement 28 common single-ended or differential (in pairs) I/O standards with digitally controlled impedance. Each XtremeDSP (DSP48) slice contains a dedicated 18x18-bit multiplier, adder, and 48-bit accumulator. These specialized blocks contain a small but critical number of configurable bits.

Manuscript received March 5, 2006.

J. George and R. Koga are with The Aerospace Corporation, El Segundo, CA 90245 USA (Jeffrey.S.George@aero.org)

G. Swift and G. Allen are with the Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA

C. Carmichael and C. W. Tseng are with Xilinx, Inc., San Jose CA

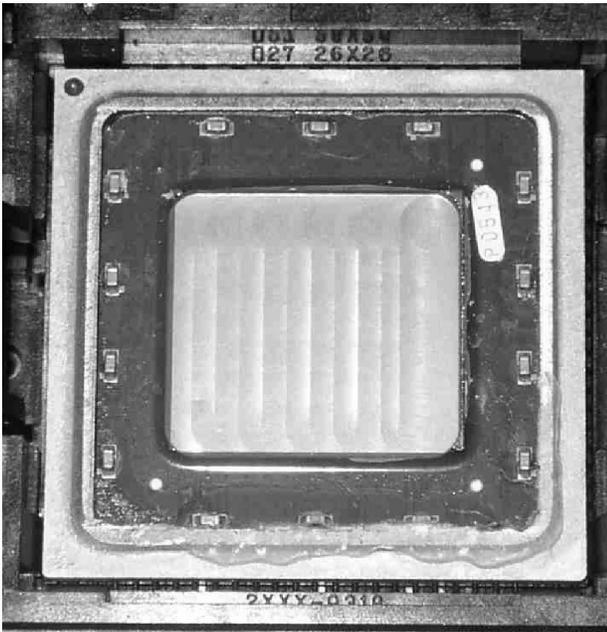


Fig. 1: Thinned LX60 device in evaluation board socket.

### III. TEST DEVICES

We tested three commercial-grade Xilinx Virtex-4 device types. The specific part numbers and the size of the configuration bitstream are listed in Table 2. All are commercial temperature grade (0°C to +85°C) and are manufactured on a 90nm copper CMOS process. The BGA package uses a “flip-chip” geometry in which the microcircuit is turned upside-down facing the package ball contacts. There is no direct access to the sensitive part of the circuit without damaging the contacts so the parts must be irradiated through

the substrate that is now facing up. The short range of heavy ion beams from ground accelerators requires that the package lid be removed and the substrate thinned to around 50µm in thickness. Fig. 1 shows a Virtex-4 LX60 device prepared for testing in heavy ions. Three thinned parts from each device family were used. An additional three (un-thinned) parts from each family were used for proton tests where the beams had no such range restriction.

TABLE 2  
PART NUMBERS FOR TESTED VIRTEX-4 DEVICES.

Part Number	Configuration Bitstream Size (bits)
XC4VLX60-10FF668C	17675264
XC4VSX35-10FF668C	13657920
XC4VSX55-10FF1148C	22702848

### IV. TEST SETUP

The parts were tested using commercial evaluation boards in air (for proton beams) or inside a vacuum chamber (for heavy ions). Fig. 2 gives a diagram of the test setup. The devices were configured via a Xilinx Parallel IV configuration cable connected to a laptop computer running the Xilinx IMPACT configuration software. A standard 25-pin parallel cable extension allowed the laptop to be placed outside the target area. IMPACT was used to configure the device before each irradiation and to verify the configuration post-exposure, reporting the number of errors detected. The device’s configuration bitstream was automatically saved during each verify to allow more extensive analysis after the test.

The test configuration contained only a single logic high on an input/output block (IOB) connected to a board LED that confirmed the design was still loaded. A few bits that provide

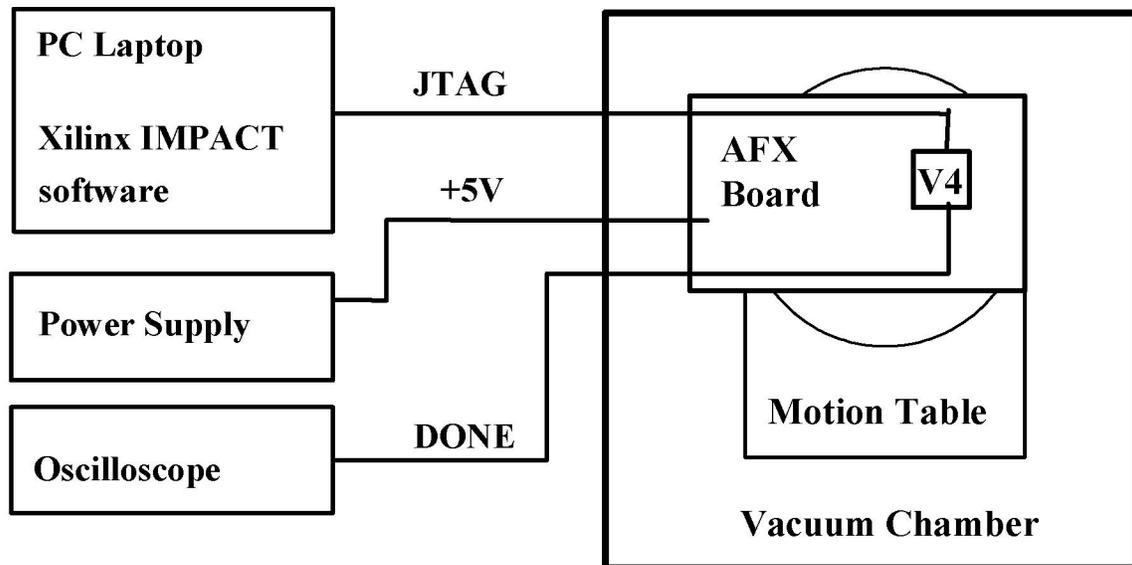


Fig. 2: Diagram of heavy ion test setup in vacuum chamber at LBNL cyclotron. The proton setup is similar, but without the vacuum chamber and feedthrough connections. The part is configured via a Xilinx Parallel IV configuration cable or a programmable read-only memory on the AFX board. Signals like the configuration DONE are brought out from the FPGA for monitoring by oscilloscope or control by the operators.

a base configuration for the Digital Clock Managers are also set by default in the Xilinx design tools. This means that the bitstream consisted almost entirely of 0's. The BlockRAM cells contained 0's so all single-event-upsets in the BlockRAM portion of the configuration bitstream represent a 0->1 transition.

For single-event-functional-interrupt (SEFI) testing, the configuration DONE pin was monitored with an oscilloscope set to trigger on a falling edge. A low value on the DONE pin indicates that the part is in reset and attempting to reconfigure. This signal is a good indicator of upsets in the power-on-reset (POR) circuit of the device though previous experience with Virtex devices suggests that in a minority of cases a POR upset may not affect the DONE signal.

The setup was identical for both proton and heavy ion testing except for the use of a vacuum chamber for heavy ions. In this case, all signals were brought out of the chamber through feedthrough connectors.

We used commercial evaluation boards purchased from Xilinx (HW-AFX-FF668-400 and HW-AFX-FF1148-400) [4]. The boards use sockets for the FPGA so test devices may easily be interchanged. Another nice feature is a large prototyping area around the FPGA socket. This allows us to have a large, uniform beam of ions without affecting other parts on the evaluation board. The boards were powered

through the 5V jacks using the on-board regulators to supply the 1.2V core and 3.3V I/O voltages to the device. The supply current was constantly monitored for evidence of single-event-latchup (SEL). Since we were not actively reconfiguring (scrubbing) the device, excessive numbers of upsets that activate contending routes could also increase the supply current during SEFI test runs with high particle fluence. Care was taken to pause the beam and reconfigure the device manually before the supply current reached a point where the voltage drop on the supply line might take the on-board regulators out of regulation.

Fig. 3 shows an AFX development board mounted on the positioning table in the vacuum chamber at LBNL. A thinned FPGA device can be seen in its socket at center right, surrounded by a prototyping area with no active components. The configuration cable and power supply jacks are at the left. Clip leads like those shown brought the DONE and PROGRAM lines out to the test area for monitoring and control.

Heavy ion testing was conducted using 10 MeV/n cocktail beams in vacuum at the LBNL 88" cyclotron. Proton beams in air with energies up to 50 MeV were available at the same facility. Additional proton data at higher energies was collected at the Indiana University Cyclotron Facility (IUCF).

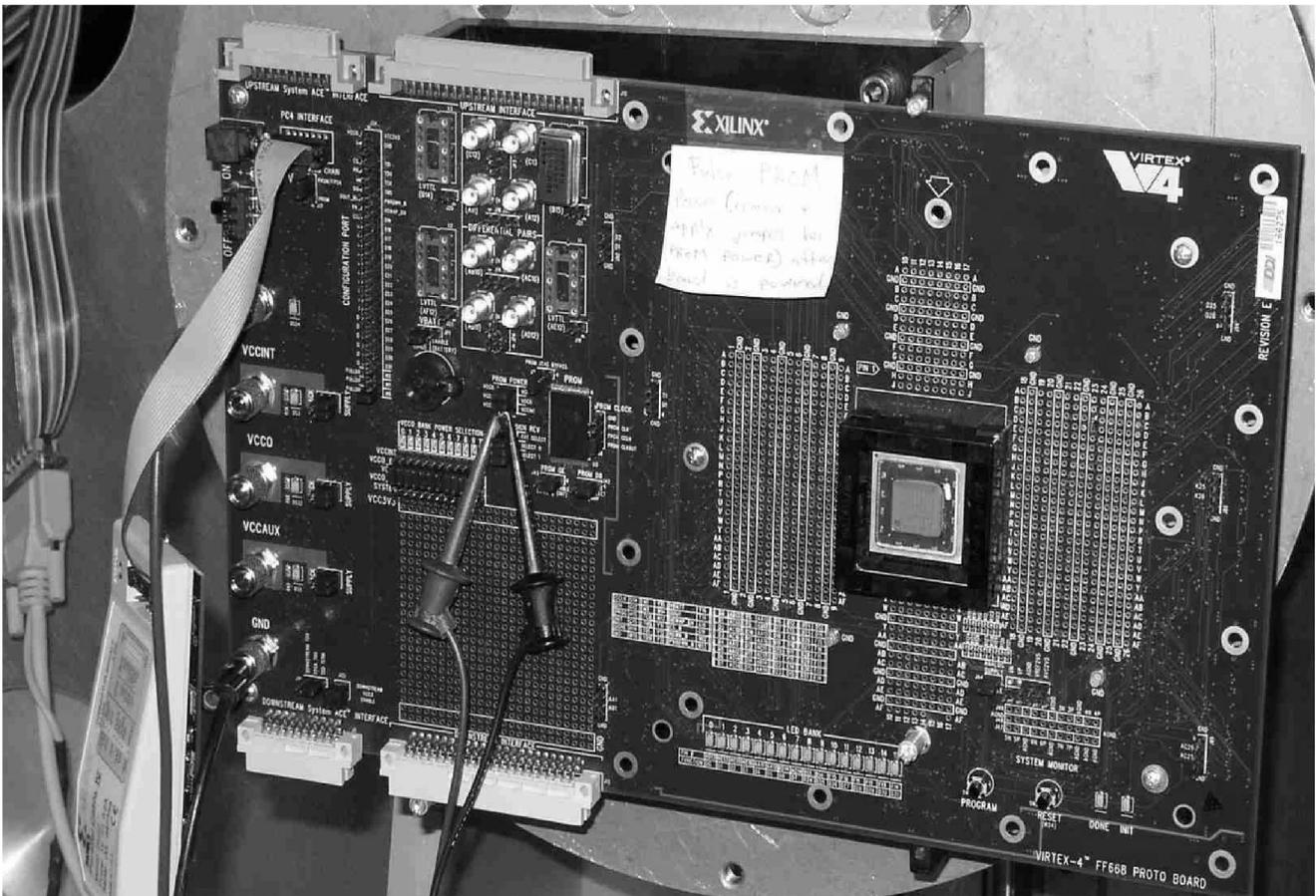


Fig. 3: Xilinx AFX development board on motion table in LBNL vacuum chamber. The FPGA device can be seen in its socket at center right. The configuration cable and power supply jacks are at left. Clip leads like those shown brought relevant signals out for monitoring.

All testing was carried out at 0° incident angle, that is, with the particle beam perpendicular to the face of the chip. Data were collected during multiple trips over a span of six months. The results were completely consistent from one trip to the next.

## V. RESULTS

### A. Heavy Ion Single Event Upsets

Results for the heavy ion SEU static cross sections are shown in Fig. 4. Multiple parts from each device type were tested and the LET values for each part were adjusted to reflect the thickness of the thinned substrate using the commonly used SRIM 2003 range-energy relations [5]. The solid and dotted curves illustrate previous results from the Virtex-II [6,7] and Virtex-II Pro [8] families. The plotted data show upset sensitivity for any physical bit in the configuration bitstream, largely dominated by the configuration logic blocks (CLBs). The Virtex-4 data look very much like that of the Virtex-II Pro, as might be expected. Error bars are not shown but are typically much smaller than the plotted points.

There is very little part-to-part variation in the plot. The two SX devices are nearly identical. The scatter in the data results largely from uncertainties in the thickness corrections. A small difference between the SX and LX parts is attributed to process variations between lots. All parts were manufactured at the Taiwan foundry and there is no family difference in the design of the FPGA fabric. The increase in the per-bit upset cross section at the highest LET values is believed to come from clusters of multiple-bit upsets (MBUs). This view is supported by a cluster analysis of MBU data performed by other members of the Xilinx Test Consortium (not yet released). On this basis we implicitly assumed that the saturation region of the heavy ion cross sections is similar

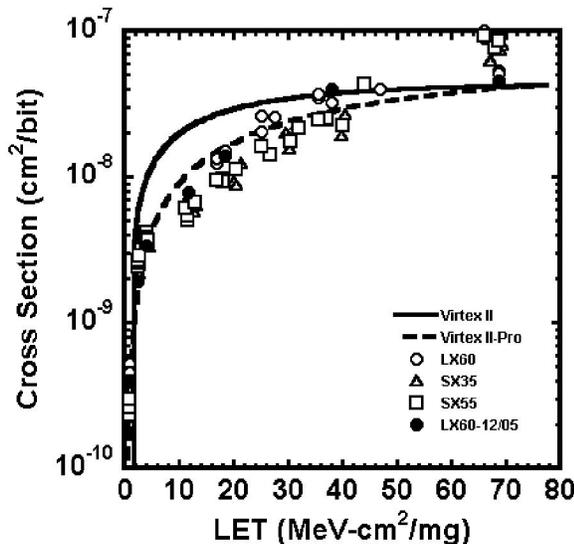


Fig. 4: Virtex-4 static SEU cross sections for three device types. Multiple parts for each type were tested. The LET value for each part has been corrected for the thickness of the thinned substrate. The filled and open circles show the consistency of the LX60 data over several trips.

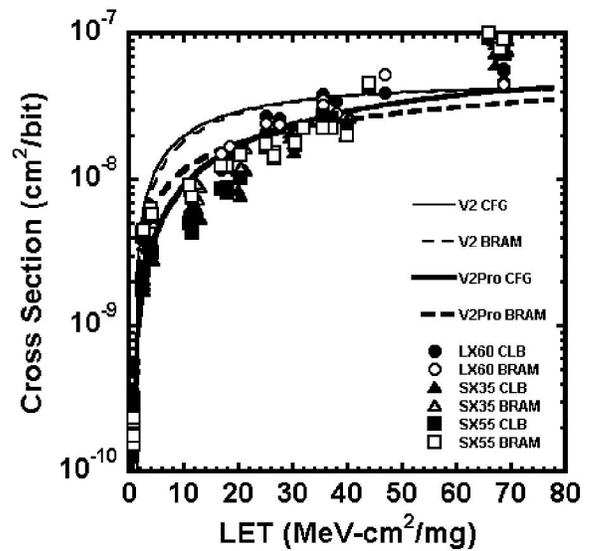


Fig. 5: Virtex-4 static SEU cross sections for three device types. Errors in the configuration logic blocks (CLB) and Block RAM (BRAM) resources are shown separately. The BRAM cells (open symbols) are consistently more sensitive in the knee region by a small amount and are very similar to cells in the Virtex II-Pro device [7].

to those for prior generations.

In Fig. 5, data for the configuration logic blocks (CLBs) and BlockRAM (BRAM) are shown separately. The Block RAM cells (open symbols) have a small but consistently higher susceptibility than the CLBs (filled symbols) in the knee region of the curve on a per-bit basis. Reasons for this are discussed below with the proton results where the difference is more apparent.

### B. Proton Single Event Effects

Fig. 6 shows the single event upset susceptibility due to protons for the three Virtex-4 devices. Multiple parts were tested for each type. Data at energies up to 50 MeV were taken at the Lawrence Berkeley National Laboratory 88" Cyclotron. Data at 98 MeV and higher were obtained at the Indiana University Cyclotron Facility. Proton energies in the plot have been adjusted to account for the thickness of the package lid and device substrate. The cross section at 98 MeV appears to be slightly higher than at 200 MeV, though the high energy point is in good agreement with other data at 100 MeV [9] and with the shape of the curves from prior Virtex generations. Some models do predict a small decrease in the cross section with increasing energy.

It is clear that all three device types are consistent with each other, the three symbols are almost always overlapping. This plot was formed by simply counting upsets in all physical bits of the configuration bitstream and overall, the Virtex-4 is less susceptible by nearly a factor of two over the Virtex-II. The threshold is more or less consistent with prior results but may be affected by straggling at the end of the beam range due to degradation of a 20 MeV proton beam incident on the surface of the part to around 4.5 MeV at the sensitive volume. Note that the plot's y-axis is broken with two orders of magnitude

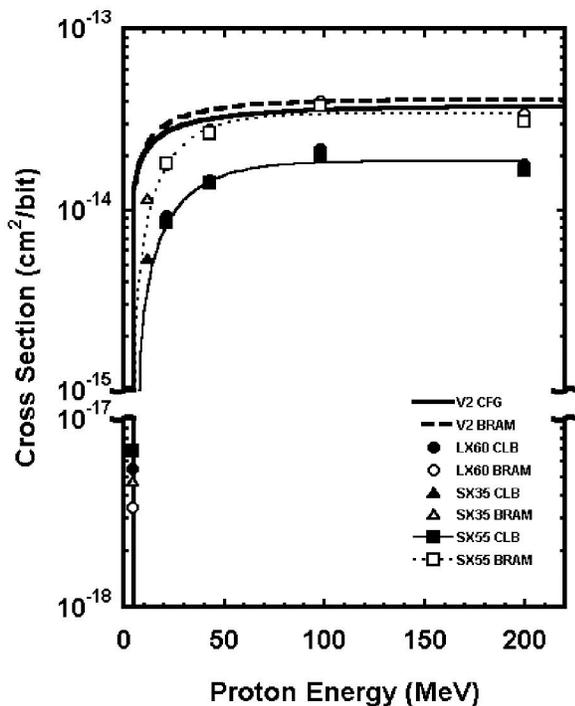


Fig. 6: Proton SEU curves for Virtex-4 devices. Data for the configuration logic blocks (CLBs) and the Block RAM (BRAM) cells are shown separately. Note the y-axis break omits two orders of magnitude.

omitted.

Fig. 7 shows the same data but with the configuration logic block (CLB) and Block RAM (BRAM) errors shown separately. The threshold energy remains the same but there is a dramatic difference in the saturation cross sections. One possible explanation may be related to differences in manufacturing. The Block RAM cells are conventional thin-oxide 90nm SRAM cells running at 1.2V with no other mitigation. The CLBs are made as thick-oxide 110nm cells with a larger channel. They also have metal added wherever possible for additional capacitive loading. The design goal was to reduce the sensitivity to neutrons (for terrestrial and aircraft applications) but the improvement clearly shows in protons as well. The large numbers of CLBs in these devices explain why the overall upset curve (for all physical configuration bits) is dominated by the CLB cross section.

Data bits stored in Block RAM memory are inherently more susceptible to proton upset than configuration logic. This reiterates the need for mitigations schemes for Block RAM data that by its dynamic nature can typically not be “scrubbed” against a golden copy as is done for the configuration itself. At the same time, even the enhanced sensitivity of the Block RAM in the Virtex-4 is as good or better than the performance of prior generations.

### C. Single Event Functional Interrupts (SEFIs)

In addition to single event upsets (SEUs), complex devices like the Virtex-4 are susceptible to single-event-functional-

interrupt (SEFI) modes. These are upsets to a control circuit that disable large portions of the devices function. From studies of prior Virtex FPGA generations we might expect to see SEFI modes involving the power-on-reset circuit (POR), failures of the JTAG or SelectMap communication ports, or others. A possible configuration clock (CCLK) upset observed in the Virtex-II Pro device was the only Virtex SEFI mode yet seen that required a power-cycle to recover. All other modes could be recovered by simply reloading the configuration. At this writing, we have studied only the POR SEFI and looked for modes requiring a power cycle.

The POR SEFI mode was investigated by monitoring the device DONE pin with an oscilloscope while exposing the part to heavy ion at high rates. A logic low on the DONE line was a clear indication that the design was lost and the part was attempting to reconfigure. As previously mentioned, a small subset of POR upsets may not affect the DONE signal and these are not counted here. Each time DONE went low, the beam was paused and the original design reloaded with IMPACT over a Xilinx Parallel IV cable (JTAG). A second iteration had the design stored in an onboard programmable read-only memory (PROM) connected to the FPGA SelectMap interface. Reconfiguration could be initiated by pulsing the PROGRAM pin on the test board via a long BNC cable.

Fig. 8 shows the POR SEFI cross section for the Virtex-4 for the two SX family devices. The results are consistent with each other. The POR cross section is improved in the knee region compared with the Virtex-II results shown by the solid black curve.

Based on the Virtex-II Pro results, some kind of SEFI requiring a power cycle for recovery was expected. We specifically looked for such a case during each of the many POR events described above. When only the JTAG cable was available to configure the device, we did power-cycle in about four cases to recover from a JTAG chain failure. Once the design was programmed into the PROM however, not one of more than 50 POR events required any more than a logic pulse to the PROG pin to reconfigure and fully recover the device. If a SEFI mode requiring a power cycle to recover exists in the Virtex-4, it has not yet been seen. The limits for such a mode are shown in Fig. 8 as error bars (at the 95% Poisson confidence level) and are already lower than the observed events in the Virtex II-Pro, shown by the dashed curve.

## VI. SUMMARY

The Virtex-4 FPGA family is a recent generation in the Xilinx lineup of advanced SRAM-based FPGAs. A characterization of the static upset performance is an essential first step toward considering these devices for use in space applications.

The static upset cross sections for bits in the configuration bitstream appears to be similar to those observed for the Xilinx Virtex-II Pro devices. The heavy ion SEU linear-energy-transfer (LET) threshold was about 1 MeV-cm<sup>2</sup>/mg

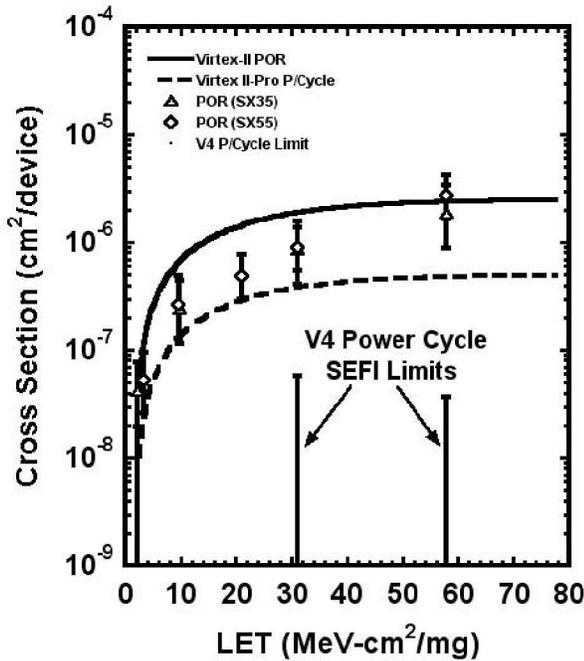


Fig. 7: Virtex-4 SEFI sensitivity for the Power-On-Reset (POR) SEFI. Results show some improvement in the knee region compared to previous generations. The Virtex-II and Virtex II-Pro curves are essentially identical [7]. Limits on the Virtex-4 SEFI modes requiring a power cycle for recovery are below the approximate level of observed events in the Virtex II-Pro.

with a saturation cross section of about  $5 \times 10^{-8}$  cm<sup>2</sup>/bit. The proton SEU threshold appears to be similar to that for the Virtex II (a few MeV) with a saturation cross section of about  $2 \times 10^{-14}$  cm<sup>2</sup>/bit for the configuration logic blocks (CLBs). Certain Single-Event-Functional-Interruption (SEFI) modes were observed, in particular the activation of the Power-On-Reset (POR) circuit that clears the configuration and resets the device. No modes observed to date require a device power-cycle for recovery. No single-event-latchup (SEL) was seen at an LET of 58 MeV-cm<sup>2</sup>/mg and a total fluence of well beyond  $1 \times 10^8$  ions/cm<sup>2</sup> for these commercial-grade devices under normal operating conditions.

#### ACKNOWLEDGMENT

The authors gratefully acknowledge the assistance of the staff at the Lawrence Berkeley National Laboratory 88" Cyclotron and at the Indiana University Cyclotron Facility. Additional assistance with the test preparation and analysis was provided by members of the Xilinx Radiation Test Consortium.

#### REFERENCES

- [1] Xilinx Virtex-4 FPGA Data Sheet (Family Overview), Xilinx, Inc., <http://direct.xilinx.com/bvdocs/publications/ds112.pdf>
- [2] Xilinx Virtex-4 FPGA User Guide, Xilinx, Inc., <http://direct.xilinx.com/bvdocs/userguides/ug070.pdf>
- [3] McMahan, M.A., "Radiation Effects Testing at the 88-inch cyclotron," RADECS 1999.
- [4] Xilinx AFX Development Board Data Sheet, Xilinx, Inc., <http://direct.xilinx.com/bvdocs/userguides/ug078.pdf>
- [5] "The Stopping and Range of Ions in Solids", by J. F. Ziegler, J. P. Biersack and U. Littmark, Pergamon Press, New York, 1985. Algorithm implemented in SRIM2003 code, see <http://www.srim.org/>
- [6] Koga, R., J. George, G. Swift, et al., "Comparison of Xilinx Virtex-II FPGA SEE Sensitivities to Protons and Heavy Ions," *IEEE Trans. Nucl. Sci.*, vol. 51, no. 5 (2004)
- [7] "Virtex-II Static Characterization", Xilinx Single Event Effects Consortium, 2004, [http://parts.jpl.nasa.gov/docs/swift/virtex2\\_0104.pdf](http://parts.jpl.nasa.gov/docs/swift/virtex2_0104.pdf)
- [8] George, J., S. Rezgui, G. Swift, and C. Carmichael for the Xilinx Single Event Effects Consortium, "Initial Single-Event Effects Testing and Mitigation in the Xilinx Virtex II-Pro FPGA", MAPLD 2005.
- [9] Hiemstra, D.M., F. Chayab, Z. Mohammed, "Single Event Upset Characterization of the Virtex-4 Field Programmable Gate Array using Proton Irradiation", NSREC 2006 Radiation Effects Data Workshop Record (this conference).