

SITE SPECIFIC CATASTROPHIC LATCHUP OBSERVATION IN ADVANCED VLSI ANALOG-TO-DIGITAL CONVERTERS



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Abstract—We report a verifiable condition in a state-of-the-art analog-to-digital converter that indicates the condition of a catastrophic latch-up is dependent on the position of the ion strike in the device. The device is seen to withstand several orders of magnitude more current during a single-event latch-up when a nonviable site is latched. The damage can be traced to a single latch in the memory of the device.

INTRODUCTION

As devices become more and more scaled, the catastrophic damage from Single-Event Latch-up (SEL) in complementary metal-oxide semiconductor (CMOS) inverters has become a more difficult problem. For example, bulk devices, as well as some epi-layered devices, have demonstrated latch-up. The character and signature of SEL have become equally complex with technology trends: Micro-latch [1,2], sympathetic latch-up paths [3] and latent damage [4,5] have all been reported as a direct result of the complex architecture in modern devices. For the most part, SEL is considered to have a uniform effect in CMOS devices. That is, the cross section and other statistical metrics of SEL characterization are thought to originate from near identical structures that have equal single-event-effect (SEE) characteristics. Studies like [4] and [5] show that this is a reasonable assumption since the damage is due to a metal trace that is equally accessible from all SEL sites. On the other hand, if a metal trace or local structure can be damaged by only one SEL-vulnerable site, it will be damaged only by an SEL at that site and not another site. The result of this condition is that a device may latch with little or no current limit and recover until an SEL in this "sweet spot" occurs and destroys the device. This paper focuses on a site-dependent SEL seen in an Analog Device AD7714 ADC, a photomicrograph of which is shown in Fig. 1. Several likely inverter structures which may latch are shown in Fig. 2.



Fig 1: Photomicrograph of the AD7714 die. The control resistor is on the right, while the analog function is on the left.

Fig 2: Photomicrograph of several SEL vulnerable structures on the AD7714.

EXPERIMENTAL: AD7714 AND BEAM TESTING

An evaluation board manufactured by Analog Devices was used for all tests. The evaluation board was interfaced to the computer's parallel port to provide functionality information via bundled software. Any modifications to the series resistance of the device were made at the power input of the board. An HP6629 quad power supply was used to power the test circuit. One of the supplies was used to power the analog circuit, and a second supply was used to power the digital circuit. SEL is detected via the test-system software which both controls the power supply voltage and monitors the supply current to the device under test (DUT). The software also provides automatic latchup detection, latch-up counting, and DUT protection. Strip charts of power supply currents and voltages are also recorded to disk by the software.

Each result in this section contributed to the conclusion of this study. During the heavy-ion and californium testing, the device was seen to repeatedly exhibit SEL with a very low current limit (20mA) and still function. If the device latched repeatedly with a higher current limit (50mA), only after a certain number of SELs would the device cease to function. Also, if the device was left in the latch state in a high current (300mA), it was seen to survive. The device always destroyed itself with over 50mA of current. Laser testing showed that different sites on the device could be latched with different resulting current levels observed. Analysis of each device showed that all damaged devices exhibited damage in the same configuration latch, which is also the damage symptom due to total ionizing dose (TID) failure of the part. All these facts, illustrated below, point to a uniquely susceptible site in this device.

BROAD BEAM/CF HEAVY ION RESULTS

Two devices were tested at room temperature as well as at an elevated temperature of 85°C. With the device at room temperature (~300K), latch-up was observed at an LET of 27.1 MeV cm²/mg. As is usual on latch-up tests, the latch-up threshold shifted to lower LETs when the test device was heated. The LET threshold for the heated measurements was below 19 MeV cm²/mg. Fig. 1 shows the results for two devices that were tested at room temperature. These data indicate that (1) ADC7714 is relatively sensitive to latch-up and (2) has a LET threshold below 27.1 MeV cm²/mg. In Fig. 2, the average results of two room-temperature measurements are compared with the heated measurements. As expected, the latchup cross section is higher for the heated device. There was a factor of 1.5-2.0 increase in latch-up cross section for the heated device. There was also a shift in the LET threshold towards lower LETs.

Current-limiting resistors were used in an attempt to protect the device from damage. A 100-Ω resistor was placed in series with the V₊ supply pin and another with the V₋ supply pin. The power supply voltages were adjusted to compensate for voltage drop across the resistors.

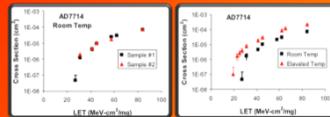


Fig 3: Comparison of SEL data obtained at room temperature for two samples.

The temperature response of SEL of the AD7714. The device exhibited the typical exponential increase in cross section in response to increase in temperature.

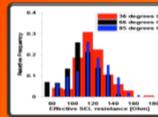


Fig 4: The effect of temperature on SEL path resistance (i.e., the ratio of voltage to current during an SEL) distribution.

Fig 6: Histogram of the resistances (defined by the measured voltage divided by the peak current) of the SELs from a CF-252 run in the digital line. The 37 traces at low current were due to SELs on the analog line. No series resistance was present.



Fig 7: Strip chart of supply current into digital power pin of device as a function of fluence. Device was nonfunctional when the supply current leapt to ~7 mA. The SEL that preceded this jump (and was expected to have been the event that damaged the write-control register) exhibited no atypical characteristics.

FOCUSED PICOSECOND LASER MAPPING OF SEL SITES

Single Event Latchup (SEL) mapping was performed using the JPL picosecond laser system comprising a mode-locked Spectra-Physics Tsunami Ti: Sapphire laser pumped by a Millennia SW laser. The system is similar to the one installed by Pouget et al. at the Université de Bordeaux [6]. A "pulse picker" module allows adjustment of the pulse rate and synchronization with instrumentation. Average laser energy is measured using a Thorlabs (PM-100 and S130A detector). For all SEL work to follow SEL dependence on laser energy was not investigated and pulse energy of around 100pJ (at the surface) was employed. The effective laser LET was calculated assuming an RPP collection depth of several microns in the digital region of the DUT. Ion tests using Californium have already confirmed the most destructive latchup sites to be in this region. Using the data from Palk et al. [7] and an assumed collection depth of several microns gives an LET of around XXX which is obviously extremely high and much larger than the LET threshold of around 24 as seen in ensures latchup for all possible sites where metallization coverage isn't an issue. Latchup measurements using a National Instruments PXI based system including a PXI 4410 power supply (up to 1A internal on 1channel). For this reason both the digital and analog VDD lines were tied to the single channel. Although this means, the location (digital or analog) cannot be discriminated against, the added benefit of spatial mapping should overcome these limitations.

An NI PXI 612 digit 1MHz DMM is used to monitor the supply current with each trigger from the laser system (plus an appropriate delay to bring the transient edge closer to view). If a latchup event was detected at a position within an XY scan, the laser was stopped, the power was removed from the DUT and the device allowed to thermally recover over 2seconds. After a further 2 seconds the device power was returned and a delay of another 2 seconds ensured complete recovery (if indeed the part had not died) before moving to the next spot in the scanning array. For the threshold currents (2mA) and clamp applied here (4mA for the data below), the device was not allowed to destroy itself. SEL mapping based on pulse shape analysis: extraction of the peak in the latchup transient over the die region image in Figure 8 above. Brighter regions correspond to higher peak currents.

Fig 10: SEL Map of die



Fig 9: 3500x2500um reflectivity image of the entire die. Bright areas correspond to areas of metallization noted in the Fig 1.

Fig 11:

Fig 12:

Fig 13:

CONCLUSION

We show that, of all the SEL-vulnerable sites on the AD7714, a single site (or a subset of sites) can cause catastrophic damage. The recurrence of damage at the same site for all damaged devices, the observation of only a fraction of SELs caused damaged devices, and the preliminary laser effects all lend credence to this supposition. The alternate hypothesis of these data, which is that repeated events cause incremental latent damage that expresses itself in device failure after a critical damage amount, is not excluded in this study, however... This ambiguity is due mostly to the wide range of SEL response across the die, but the contention that some sites result in device damage where others do not for identical conditions other than site is verified.

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