

Characterization of Upset-Induced Degradation of Error-Mitigated High-Speed I/O's Using Fault Injection on SRAM Based FPGAs

Sana Rezgui, *Member, IEEE*, Gary M. Swift, *Member, IEEE*, and Austin Lesea

Abstract—Fault-injection experiments on Virtex-II™ FPGAs quantify failure and degradation modes in I/O channels incorporating triple module redundancy (TMR). With increasing frequency (to 100 MHz), full TMR under both I/O standards investigated (LVC MOS at 3.3V and 1.8V) shows more configuration bits have a measurable detrimental performance effect when in error.

Index Terms—Fault injection, field programmable gate arrays (FPGAs), upset mitigation, upset simulation.

I. INTRODUCTION

SRAM BASED FPGAs (S-FPGAs) are very suitable for reconfigurable applications but due to their high sensitivity to SEEs in space environment, the use of those circuits should always be accompanied with mitigation techniques. One of the most used mitigation technique is the triple module redundancy (TMR) approach, which involves building three redundant copies of the mission logic and “voting out” incorrect behavior. For very critical missions, this approach requires also the triplication of the used FPGA's inputs and outputs, which might be costly in terms of FPGA resources. Although, the flexibility of FPGAs in terms of internal fabric redesigns is very powerful and complete, I/O interfaces however are fixed once the board has been fabricated. Therefore, the decision on which I/O mitigation scheme to implement should be made in advance.

As many space missions are interested in using the Xilinx Virtex FPGAs, many research activities [1], [2] have been done to evaluate the performance of the Virtex-II Input Output Blocks (IOBs) with or without mitigation. It has been recommended to mitigate the design's inputs (triplicated and voted) because of the risk of error propagation in the circuit design. No accurate studies have been made on whether the outputs should be mitigated and what the tradeoffs are if we choose not to. The main objective of this paper is to evaluate the Virtex-II output block performances when mitigated in comparison to when it is not (assuming that the input is always mitigated).

Virtex-II devices are provided in -6 , -5 , and -4 speed grades, with -6 having the highest performance. At the

highest speed grade, the maximum speed for an output block is 277 MHz. Further details on the Virtex II IOB switching characteristics are provided in [3]. This study is based on the Virtex-II XC2V6000-6, and the mitigation approach (TMR) is tested on two of the most used IO standards in space applications: the Low Voltage Complementary Metal-Oxide Semiconductor (LVC MOS) at two different voltage levels 3.3 V and 1.8 V.

The Low-Voltage CMOS for 3.3 V or LVC MOS33 standard is used for general purpose 3.3 V operations. This IO standard is defined in JEDEC (once known as the Joint Electron Device Engineering Council) Standard JESD 8-B, Interface Standard for Nominal 3.0 V/3.3 V Supply Digital Integrated Circuits. LVC MOS33 is more stringent than the LVTTTL specifications in that the outputs are required to swing rail to rail under light DC load conditions. The input buffer requirements are the same as the LVTTTL requirements. This standard requires a 3.3 V output source voltage.

The Low-Voltage CMOS for 1.8 V or LVC MOS18 standard, as defined by JEDEC standard JESD 8-7, is used for general purpose 1.8 V applications. It is similar to LVC MOS33 but is used for 1.8 V power supply levels and has been modified to reduce input and output thresholds. This standard requires a 1.8 V output source voltage. Both LVC MOS33 and LVC MOS18 IO standards do not require the use of a reference voltage or a board termination voltage. More information about these IO standards is provided in JEDEC catalogue [4].

For each IO standard, two main designs (non-mitigated output and mitigated output) have been targeted to evaluate the proposed mitigation technique (TMR) for a given output.

II. RELATED WORK

Previous work [1] shows beam data from the testing of four IO standards [LVC MOS (3.3 V and 1.8 V) and LVDS (2.5 V and 3.3 V)] under heavy ion beams. The results showed that for very critical missions, requiring a very low error rate, the outputs must be triplicated. Because of the long beam hours for the IOs' characterization required to reach such a conclusion and the wide range of IO configurations that should be tested, additional Fault Injection (FI) testing was required to help characterize the effects of SEUs on the Virtex-II IOBs. The FI technique, described in [1], is based on the *partial* reconfiguration of a memory segment (specific feature to the Xilinx Virtex FPGAs) and allows fault-insertion in all the FPGA's configuration bits which are susceptible to SEUs. The main objective of using such a technique is to give a detailed understanding of the impact of

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S. Rezgui and A. Lesea are with Xilinx, Inc., San Jose, CA 95124 USA (e-mail: sana.rezgui@xilinx.com).

G. M. Swift is with the Jet Propulsion Laboratory/California Institute of Technology, Pasadena, CA 91109 USA (e-mail: gary.m.swift@jpl.nasa.gov).

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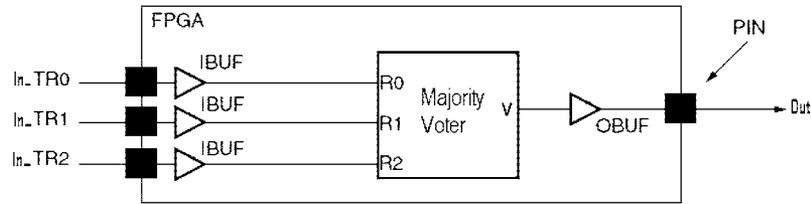


Fig. 1. Majority Voted TMR FPGA Output.

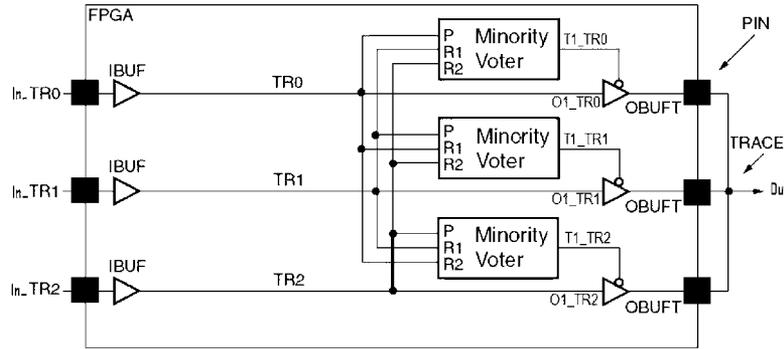


Fig. 2. Minority Voted TMR FPGA Outputs. The 3 output pads are connected externally to the DUT to bring the triple logic paths back to a single output path.

SEUs on specific regions of the FPGA such as the IOBs in an efficient and affordable alternative to the beam experiments.

In [1], FI experiments have been exercised on the LVCMOS33 IO standard while operating at 8 MHz. It has been demonstrated that FI results and beam data are compatible. It should be mentioned that, no FI tests have been conducted on high-speed IO interfaces (above 100 MHz) or with low voltage levels (1.8 V). The experiment of [1] consisted of a pass or fail test, which compares the logic value of the input sent to the DUT to its output and any resulting mismatch, is counted as an error. This type of test does not show the signal degradation that might occur on the output signal although the test has passed. With rise times less than 1 ns and timing margins measured in picoseconds and voltage input thresholds of several 100 mV a closer look at output TMR IOB structures operating at high speed overall operation in a SEU environment is necessary [2].

Therefore, the main goals of this paper are to:

- Go beyond a pass/fail test and observe each output signal on the oscilloscope after each flip of a bit to capture any signal degradation that might have resulted from FI.
- Study the performance of output mitigation schemes, while operating at high-speed (up to 100 MHz) using FI technique and assuming that the inputs are always triplicated and voted.
- Test the LVCMOS IO standard with two different voltage levels (3.3 and 1.8 V) to evaluate the impact of the voltage variance.

III. STUDIED CASES

Reference [1] presented single-event upset results on a Virtex II device for four IO standards using two specific IOB mitigation

schemes suggested by [5]. The three designs to test the mitigation schemes are:

1. The “unprotected” test design, which consists on routing 32 input-signals to 32 output-signals. Each input-output pair is called IO channel.
2. The “TMR-in Only” test design where each IO channel uses three IOBs as triplicated inputs (In_TR0, In_TR1 and In_TR2) voted by a single majority voter and connected to a single output buffer, an “OBUF” primitive for output (see Virtex II Libraries in [6]). The scheme of this design is depicted in Fig. 1.

The function of the majority voter is to output the logic value (“1” or “0”) that corresponds to at least two of its inputs. If the inputs of the voter are labeled R0, R1, and R2, and the output V, respectively, then the Boolean equation for the voter is:

$$V = R0R1 + R0R2 + R1R2$$

3. The “Full TMR” design, where each IO channel uses three IOBs as triplicated inputs connected to three more IOBs configured as triplicated outputs voted through triplicated minority voters (called also TRV in this paper). The function of a minority voter is to block the output if it disagrees with the other two. Fig. 2 shows the block diagram of this implementation.

In the “Full TMR” design, a TMR output is constructed using a tri-state output buffer “OBUFT” primitive [6] as shown in Fig. 3. Each redundant logic path exiting the FPGA on an output does so through an OBUFT. The enable T pin of each OBUFT is controlled by a minority voter circuit. The minority voter indicates whether the path in question (primary path) agrees with either of the two redundant paths. If the primary path agrees with at least one of the redundant paths, then the primary path

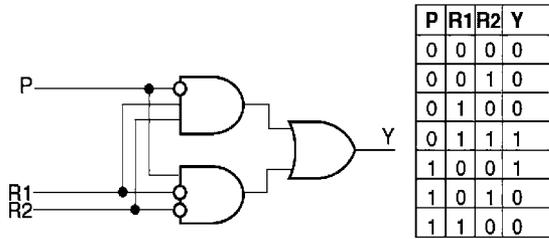


Fig. 3. Minority Voter Circuit Scheme and Truth Table of its Function.

is considered to be part of the majority. If the primary path disagrees with both redundant paths, then the primary path is the minority.

If the primary path is part of the majority, then the minority voter will enable the corresponding (active low) OBUFT allowing the data on its primary path to be driven out through the OBUFT and onto the Pad-Pin. If the primary path is not a part of the majority, then the OBUFT is disabled placing its output in a high-impedance state allowing the redundant outputs to drive the correct data.

External to the FPGA, the three outputs are hardwired together on the circuit board. This structure should not cause any contentious states because only paths that agree with each other are actively driven. This method also has the added benefit of doubling and/or tripling the sink and source current capabilities of the output from the perspective of other components on the board that are connected to this board trace. But the primary advantage to this method is that no external devices are needed to complete the triple redundant voting, as would be the case when using triple redundant FPGAs instead of internal redundancy within a single FPGA.

As the main objective of this paper is to evaluate output mitigation performance, only the two latter test designs (“TMR-in Only” and “Full TMR”) have been considered in this paper. Because the exact same test designs (same routing and components) of [1] were used for this study, the comparison with those 8 MHz beam and FI results is possible.

To demonstrate the impact of the frequency and voltage variances for an IO standard on the IOB’s sensitivity to SEUs, FI experiments have been performed on the LVCMOS IO standard test designs operating first at 3.3 V (LVCMOS33) and then at 1.8 V (LVCMOS18). For each one of them, the experiments have been performed at two frequencies: 50 MHz and 100 MHz.

A. FI Implementation

Each FPGA internal architecture is built on sequential and combinatorial logic (Look-Up Tables (LUTs), Flip-Flops (FFs), IOBs, etc.). LUT architecture for instance, enables flexible implementation of any function with variable inputs, as the majority or minority voters in the studied test designs. All these internal resources are coded in a stream of bits, known as bitstream or configuration memory of the FPGA. Each implementation of a given design codes the bits of this configuration memory in a certain way. However, not all the bits of the bitstream are used for every design. The bits associated to a given design are called “used bits” in this paper.

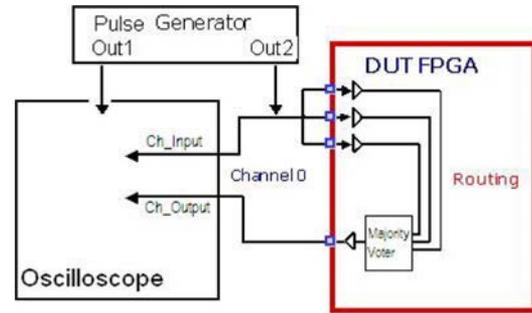


Fig. 4. “TMR-in Only” Design.

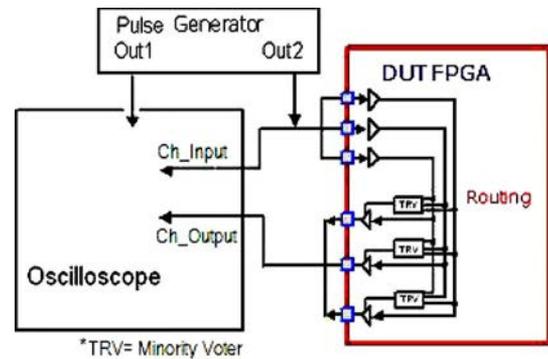


Fig. 5. “Full TMR” Design.

The configuration memory of an FPGA from the Virtex family is shared in a set of “frames”. A frame is the smallest unit for partial reconfiguration in a Virtex bitstream. The selected target circuit, the XC2V6000, is segmented into over 2000 configuration frames, where each one of them is a set of 7872 bits.

To implement the FI technique, the FIVIT (Fault Injection and Verification Tool) software application (previously used for the SEE characterization of the Virtex-II [7]) has been enhanced with a new functionality that allows FI in the bitstream with less intrusiveness. Indeed, by means of partial reconfiguration through the JTAG port and with no interruption of the test design operation, the FI test sequence consists of the following.

1. Locate target bit in the bitstream for FI;
2. Read and store frame in a buffer of 7872 bits;
3. Flip the target bit, which will result in a faulty frame;
4. Write back faulty frame in the configuration memory;
5. Observe the output on the oscilloscope and store the waveform snapshot;
6. Correct the upset by flipping back the bit in the faulty frame and rewriting this frame in the FPGA;
7. Check the correctness of the output waveform;
8. Select another target bit and repeat from (1).

In addition, as the objective of this paper is to use the FI approach to observe the output response with an oscilloscope mainly when the Xilinx TMR tool mitigates it, hardware accessibility to the inputs and outputs of any IO channel is required. An AFX Virtex-II-FF1152 board, which offers easy access to all the IOs of the DUT, was used as an experimental platform.

For design’s input supply, a pulse generator is used to generate two identical high-speed signals. The voltage level of these

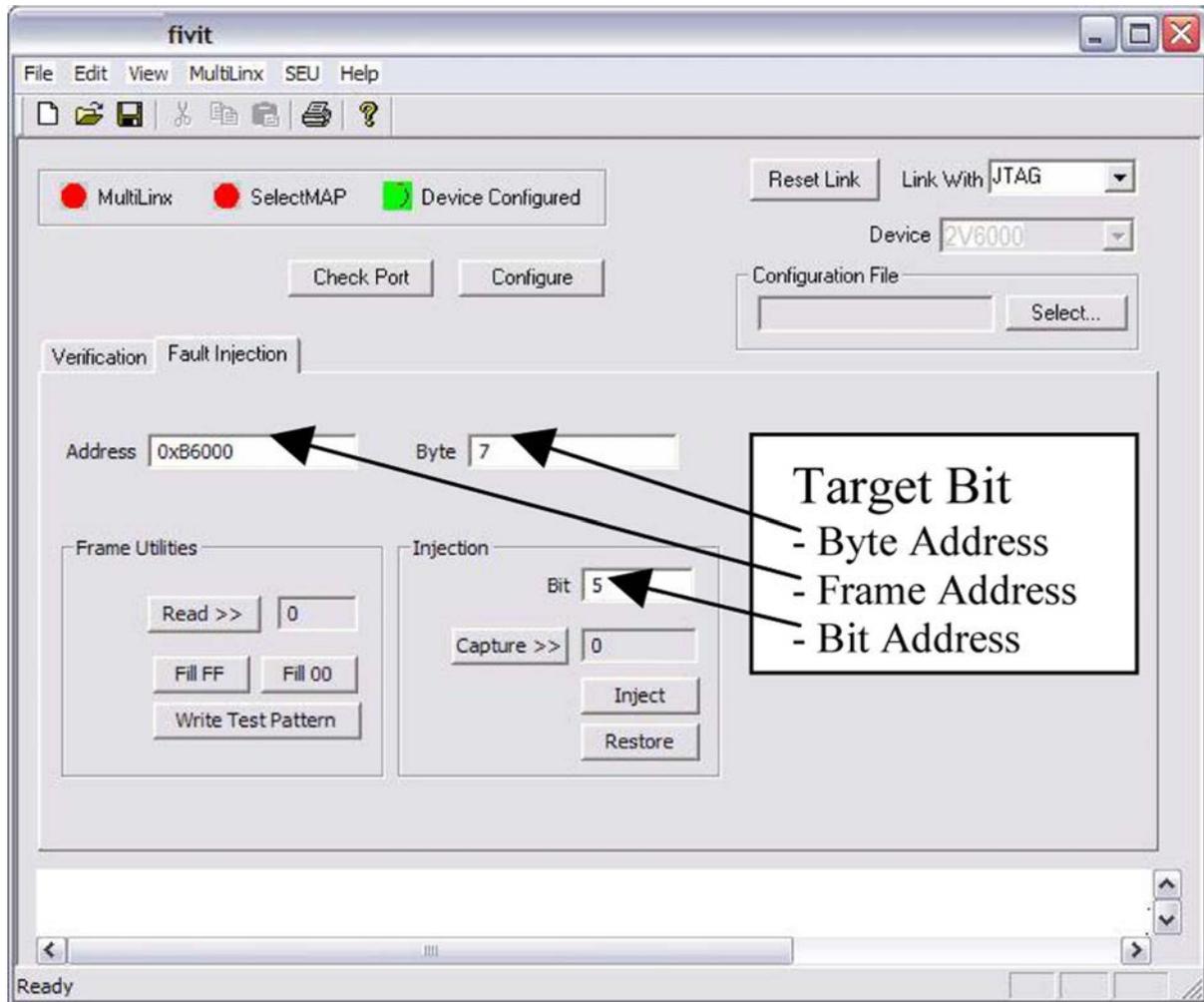


Fig. 6. FIVIT User Interface.

signals is set according to the tested IO standard (3.3 V for the LVC MOS33 and 1.8 V for the LVC MOS18). This output signal is a simple train of pulses at a given frequency (50 or 100 MHz) in order to simulate the low and high logic levels on the FPGA IOB input. Indeed, if an SEU in the configuration memory used for the output IOB caused a stuck at high of the output signal, this error won't be missed as it would be in the case of a constant high input.

The block diagrams of the two designs' implementations on the test bench are given in Figs. 4 and 5. The first pulse generator output is driven to the oscilloscope and the second output is connected to the three inputs of the IO channel, as shown in Figs. 4 and 5. After each injected bit-flip, a new oscilloscope snapshot of the output waveform with the measurements of its features (frequency, voltage (maximum, high and low), and rise and fall times) is captured in a snapshot for later comparison to the reference snapshot (where no bit flips was injected).

B. Design Fault List

To view the set of used configuration bits of the studied designs, a Xilinx tool called SEUPI (Single Event Upset Probability Impact Tool) has been used [8]. Besides calculating the number of used bits, this tool also gives the user the ability to

locate those bits in the bitstream and hence to generate a better view of any user design. As they are considered as *possibly* sensitive to SEUs, the set of a design's used bits is called "fault list" in this paper. This list has been determined for each of the studied cases (4 test designs) and classified per IO channel. However, unlike the automated FI technique that has been applied in [1], the selection of the target bit location (which requires the entry of the frame, byte and bit addresses) is entered manually in the Graphical User Interface, as shown in Fig. 6. This allows the capture of the output waveform after flipping a bit without missing signal degradation on the output signal.

This FIVIT FI is definitely slower than the automated one presented in [1], where a second FPGA runs it and makes the decision whether a bit is causing an error on the output block.

A few test approaches have then been made, to enhance this FI and speed up these measurements.

- 1) The new FI experiments (with FIVIT) have been exercised only on one IO channel (channel 0).
- 2) The first FI technique [1] is designed to insert faults in all the bits of a design's used frame whether the bit has been found to be used or not. This conservative choice has been made previously to test the efficacy of the SEUPI tool and to not miss any of the sensitive bits. Because of the

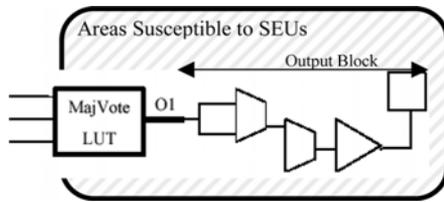


Fig. 7. Area Susceptible to SEUs in the “TMR-in Only” case (single majority voter, Output Block and the routing between them).

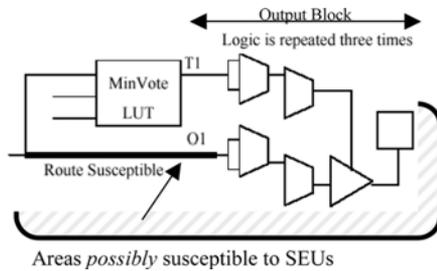


Fig. 8. Area Susceptible to SEUs in the “Full TMR” case (three IOBs as triplicated outputs, triplicated routes O1).

fact that every bit found experimentally had indeed been identified by the SEUPI tool, only the SEUPI bits have been considered in this study.

- 3) For the unprotected design and for each IO channel, the fault list includes the bits used for the triplicated inputs, the majority voter, the used part in the output block, and the routing between them as shown in Fig. 7. For this design, only the used bits to define the majority voter, the routing O1 from the voter to the output and the IOB are considered to be *possibly* sensitive to SEUs. FI experiments have been performed only on those bits.
- 4) In the protected output case, the fault list includes the bits used for the triplicated inputs, the minority voters, the triplicated outputs and the routing between them. In this case, only the routing to the input O1 of the output IOB is considered to be *possibly* sensitive since all the other paths are voted through minority voters (Fig. 8). In addition, for any TMR scheme, the three copies (called domains TR0, TR1 and TR2) of an IOB should be symmetric. Any bit flip in domain TR0 should have the same effect as if injected in domain TR1 or TR2. But, as the Xilinx solution proposes hardwiring the 3 outputs externally to the DUT, the bits that have been used to define the 3 used IOBs for outputs are also subject to these FI experiments. This will allow the validation of the theoretical assumption made earlier about the non-existence of any contentious states when hardwiring the 3 output-pads externally.

Considering the above assumptions and for each tested IO standard, Table I shows the number of used bits corresponding to each used part of the circuit design (routing, voters and IOB). Note that for each one of the test designs (“TMR-in Only” or “Full-TMR”) both IO standards (LVCMOS33 and LVCMOS18) have the same set of used bits.

TABLE I
CLASSIFICATION OF THE BITS SUSCEPTIBLE TO SEUs

Design	Output IOB	Voter (Maj. or Min.)	Routing
TMR-in Only	63	46	90
Full TMR	189	-	482

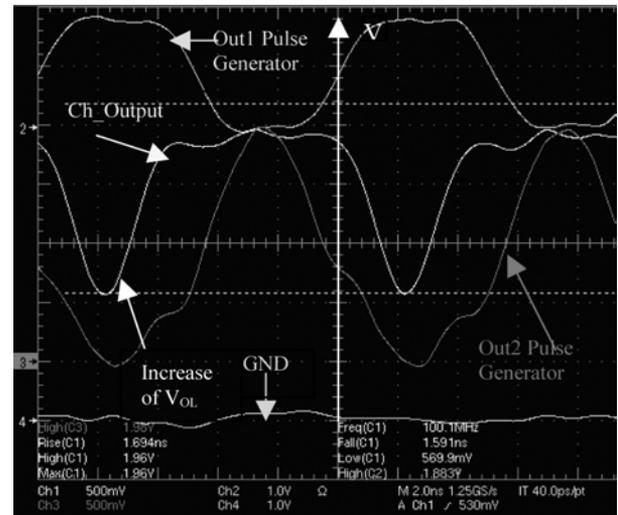


Fig. 9. Error mode where the output voltage V_{OL} is higher than the LVCMOS IO standard specification (0.4 V).

IV. EXPERIMENTAL RESULTS

Each stored scope snapshot of the output waveform was compared to the reference snapshot (where no bit flips were injected). The signal degradation was measured based on the output and input voltage levels of the LVCMOS specifications given in Table II, where:

- V_{IH} (Voltage Input High): The minimum positive voltage applied to the input which will be accepted by the device as a logic high.
- V_{IL} (Voltage Input Low): The maximum positive voltage applied to the input which will be accepted by the device as a logic low.
- V_{OL} (Voltage Output Low): The maximum positive voltage from an output which the device considers will be accepted as the maximum positive low level.
- V_{OH} (Voltage Output High): The maximum positive voltage from an output which the device considers will be accepted as the minimum positive high level.

During the FI experiments performed on the “TMR-in Only” design, six types of errors have been observed on the output waveforms:

- Stuck at fault where the output signal is stuck at 0 V or at the voltage level of the IO standard (1.8 or 3.3 V)
- Inversion of the output signal
- Increase of the output voltage V_{OL} higher than the LVCMOS IO standard specification (Fig. 9)
- Increase of the output voltage V_{OH} higher than the LVCMOS IO standard specification
- Drop of the output voltage V_{OH} lower than the LVCMOS IO standard specification (Fig. 10)

TABLE II
LVC MOS IO STANDARD SPECIFICATIONS

Voltage (V)	V_{OH}		V_{OL}		V_{IH}		V_{IL}	
	Max	Min	Max	Min	Max	Min	Max	Min
LVC MOS18	1.9	1.3	0.4	-0.5	1.95	1.19	0.4	-0.5
LVC MOS33	3.6	2.6	0.4	-0.5	3.6	2.0	0.8	-0.5

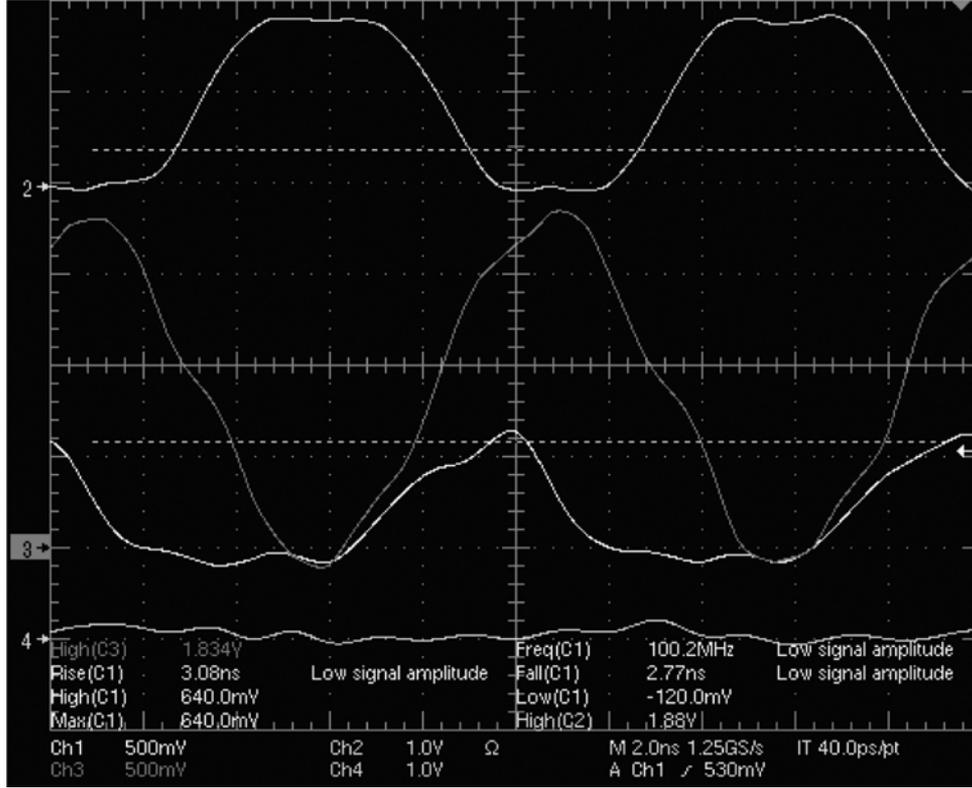


Fig. 10. Error mode where the output voltage V_{OII} is higher than the LVC MOS IO standard specification (1.3 V).

TABLE III
NUMBER OF SENSITIVE BITS OF THE DESIGN “TMR-IN ONLY”

Test	Volt. (V)	Freq. (MHz)	$V_{OH} \nearrow$	$V_{OH} \searrow$	$V_{OL} \nearrow$	Inversion	Stuck at fault	Others
Oscilloscope	1.8	50	2	1	1	1	35	6
Oscilloscope.	1.8	100	2	1	1	1	35	6
Oscilloscope.	3.3	50	2	1	1	1	35	6
Oscilloscope.	3.3	100	2	1	1	1	35	6
Pass/Fail	3.3	8	0	1	1	1	35	6

— Observation of a difference in the signal response waveform, classified as others in Table III. Any modification of the rise and fall times of the output signal was classified in this category.

Note that no drop of the output voltage V_{OL} lower than the LVC MOS IO standard specification has been noted upon upsets in the configuration memory bits.

In Tables III and IV, we provide the counts of sensitive bits (that cause an error on the output signal) for each type of errors. Because the earlier work [1] and the new FI experiments have been made on the same test designs, the comparison between the results from the testing of the LVC MOS33 at 8 MHz and the new results derived from the testing of this IO standard at higher frequencies is possible.

TABLE IV
NUMBER OF SENSITIVE BITS OF THE “FULL-TMR” DESIGN

Test	Volt. (V)	Freq. (MHz)	(V_{OH} , V_{OL})	(V_{IH} , V_{IL})
Scope	3.3	100	36	12
Scope	1.8	100	36	12
Scope	3.3	50	36	0
Scope	1.8	50	36	0
Pass/Fail	3.3	8	0	0

In the case of the “TMR-in Only” design (Table III), the results show that the decrease of the voltage level or the increase of the output signal frequency has no impact on the total number of sensitive bits of the tested design (46 bits for the tested IO standards). In addition, in all the previous and new FI experiments

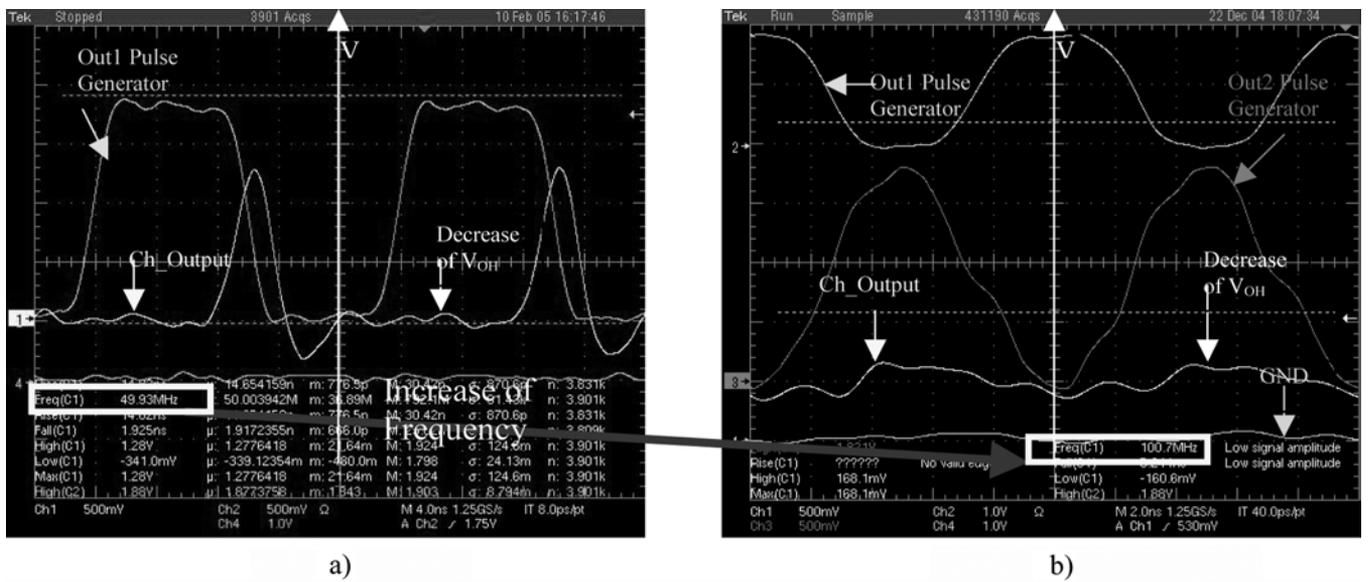


Fig. 11. Impact of the frequency on the signal degradation of the LVC MOS18 IO standard (a) 50 MHz, (b) 100 MHz.

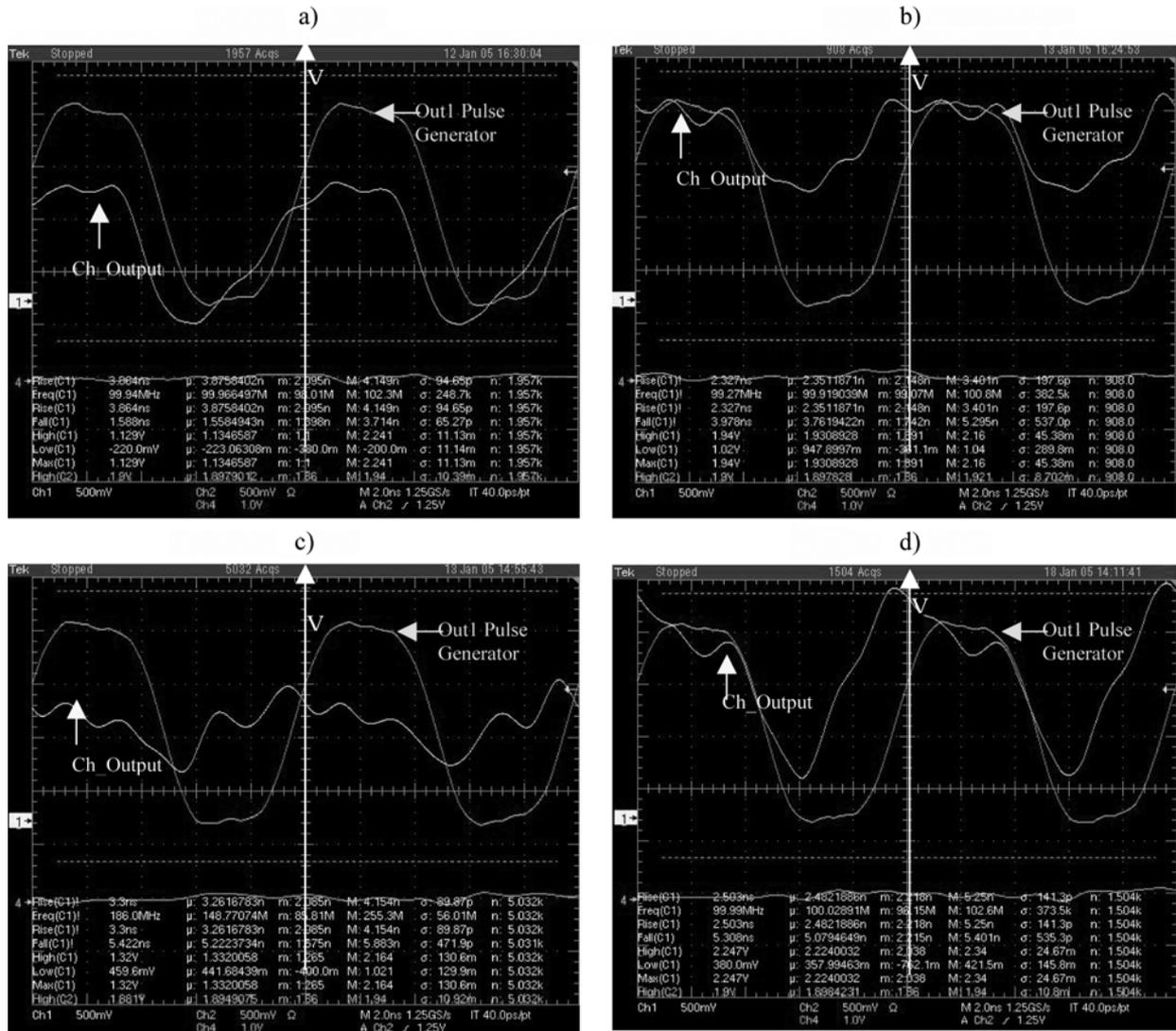


Fig. 12. Snapshots of the output voltage level beyond the LVC MOS IO standard specifications (a) $V_{OH} < 1.3$ V, (b) $V_{OL} > 0.4$ V, (c) $V_{OL} > 0.4$ V, (d) $V_{OH} > 1.9$ V.

performed on the "TMR-in Only" design (for all the tested IO standards), errors have resulted from the single flip of the exact same bits. Thus, it's clear that a pass/fail test would have been enough to estimate the SEU-sensitivity of an IOB, although such kind of test does not show the number of bits (2 in this case) that increase the V_{OH} higher than the IO standard specifications or the output signal degradation.

Indeed, observing the output waveforms while implementing the LVCMOS IO standards and operating at different frequencies showed higher signal degradation when increasing the frequency (from 50 to 100 MHz) or decreasing the voltage level (3.3 V to 1.8 V) as shown in Fig. 11. The same number and locations of sensitive bits have been noticed when comparing the output signal based on the specified input voltage levels cited in the Table II.

In the case of the "Full-TMR" design (Table IV), no hard faults (stuck at faults, inversion of the signal), have been noted but the observation of the oscilloscope snapshots showed that the increase of frequency has an impact on the output IOB sensitivity to SEUs. Fig. 12 shows 4 scope snapshots where the output signal did not meet the specifications of IO standards.

The results show that, at 8 and 50 MHz, no injected faults cause sufficient degradation of the output signal to fail to meet actual voltage input levels. However at 100 MHz, there are 12 bits that cause sufficient degradation to fail for both tested IO standards (LVCMOS33 and LVCMOS18). But when the output signal is calibrated in regards to the voltage output levels, we have observed an increase of those numbers (up to 36 bits) which also don't vary with the frequency. This result was expected since the voltage input levels are more tolerant than the voltage output levels and the number of sensitive bits per output block should always be lower if we judge on the voltage input specifications.

It should be mentioned that the observation of the scope snapshots shows higher signal degradation at 100 MHz than at 50 MHz even when the number of sensitive bits remains the same. This proves that the higher the frequency, the higher the signal degradation of the output block. It is clear however that the number of sensitive bits does not depend on the voltage although a careful observation of the scope snapshots showed that few bits if flipped provoked higher signal degradation when running the LVCMOS18 test design than when testing the LVCMOS33.

V. CONCLUSION

In this paper, we present a detailed characterization of the Virtex-II IOBs used as outputs based on the observation with

an oscilloscope of the output response after each injection of a single-bit error in the configuration of the studied circuit design. Two IO standards have been studied while varying the frequency. The results show that a simple pass/fail test is sufficient for the IOB characterization except for voltage overshoot. Bits affecting voltage overshoot can only be found with oscilloscope visibility under single-event irradiation or fault injection, as was done here.

It has also been demonstrated that the number of sensitive bits increases with the frequency of the output signal (12 bits for an output signal operating at 100 MHz, but none at 50 MHz). For high-speed IO interfaces (> 100 MHz), it is advisable to avoid the hardwiring of the three output signals and rather drive the three signals to be voted by an external active device. In contrast to the importance of frequency, bias did not have any effect on the output block sensitivity in terms of number of sensitive configuration bits.

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REFERENCES

- [1] G. M. Swift, S. Rezgui, J. George, C. Carmichael, M. Napier, J. Maksymowicz, J. Moore, A. Lesea, R. Koga, and T. F. Wrobel, "Dynamic testing of Xilinx Virtex-II field programmable gate array's (FPGA's) input output blocks (IOBs)," *IEEE Trans. Nucl. Sci.*, Dec. 2004.
- [2] M. Napier, J. Moore, K. Lane, S. Rezgui, and G. M. Swift, "Single event effect (SEE) analysis, test, mitigation & implementation of the Xilinx Virtex-II input output block (IOB)," presented at the MAPLD'04, Washington, DC, Sep. 9-11, 2004.
- [3] Virtex-II Platform FPGAs: Complete Data Sheet [Online]. Available: <http://direct.xilinx.com/bvdocs/publications/ds031.pdf>
- [4] [Online]. Available: <http://www.jedec.org/Catalog/display.cfm>
- [5] C. Carmichael, "Triple module redundancy design techniques for Virtex FPGAs," *Xilinx Application Note XAPP197*, Nov. 2001.
- [6] Virtex-II Platform FPGA: User Guide 2005 [Online]. Available: <http://direct.xilinx.com/bvdocs/userguides/ug002.pdf>
- [7] C. Yui, G. M. Swift, C. Carmichael, R. Koga, and J. George, "SEU mitigation testing of Xilinx Virtex II FPGAs," presented at the NSREC'03, Monterey, CA, Jul. 21-25, 2003.
- [8] P. Sundararajan, C. Patterson, C. Carmichael, S. McMillan, and B. Blodget, "Estimation of single event upset probability impact of FPGA designs," presented at the MAPLD'03, Washington, DC, USA, Sep. 9-11, 2003.