Commercial Off-The-Shelf (COTS)
The Next Generation of Electronic Parts for Space

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Agenda

Introduction to COTS

Methodology/Evaluation for Risk Assessment

COTS Work Plan/Status

COTS Work (Examples)

Summary
The COTS Program

Develop a *methodology* to evaluate & select COTS that-

- Minimizes the cost of part risk management
- Uses an engineering-based approach vs “rule’ based
- Stimulates gaining new knowledge and experience
- Establishes a systematic approach to evaluation
- Uses Mfr. and other pre-existing data as much as possible
- Provides optimized evaluation & test path per part
- Allows trade-off assessment with high reliability parts
- Establishes COTS guidelines for Space Applications
The Meaning of COTS

• “Buy and Fly”

• “Procuring via catalog part number to QML-V standards”

• “Procurement is performed without formal specification”

• “The usage of any COTS equipment does not constitute any waiver to fundamental applicable requirements”

Our Interpretation:

• COTS are parts whose specification is manufacturer-controlled as opposed to traditional “Hi-Rel” parts whose specification was Government or customer-controlled
Why Put COTS in Space?

1. The availability of COTS parts is proliferating.

2. COTS parts performance capabilities continue to increase (e.g. processing power & high density memories)

3. A new generation of leading COTS IC technologies is introduced every 3 years.

4. COTS parts typically cost much less than radiation hardened counterparts; by using radiation tolerant parts the cost advantage can be preserved.

5. Some COTS parts have been reported to demonstrate good to excellent reliability.
Concerns About Using COTS

- Life Cycle is Determined by Market Demand
- Process/Designs Change Frequently
- Narrow Temperature Range
- Non Rad Hard Designed (maybe Rad Tolerant)
- Reliability of PEMS vs Ceramic
COTS Infusion Path

PROJECT DRIVERS

PROJECT NEEDS

CANDIDATE PARTS

EVALUATION

RISK MITIGATION

IDENTIFY

RECOMMEND

PERFORM

IMPLEMENT

JET PROPULSION LABORATORY
Electronic Parts Engineering Office
Off-The-Shelf Part Tradeoffs

- **Hi Reliability SCD**
- **Hi Reliability Class S**
- **KGD**
- **COTS**
- **Military**

$ & T Increases, Risk Decreases With Evaluations & Upscreens

Cost of Acquisition($) vs Schedule of Availability(T)
A COTS Methodology for Evaluating Parts

- Define critical part criteria for evaluation
- List the best risk indicators for the part type
- Gather data for each indicator with minimum $
- Augment part data when necessary (+$)
- Find mitigating solutions for the high risk indicators
- Perform final part risk assessment for the application
COTS Evaluations That Can Cost Little:

- Process
- Reliability
- Quality
- Package
- Performance

COTS Evaluations That Can Cost More:

- DPA
- Test/Burn-In
- Radiation
Examples of Risk Indicators & Their Relative Costs for a Plastic Package:

- Temperature Humidity
- Temperature Cycling
- Moisture Absorption
- Radiation
- Outgassing
- Glass Transition

Corrosion ($)
Assembly Defects ($)
Popcorning ($$)
TID Degradation ($$$$
Condensables ($$
Stability ($$)
Criteria Selected for Risk Assessment of Flash Memory

<table>
<thead>
<tr>
<th>List of criteria used for COTS</th>
<th>Current Status</th>
<th>Evaluation</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Vendor</td>
<td>Information Complete</td>
<td>Accept</td>
</tr>
<tr>
<td>2. Part</td>
<td>Information Complete</td>
<td>Accept</td>
</tr>
<tr>
<td>3. Wafer Fab Technology</td>
<td>Partial Information Received</td>
<td>Accept</td>
</tr>
<tr>
<td>4. Design</td>
<td>No Information Available</td>
<td>Unknown</td>
</tr>
<tr>
<td>5. Reliability Assurance</td>
<td>Partial Information Received</td>
<td>Warning</td>
</tr>
<tr>
<td>6. Quality Assurance</td>
<td>No Information Available</td>
<td>Unknown</td>
</tr>
<tr>
<td>7. Testing</td>
<td>No Information Available</td>
<td>Unknown</td>
</tr>
<tr>
<td>8. Screening</td>
<td>No Information Available</td>
<td>Unknown</td>
</tr>
<tr>
<td>9. Performance</td>
<td>Partial Information Received</td>
<td>Accept</td>
</tr>
<tr>
<td>10. Package</td>
<td>Partial Information Received</td>
<td>Warning</td>
</tr>
<tr>
<td>11. Radiation</td>
<td>Partial Information Received</td>
<td>Unknown</td>
</tr>
<tr>
<td>12. Known Good Die</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>13. JPL Chip Overview</td>
<td>Information Complete</td>
<td>Accept</td>
</tr>
<tr>
<td>14. JPL DPA (Package)</td>
<td>Information Complete</td>
<td>Accept</td>
</tr>
<tr>
<td>15. JPL DPA (Die Cross Section)</td>
<td>Information Complete</td>
<td>Accept</td>
</tr>
<tr>
<td>7a. JPL Testing/Burn-In</td>
<td>Information Complete</td>
<td>Warning</td>
</tr>
</tbody>
</table>
## Risk Indicators Selected for Reliability Assurance

**A. Infant Mortality**

**B. Dynamic Life**

**C. Program Erase Cycle**

<table>
<thead>
<tr>
<th>Vendor's Data</th>
<th>Information Received</th>
<th>For JPL Use Only (Quality/Risk Evaluation)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>A.</strong> Ten lots were tested at 6.5V and 125C. Results are 0/2002 after 48 hrs. and 0/2002 after 168 hrs. Intel Report 12/29/95.</td>
<td>X</td>
<td><strong>Unknown</strong></td>
</tr>
<tr>
<td><strong>B.</strong> Four lots were tested at 6.5V and 125C. Results are 0/249 after 500 hrs. and 2/249 after 1000 hrs. 2 rejs are lccs due to gate oxide breakdown. Intel Report 12/29/95.</td>
<td>X</td>
<td><strong>Low risk (1 failure out of 50K cyc.)</strong></td>
</tr>
<tr>
<td><strong>C.</strong> Four lots were tested at 0C at 100cyc.; 1K cyc.; 5K.; 10K.; and 50K. Results are 1/530 at 15,010 cycles. There were no additional failures when tested at 70C. Intel Report 12/29/95.</td>
<td>X</td>
<td></td>
</tr>
</tbody>
</table>
COTS Work- Plan/Status

Completed:
- Plastic Packages
- Part Family Evaluations
- LPSEP

In Progress:
- Vendor Surveys
- Outgassing
- A/D & D/A
- Flash Memory
- Characterization
- Reliability
- Radiation

Planning:
- Known Good Die
- Vendor Screens
- User Risk
- Radiation
- Logic
- Delamination
- Others

In Progress:
15
COTS Work- KGD Vendors Reviewed:

MCM Assemblies Rely on KGD for Meeting Their Operational Requirements

- National Semiconductor
- Intel
- Motorola
- Elmo Semiconductor *
- Harris Semiconductor
- Hamilton Hallmark *
- Texas Instruments
- Micron Technology
- Linear Technology
- Maxim
- Others

* Distributors - Hamilton Hallmark is a distributor that offers die solutions for the Commercial & Military World - Program is called “DiePro℠”
COTS Work- MCM Risk
Assumptions

- MCM Yield (with die) = Die yield \( \times \text{No. of die Vendor A} \)

- A MCM yield of 1.0 means the die are tested to the same level as the package part for quality, reliability, and performance --> (KGD)

- The MCM assembly yield (w/o die) is assumed equal to 1.0

- Rework of MCMs due to faulty die is costly, hard to trouble shoot, and causes delay in schedules - it should be avoided

- Vendors who supply KGD offer many screening options
Illustration of MCM Risk of Failure vs KGD Upscreen Level

Note: Die yield=88% @ L1
COTS Work - Popcorning of PEM SMDs

- High Temperature Applied
- Internal Stress Buildup
- Cracks Form (Popcorning)
COTS Work - Moisture Absorption of Flash Memories in Plastic

Packages that exhibit > 0.1% relative weight gain within the 1st 100 hours of test are extremely moisture sensitive and likely to cause popcorning unless drying precautions are in place.
All four packages passed specification of (TML = 1.0% ; CVCM = 0.1%).

<table>
<thead>
<tr>
<th>Material</th>
<th>MCR</th>
<th>761238FBA, E24, DA28F016SV, K8055, U6240332</th>
<th>AM28F020-150PC, 9618FBB</th>
<th>CSI, CAT28F020F, 1-15 09550B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Part</td>
<td>Motorola SCR</td>
<td>Intel 16 M Flash Memory</td>
<td>AMD 2M Flash Memory</td>
<td>Catalyst 2M Flash Memory</td>
</tr>
<tr>
<td>Sample No.</td>
<td>5</td>
<td>6</td>
<td>avg</td>
<td>7</td>
</tr>
<tr>
<td>WT. Loss %</td>
<td>0.45</td>
<td>0.46</td>
<td>0.45</td>
<td>0.23</td>
</tr>
<tr>
<td>Water Vapor Recovered, WVR</td>
<td>0.28</td>
<td>0.25</td>
<td>0.26</td>
<td>0.14</td>
</tr>
<tr>
<td>%TML (WT, LOSS- WVR)</td>
<td>0.17</td>
<td>0.21</td>
<td>0.19</td>
<td>0.09</td>
</tr>
<tr>
<td>CVCM %</td>
<td>0.04</td>
<td>0.08</td>
<td>0.06</td>
<td>0.02</td>
</tr>
<tr>
<td>DEPOSIT on CP</td>
<td>Opaque</td>
<td>Negligible</td>
<td>Opaque</td>
<td>Opaque</td>
</tr>
<tr>
<td>FTIR Results</td>
<td>Amine cured epoxy</td>
<td>Anhydride cured epoxy</td>
<td>Amine cured epoxy</td>
<td>Amine cured epoxy</td>
</tr>
</tbody>
</table>
COTS Work - Radiation Levels

<table>
<thead>
<tr>
<th></th>
<th>Commercial Part</th>
<th>Rad-Tolerant Part</th>
<th>EPI CMOS Part</th>
<th>SOI CMOS Part</th>
<th>Rad-Hard Part</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hardness Limited by</td>
<td>Hardness offered as a by-product of the design &amp;</td>
<td>Hardness offered as a by-product of the design &amp; process</td>
<td>Hardness offered as a by-product of the design &amp; process</td>
<td>Hardness offered as a by-product of the design &amp; process</td>
<td>Designed &amp; processed for specific hardness level</td>
</tr>
<tr>
<td>inherent process and</td>
<td>process</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>design; customer’s risk</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Total Dose</strong></td>
<td>2 krad to 10 krad (typical)</td>
<td><strong>Total Dose</strong> : 20 krad to 50 krad (typical)</td>
<td><strong>Total Dose</strong> : &gt; 50 krad (typical)</td>
<td><strong>Total Dose</strong> : &gt;100 krad (typical)</td>
<td><strong>Total Dose</strong> : &gt;200 krad to 1 Mrad or more (typical)</td>
</tr>
<tr>
<td><strong>SEU</strong> : threshold LET:</td>
<td>5 MeV/mg/cm² (typical)</td>
<td><strong>SEU</strong> : threshold LET: 20 MeV/mg/cm² (typical)</td>
<td><strong>SEU</strong> : threshold LET: 30 MeV/mg/cm² (typical)</td>
<td><strong>SEU</strong> : threshold LET: 120 MeV/mg/cm² (typical)</td>
<td><strong>SEU</strong> : threshold LET: 80-150 MeV/mg/cm² (typical)</td>
</tr>
<tr>
<td><strong>SEU error rate</strong></td>
<td><strong>SEU error rate</strong> : 10E-5 to 10E-8 errors/bit-day (typical)</td>
<td><strong>SEU error rate</strong> : 10E-9 to 10E-10 errors/bit-day (typical)</td>
<td><strong>SEU error rate</strong> : 10E-9 to 10E-10 errors/bit-day (typical)</td>
<td><strong>SEU error rate</strong> : 10E-9 to 10E-12 errors/bit-day (typical)</td>
<td><strong>SEU error rate</strong> : 10E-10 to 10E-12 errors/bit-day (typical)</td>
</tr>
<tr>
<td><strong>Latchup</strong> : Customer</td>
<td><strong>Latchup</strong> : Customer evaluation and risk</td>
<td><strong>Latchup</strong> : Varies by process and EPI thickness</td>
<td><strong>Latchup</strong> : Eliminated</td>
<td><strong>Latchup</strong> : Eliminated</td>
<td><strong>Latchup</strong> : SOS, Bipolar Technologies; Eliminated</td>
</tr>
<tr>
<td>evaluation and risk</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Guarantees: None</td>
<td>Guarantees: None</td>
<td>Guarantees: None</td>
<td>Guarantees: None</td>
<td>Guarantees: None</td>
<td>Guarantees: High</td>
</tr>
</tbody>
</table>
TID Response of Intel 16M Flash Memory In Plastic Package

- Erase Time of 32 Blocks (secs)
- Total Dose (Krads)

- 85C/85%RH
- No Precond.
- 100C Bake for 44 hr.
COTS Work- Reports

Published
• PCA for Intel DA28F016SV
• Part/Package Analysis for Intel DA28F016SV
• Part/Package Analysis for AMD AM28F020
• Part/Package Analysis for Catalyst CAT28F020P
• Electrical Performance for Intel DA28F016SV with Temperature
• Burn-In Results for Intel DA28F016SV

In Writing:
• Total Dose for Intel DA28F016SV
• Moisture Absorption/Desorption for Plastic Packages
• Outgassing Characteristics for Plastic Packages
• Methodology & Criteria for Risk Assessment of COTS Parts
COTS Work- 507 Data Base

UTILITIES:

DATA (Parts, Vendors, Surveys, etc.)

INFORMATION (Generic, Plastics, KGD, etc.)

ASSESSMENT (Parts, Technology, etc.)

ANALYSIS (DPA, CA, SEM, etc.)

TOOLS (what if analysis for KGD yield, etc.)

FORMATS:

EXCEL, WORD, PDF, HTML, PowerPoint
In Summary

- Using COTS parts without understanding their pedigree can lead to mission delay or worst mission failure.

- A methodology is in place in Office 507 to help JPL users of COTS parts ascertain their risk and acceptance for Space Application.

- Work is underway in Office 507 to evaluate all risk factors of using COTS parts (quality, reliability, radiation, package, and device performance).
For Further COTS Information Contact:

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