

VI. PIN Diodes

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Although PN junctions are the workhorse of Si circuit designs, GaAs PN junctions did not develop as a viable device. The primary reason for this is the much lower hole mobility compared to the electron mobility for GaAs, whereas in Si the difference in mobility is not as great. The resulting low hole drift velocity limits the maximum frequency of GaAs p-type devices, and since GaAs is primarily used for high-frequency and high-speed circuits, GaAs PN junctions were not developed. Unfortunately, without the need or desire for GaAs PN junctions, p-type GaAs ion implantation and MBE growth were not developed and integrated into GaAs circuit production facilities. As a result, GaAs PIN (p-type–insulator–n-type) diodes were not available to MMIC designers. The unavailability of MMIC PIN diodes was unfortunate because they have fast switching speeds, high breakdown voltage, and a variable resistance with bias. These positive characteristics may be used in the design of high-power switches [1], variable attenuators [2], photo detectors, and variable-gain amplifiers [3].

The unavailability of GaAs p-type regions changed with the recent advent of the GaAs HBT MMIC. With the good performance of these HBTs, p-type ion implantation and MBE growth are now being incorporated into GaAs production facilities. By using the p^+ base layer, the n^- collector region, and the n^+ collector ohmic contact layer of the HBT as shown in Figure 3-21, MMICs with PIN diodes can now be made easily on an GaAs HBT fabrication line. Since the emitter of the HBT is not used, the diode is strictly a GaAs device.

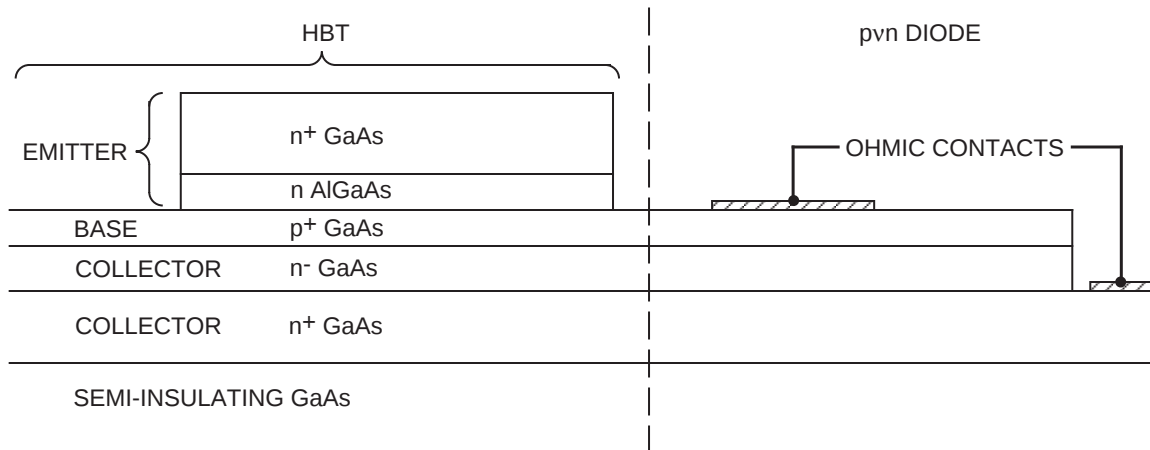


Figure 3-21. pvn fabrication from HBT structure.

A. Device Physics

Ideally, a PIN diode would have a perfect insulator between the p-type and the n-type regions. Although semi-insulating GaAs would be a good insulator, as already shown in Figure 3-21, the p and n regions of practical diodes are separated by a lightly doped n or n^- region. This n^- region is referred to as a v region and the resulting diode as a pvn diode. If a p^- region were used instead, the diode would be referred to as a $p\pi n$ diode. Throughout this section, the pvn diode will be presented. The extension to the $p\pi n$ diode is straightforward.

(a) 



junction, but unlike the metal–semiconductor junction, depletion regions are formed on both sides of the junction. This is shown in Figure 3-22(b). Because the total charge in the p^+ depletion region must equal the total charge in the v depletion region or $W_p N_A = W_v N_D$, the depletion width in the v region will be greater. Usually, $W_v \gg W_p$ and the total depletion region may be approximated as W_v . In this sense, the metal–semiconductor model may be used where the p^+ and the n^+ regions can be considered as metal electrodes and the depletion width and junction capacitance are determined by Equations (3-2) and (3-4) in Section 3-II. The equivalent circuit for the unbiased diode is also shown in Figure 3-22(b). R_C is the total resistance of the n^+ and p^+ ohmic contacts, $R_v = \rho L/A$ is the resistance in the v region, $C_v = \epsilon A/L$ is commonly called the diffusion capacitance and accounts for charge storage in the undepleted v region, $C_j = \epsilon A/W_v$ is the depletion region capacitance, A is the area of the diode, W_v is the depletion width, W is the v region width, and ρ is the resistivity of the v region. In general, R_C is constant, but C_j , C_v , and R_v are bias dependent.

If a reverse bias is applied to the junction, $V < 0$, the depletion width will increase. If a large enough reverse bias is applied, the depletion width will extend across the v region. The potential at which $W_v = W$ is called the punch-through potential and is commonly specified as V_{PT} . Once the punch-through potential has been reached, R_v reduces to a very small value, C_v increases to a large value, and C_j is approximately $\epsilon A/W$. Since the parallel combination of R_v and C_v can now be approximated by a short circuit, the reversed biased diode may be approximated by R_C and C_j , both of which are constant. The reverse bias potential required for punch through is given by:

$$V_{PT} = \frac{qN_d W^2}{2\epsilon_r \epsilon_0} \quad (3-22)$$

It is seen that if a perfect insulator were used in the PIN diode, $V_{PT} = 0$. Although this is rarely the case, V_{PT} can still be small. For example, if a pvn diode were made from the HBT structure shown in Figure 3-17 of Section 3-V, V_{PT} would be approximately 5 V. The punch-through potential is important since the diode has its greatest reverse-biased impedance when $V_{RB} > V_{PT}$. Therefore, for switching applications, the diode is always driven into punch through and can be modeled as shown in Figure 3-22(c). By designing the diode so that C_j is small, the impedance of the reverse-biased diode will be large. This is required for switching applications since a large reverse-biased impedance results in good isolation. Therefore, a small A/W ratio is desired for switch applications.

If the diode is forward biased, the depletion width decreases and the junction capacitance increases to a large value. For most applications, the impedance resulting from C_j is small and the element can be ignored. The forward bias also causes electrons to be injected into the v region from the n^+ contact and holes to be injected into the v region from the p^+ contact. This increase in carriers causes the resistivity of the v region to decrease. Since the amount of charge injection is dependent on the bias potential, the forward-biased impedance is bias dependent. Using Equation (3-6) of Section 3-II, R_v may be written as [2]

$$R_v = \frac{nkT}{qI_F} \quad (3-23)$$

where I_F is the forward current and n is the ideality factor. Similarly, C_v may be written as [2]

$$C_v = \frac{\tau}{R_v} \quad (3-24)$$

where τ is the carrier transit time in the v region. If one writes the impedance for the capacitor, C_v , as

$$Z_{Cv} = \frac{R_v}{j\omega\tau} \quad (3-25)$$

it is seen that the ratio of the impedance associated with C_v to R_v can vary from values less than one to greater than one, depending on the product of ω and τ . Therefore, in general, the forward-biased diode is modeled as shown in Figure 3-22(d). For switching applications, the diode will be driven hard to decrease the forward impedance. Under strong forward drive, GaAs pvn diodes fabricated from HBT structures have impedances from 3 to 5 ohms.

The preceding development of the equivalent circuit models is valid for most applications. For some applications, though, a parasitic capacitance, C_p , which shunts the entire device, must be added to account for fringing fields from the two device contacts. The value of C_p depends on the diode design. For example, if the diode is designed in a circular shape, the fringing fields will be small. For diode structures designed on HBT production lines, it has been reported that $C_p > 2 C_j$ [2]. Therefore, the diodes reverse-biased impedance may be significantly lower than predicted, and switching performance may be severely degraded.

B. Reliability

The reliability of PIN diodes fabricated in HBT production lines has not been well addressed. It is anticipated that the diode will share some of the same reliability concerns as the HBT with the exception of the emitter contact and the base-emitter junction failure mechanisms. The main reliability concern with PIN diodes is that they are typically used in high-power applications such as switching circuits. Therefore, they are often subjected to large electric fields as well as elevated temperatures.

Reliability concerns for the PIN diode arise when large forward or reverse biases or RF signals are applied. Consider first the forward-biased diode. The diode has a low impedance that permits a large current to flow across the device and an associated large I^2R loss. Since GaAs is a poor thermal conductor, the power loss causes the temperature to increase, which in turn may create thermal related failures such as metal–semiconductor diffusion. Since the p^+ region of the diode is approximately $0.1 \mu\text{m}$ thick, ohmic contact diffusion through the p^+ region is a primary concern. In addition, diffusion of ions from the p^+ and n^+ contacts into the n region will be accelerated at increased temperatures causing changes in the diode's electrical characteristics.

When the diode is reverse biased, the critical parameter that must be controlled is the electric field across the device. The electric field is given by

$$E = \frac{V_{RB}}{W} \quad (3-26)$$

If $E > 4 \times 10^5$ V/cm and W is sufficiently large to permit carrier-atom collisions, avalanche breakdown results with the possibility of catastrophic device failure. For GaAs, the maximum reverse bias that may be applied is given by

$$V_{RB} = 40W \quad (3-27)$$

where W is in microns. This limitation of V_{RB} sets the lower limit on W . Recall that a large W gives a smaller C_j and therefore better switch isolation. Therefore, it may appear that W should be made large. The disadvantage of this is that the switching speed of the diode is related to the time it takes to sweep all of the injected carriers out of the forward-biased n region, and this is directly related to the width W . The tradeoffs between fast switching speed, large power handling capabilities, and large switch isolation normally would be made by the PIN-diode designer. When the diodes are integrated with or fabricated with HBT circuits, the HBT performance must also be included in the tradeoff analysis.

References

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