Chapter 4. Basic Failure Modes and Mechanisms

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Failures of electronic devices, in general, can be catastrophic or noncatastrophic. Catastrophic failures render the device totally nonfunctional, while noncatastrophic failures result in an electrically operating device that shows parametric degradation and limited performance.

This chapter provides a description of some of the more common failure modes and mechanisms affecting GaAs-based MMICs. The current understanding of the topic will be presented along with a discussion of some possible solutions, practiced process improvements, and references.

I. General Failure Modes

GaAs devices exhibit some general failure modes that can be attributed to a defined failure mechanism. The most common failure modes are observed via degradation of the MMIC parameters such as I_{DSS}, gain, P_{OUT}, and others. The degradation observed in MMIC devices is normally a function of the material interactions and the environmental conditions during test or operation. The importance of a particular parameter degradation depends greatly on the design and function of the MMIC and the relationship between the observed degradation and the general health of the device in question. A list of the most common failure modes is provided in Table 4-1. Life tests, with RF or dc excitation and performed under controlled conditions, are the most common means of failure-mode detection. These tests can provide valuable information as to the type of degradation to which the particular device under test may be most susceptible, and the severity of the effect on the performance of the device.

Table 4-1. Common MMIC failure modes.

Failure Mode	Method of Detection	Related Failure Mechanisms	Possible Solutions
Degradation in I_{DSS}	Life test, operation	Gate sinking, surface effects, hydrogen effects	Derating criteria, temperature control, environmental control
Degradation in gate leakage current	Life test, high-temperature storage test, high-temperature reverse bias	Interdiffusion	Temperature control, gate current control, proper passivation
Degradation in V_P	Life test, operation	Gate sinking, hydrogen effects	Temperature control, use of stable barrier materials, environmental control
Increase in R_{DS}	Life test, operation	Gate sinking, ohmic contact degradation	Temperature control, use of stable barrier materials
Decrease in P_{OUT}	Life test, operation	Surface effects, hydrogen effects, gate sinking	Temperature control, use of stable barrier materials, environmental control

While dc testing is much easier and more cost effective to implement, RF testing has the advantage of providing the user with direct information in regard to device degradation under conditions similar to those of the actual application. Correlation between the results of dc tests and actual RF application has been a topic of great interest and debate in the GaAs reliability community, but to date there is little understanding or agreement of the relationship.

A. Degradation in I_{DSS}

This failure mode is one of the most common and easiest to detect. Accelerated life tests have been used to provide an estimation of the lifetime of devices based on the observed level of I_{DSS} degradation. Various failure mechanisms can be attributed to be the cause of this observed degradation. One of the most common is referred to as "gate sinking." In this mechanism, a reduction in the active channel of the device results in a decrease of I_{DSS} among other parameters. Another common mechanism, which can cause similar degradation, is referred to as "hydrogen poisoning." This mechanism is theorized to cause a decrease in the donor density in the channel, which in turn causes a reduction in I_{DSS} [1]. A detailed discussion of failure mechanisms will be presented in Section II.

B. Degradation in Gate Leakage Current

This failure mode is generally observed in devices subjected to an accelerated life test or to high operating temperatures. The degradation is observed as an increase in the gate leakage current over the duration of the test. No experimentally identified failure mechanisms have been linked to this failure mode, but surface-state effects have been suspect.

C. Degradation in Pinch-Off Voltage

Pinch-off voltage (V_p) degradation is another common failure mode for GaAs devices. This degradation results primarily from metal–semiconductor interactions and instability of gate-metal structures. The degradation is normally observed on devices subjected to accelerated life tests or high-temperature operation. Reliability related effects of metal–semiconductor interactions may render the associated barrier layers ineffective due to poor manufacturing practices or material choices. The choice of the appropriate barrier material to limit Au/GaAs interdiffusion is the best method to limit the effects of this degradation.

Hydrogen-related degradation may cause the same observed pinch-off voltage degradation effects [1]. This degradation is theorized to be caused by either a reduction of carrier concentration in the active channel of the device or a change in the surface state built-in potential. Further information on this degradation is found in Section II.D.2.

D. Increase in Drain-to-Source Resistance

The increase in the drain to source resistance (R_{DS}) can be attributed to either gate sinking or to ohmic contact degradation. Both of these failure mechanisms are metal–semiconductor related degradation mechanisms that are accelerated with temperature.

Therefore, devices subjected to accelerated life tests or operation at elevated temperatures generally exhibit this degradation.

E. Degradation in RF Performance

Various RF parameters can exhibit degradation over the lifetime and operation of the devices. Although it is very difficult to extrapolate RF performance from dc test data, some manufacturers use particular dc parameters as predictors of resultant RF performance. I_{DSS}, for example, can be used as a predictor of saturated power performance, while g_m can be used for prediction of gain and noise figure degradation in small-signal and low-noise devices.

The causes of RF parameter degradation vary, depending on the technology and operating conditions of the devices under test. In general, surface-state density and resultant surface effects play a role in overall RF device performance and stability over time. Material interaction effects also play a major role in long-term device performance. Other factors, such as hydrogen-related degradation and other environmental effects, can also contribute to the overall degradation.

II. Failure Mechanisms

Failure mechanisms of electronic semiconductor devices can be divided into the following general categories:

(1) Material-interaction-induced mechanisms.
(2) Stress-induced mechanisms.
(3) Mechanically induced failure mechanisms.
(4) Environmentally induced failure mechanisms.

Material-induced mechanisms can in turn be subdivided into two general categories, the first being semiconductor die material and metal interactions, and the second being a result of die packaging and interconnect. Stress-induced failure mechanisms can be directly attributed to either poor device design or poor and careless device application. Environmentally induced failure mechanisms can cover a wide spectrum of possible environmental conditions, such as humidity and hydrogen effects.

Reported device-failure mechanisms can be a result of one or a combination of these factors. Therefore, care must be exercised in understanding the operating and environmental conditions and process variables associated with the reported failure. Table 4-2 shows the main areas of responsibility for the failure-mechanism categories. In this chapter, a discussion of the general categories of failure mechanisms will be provided, along with reference examples as applicable.

A. Material-Interaction-Induced Failure Mechanisms

GaAs processes involve a number of metal–semiconductor interfaces which, if not designed and applied properly, may cause device degradation and failure. The two main metal–semiconductor interfaces in GaAs-based devices are the Schottky gate contact and the ohmic source and drain contacts. The common metallization structures for GaAs are based on the industry standard Au/Pt/Ti or Au/Pd/Ti on GaAs. The thermal

Table 4-2. General responsibilities for the failure-mechanism categories.

Failure Mechanism Category	Manufacturer Control	User Control
Material-interaction induced		
Stress induced		
Mechanically induced		
Environmentally induced		

stability and reproducibility of Schottky barriers, the correct choice of metals and their applicable processing parameters, and the GaAs surface conditions all play a role in the reliability of the produced structures and the applicable failure mechanisms. Failures related to Schottky and ohmic contacts occur when the metals diffuse into the semiconductor, and the Ga and/or As diffuse into the contact. A description of the failure mechanisms related to these interfaces will be provided along with relevant examples.

1. Gate-Metal Sinking

The performance of GaAs-based devices relies heavily on the quality of the active channel area of the device. The Schottky gate metal-to-semiconductor interface directly influences the device electrical parameters, such as the drain saturation current and reverse breakdown. The gate structures are based on the industry standard mutilayer Au/Pt/Ti or Au/Pd/Ti on GaAs. Interdiffusion of gate metal with GaAs results in a reduction of the active channel depth and a change in the effective channel doping. This effect is termed as "gate sinking." This process is affected by the surface conditions of the GaAs material at the time of deposition, the deposition parameters, and the choice of deposited materials.

This failure mechanism is generally observed after exposure to an accelerated life test or operation at elevated temperatures, the driving factor for this mechanism being the thermally accelerated diffusion of Au into GaAs. The common gate metallization structure consists of three layers. The first layer contacting GaAs is a thin Ti layer used primarily for adhesion. The second layer is either Pd or Pt. This layer is used as a barrier to Au diffusion into GaAs. The last layer is thick Au used for conduction. The rate of Au gate-metal diffusion into the GaAs is a function of the gate-metal material diffusivity, the temperature , and the material-concentration gradient. For perfect lattice structures, the diffusion rate at normal operating temperatures is too slow to have an effect on device performance. However, when large grain boundaries or large numbers of surface defects exist, the diffusion rate can be fast [2].

Au has a high diffusion factor into GaAs, therefore a Pt or Pd layer is employed to act as a barrier to Au diffusion into GaAs. Grain boundaries in the barrier layer may allow a diffusion path for Au, which in turn may cause device degradation. The inclusion of some oxygen or nitrogen in the barrier films helps reduce the grain boundary diffusion of Au through the films. Other poor manufacturing processes or material quality may render the barrier layer useless. Several examples of Au interaction with GaAs through different barrier layers have been reported in the literature [3,4,5].

2. Ohmic Contact Degradation

The most common system for ohmic contacts is AuGe/Ni, which is alloyed into the GaAs at temperatures in excess of 400°C to provide the necessary low contact resistance (0.1 to 0.5 /mm). A thick Au layer is then deposited on top of the alloyed contacts to provide conduction. This structure, employed at the drain and source contacts, has been shown to degrade at elevated temperatures. The degradation is the result of Ga outdiffusion into the top Au layer and the diffusion of Au into the GaAs causing an increase in the contact resistance [6]. The Ni layer used in the ohmic contact is intended as a Au- and Ga-diffusion barrier. Some other materials such as Cr, Ag, Pt, Ta, and Ti have been used as barrier materials with varying degrees of success. The activation energy associated with ohmic contact degradation varies between 0.5 eV and 1.8 eV [7,8]. This activation energy may provide reasonable contact life at low operating temperatures (< 100°C) but it also indicates rapid deterioration at elevated temperatures (>150°C) [9].

The general understanding of ohmic contacts attributes the degradation to the following :

(1) Ga outdiffusion into the Au layer, which creates a nonstochiometric defect-rich region of high resistivity under the contact. This effect is reduced by employing a barrier layer sandwiched between the AuGe and the Au conduction layer [10].

(2) Indiffusion of Au and Ni into the GaAs, which can cause a reduction in the doping concentration in the active channel of the device [6,7].

(3) The formation of various intermetallic phases such as AuGa and Ni_2AsGe as a result of the alloying process.

Sputter cleaning of the surface prior to deposition along with deposition of Ni as a first layer can provide for much improved ohmic contact stability and homogeneity [11]. Continuous or noncontinuous contamination at the deposition surface by oxides or other contaminants can result in regions of high resistance. The NiAs(Ge) phase is essential for low contact-resistance values, because it satisfies the condition that the Ge atoms diffuse into the Ga vacancy sites forming a heavily doped n^+ layer at the metal/GaAs interface.

Results of recent accelerated life tests confirm that the stability of AuGeNi alloyed ohmic contacts does not appear to be a major reliability concern under normal operating conditions. However, as the gate and gate-drain/source dimensions of high speed devices shrink, vertical spiking and lateral spreading during the alloying process will not allow good dimensional control of alloyed contacts such as AuGeNi [12]. To overcome this limitation, new ohmic contacts have been developed utilizing low temperature anneal of an epitaxially grown thin layer of Ge on GaAs. Another approach is to grow an epitaxial n^+ Ge layer on n-GaAs followed by deposition of a refractory metal layer. Deposition of small amounts of In along with W contact metal and annealing using rapid thermal anneal techniques have also been used.

3. Channel Degradation

Degradation observed in device parameters can sometimes be attributed to changes in the quality and purity of the active channel area and a reduction in the carrier concentration beneath the gate Schottky contact area. These changes have been

postulated to be a result of diffusion of dopants out of the channel or diffusion of impurities or defects from the substrate to the channel [13]. Deep level traps have also been speculated to cause similar degradation in MESFETs.

HEMT devices, being strongly dependent on the properties of the interface of the AlGaAs/GaAs heterostructure, can suffer a related failure mechanism. A decrease in electron concentration in the channel, caused by a deconfinement of the 2DEG, was postulated to be the cause of the observed failure mechanism [14].

HEMT devices can also suffer from metal-diffusion-related mechanisms, which are manifested as channel-related degradation. Lateral diffusion of Al into the gate recess region changes the conduction band discontinuity and consequently the confinement of the channel electrons. Gold diffusion from the ohmic contact into the active channel region under the gate can also cause similar degradation. Lastly, vertical diffusion of Al from the AlGaAs donor layer and Si from the n^+ AlGaAs layer into the channel layer causes an increase in the impurity scattering in the undoped GaAs, thus deteriorating the high electron mobility of the 2DEG [15].

4. Surface-State Effects

The performance of GaAs-based devices depends highly on the quality of the interface between metal and GaAs or the passivation layer (Si_3N_4 or SiO_2) and GaAs. The quality of the interface can depend on the surface cleaning materials and procedures, the deposition method and conditions, and the composition of the passivation layer. The main effect of an increase in surface state density, as illustrated in Figure 4-1, is the

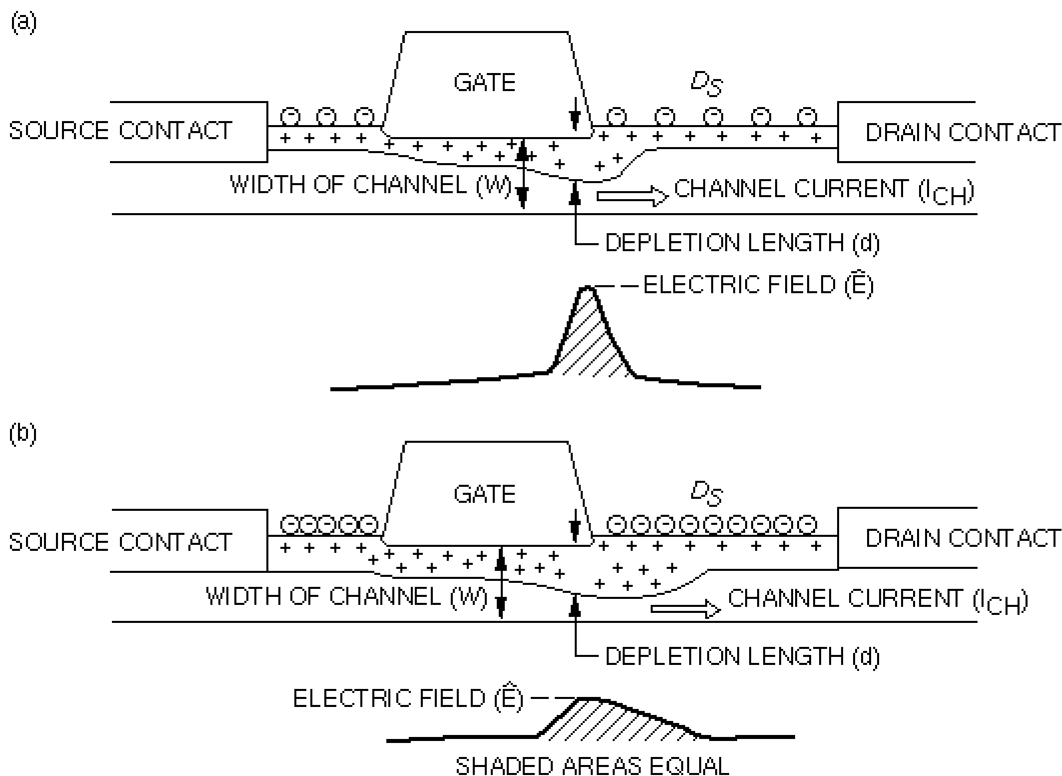

Figure 4-1. Schematic cross section of a MESFET with different surface charges. The gate-drain bias is the same for the two cases: (a) with low density of surface states D_s and (b) with high density of D_s. (From [12]; reprinted by permission of John Wiley & Sons, Ltd.)

lowering of the effective electric field at the drain/gate region, which results in an increase in the depletion region and a change in the breakdown voltage [16].

Unpassivated devices can be susceptible to surface oxidation and loss of arsenic, which may result in an increase in gate leakage current and a reduction of the breakdown voltage. Devices passivated using SiO_2 may experience surface erosion due to the interaction of SiO_2 with GaAs. The use of Si_3N_4 provides a much improved passivation layer with no GaAs surface erosion and a reduced level of arsenic loss. Plasma deposited Si_3N_4 also provides lower tensile stress compared to CVD SiO_2 passivation layers and therefore a reduced effect on surface states.

Surface-state density has a direct effect on the performance of GaAs-based devices. The reduction in the surface-state density at the Si_3N_4/GaAs interface caused by thermal treatments may result in degradation in breakdown voltage, which in turn may give rise to device burnout.

B. Stress-Induced Failure Mechanisms

1. Electromigration

Electromigration is the movement of metal atoms along a metallic strip due to momentum exchange with electrons. Since the mechanism is dependent on momentum transfer from electrons, electromigration is dependent on the temperature and the number of electrons. Therefore, this failure mechanism is generally seen in narrow gates and in power devices where the current density is greater than 2×10^5 A/cm^2, which is normally used as the threshold current density for electromigration to occur. This effect is observed both perpendicular to and along the source and drain contact edges and also at the interconnect of multilevel metallizations.

The metal atoms that migrate along the line tend to accumulate at grain boundaries. The accumulation of metal at the end of the gate or drain contact can create fingers of metal that can short the device. Figure 4-2 shows an example of material accumulation at one end and depletion (voids) at the other end of a drain contact. At the void location, the current density increases due to current crowding, which further increases the temperature due to resistive heating. These effects increase the rate of electromigration, which further increases the void size. Therefore, void creation is a self-accelerated, runaway process. If the void formation occurs in the gate of the device, electromigration may result in catastrophic failure due to the creation of gate open circuits. If electromigration occurs in the drain/source of a device, the voids may result in increased drain/source contact resistance and associated device degradation.

Material accumulation and void formation perpendicular to the source and drain contacts can cause hillock formation over the gate structure. This may result in shorting the gate to source or drain which may result in a catastrophic failure. Figure 4-3 shows an example of void and hillock formation perpendicular to the source and drain contacts. Electromigration problems at the interconnect have also been reported to occur at the AuGeNi interface [17].

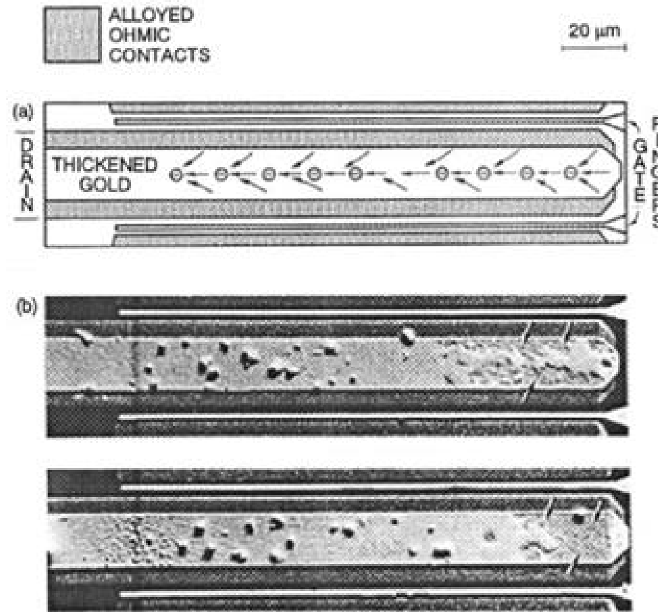

Figure 4-2. Metal-atom migration and accumulation: (a) electron wind along drain fingers; SEM images of (b) accumulation and depletion of a drain contact on a device that endured 5000 h of life testing at T_{ch} = 200°C and j = 5.3 × 105 A/cm^2. (From [12]; reprinted by permission of John Wiley & Sons, Ltd.)

It should be emphasized that electromigration failures can be avoided by limiting the current density and providing a controlled temperature of the devices during operation. Process control assuring a clean and defect-free interface structure is also essential.

2. Burnout

The partial or complete melting of a large device area resulting in catastrophic failure is referred to as burnout. This failure mechanism is considered to be the final result of a combination of other failure mechanisms causing an increase in localized power dissipation.

Burnout can be divided into two forms, "instantaneous" and "long-term." Instantaneous burnout is caused by sudden events such as electrostatic discharge (ESD), electrical overstress (EOS), and RF spikes. This failure mechanism is related more to device design and robustness than material interaction in the conventional sense of reliability.

Gate-drain burnout can be attributed to avalanche breakdown and therefore depends to a large extent on surface characteristics and device layout and technology.

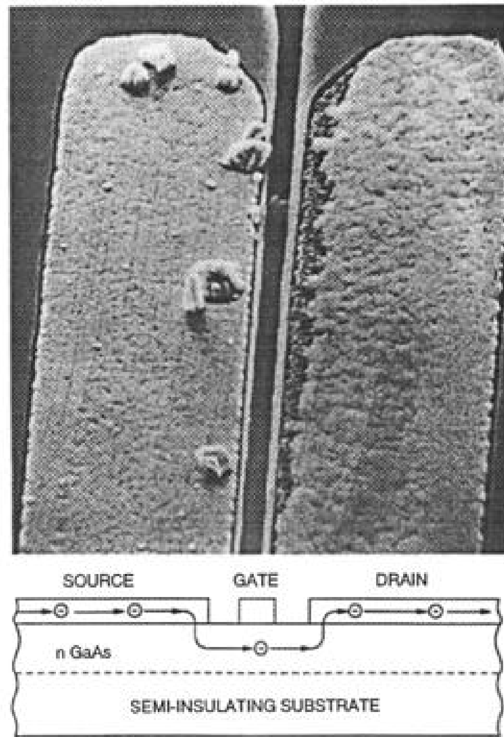

Figure 4-3. Depletion and accumulation of material in AuGeIn source and drain ohmic contacts induced by electromigration in a low-noise MESFET after life test. (From [12]; reprinted by permission of John Wiley & Sons, Ltd.)

To improve the breakdown voltage and burnout characteristics of MESFET type devices, a recessed gate design is usually implemented. Consideration of layout topology, use of an offset gate in relation to the source and drain, and careful characterization of the resultant device under various operating conditions can greatly reduce the occurrence of gate-drain burnout.

Source-drain burnout has been found to be thermally activated and has been shown to initiate at the drain contact where nonuniformities and current crowding cause local hot spots. These hot spots in turn cause a thermal runaway condition associated with the temperature coefficient of the buffer or substrate material [17]. This action has been shown to occur when the buffer and substrate materials reach local temperatures higher than 550°C, leading to a sudden increase in buffer and substrate conductivity and, consequently, in drain current.

Thermally induced metal–GaAs interdiffusion can cause a very similar failure scenario. Metal migration through the grain boundaries and crystalline defects of GaAs can reach the substrate/active channel interface causing a short between the gate or source and drain. Localized heating generated in these locations along with the positive temperature coefficient of the substrate can initiate a positive feedback mechanism in an area of high current density. Thermal runaway is consequently initiated, leading to burnout and catastrophic failure.

Long-term burnout, on the other hand, is believed to be the final result of a parametric degradation occurring during long-term aging and leading to an increased and localized power density dissipation. One of the factors that may contribute to this condition is surface effects such as oxidation reduction of GaAs and the annealing of surface states, which may cause an increase in the leakage current and reduce the breakdown voltage [17]. For example, test results show that a significant improvement is possible when silicon nitride is used instead of silicon dioxide as a passivation layer. This has been attributed to the lower tensile stress and a reduction of the effect on surface states of the plasma-deposited Si_3N_4 compared to those of CVD SiO_2.

Other factors contributing to the long-term burnout include interelectrode bridges and lateral surface metal migration causing an electrical short and, in turn, a burnout condition. Metal–semiconductor interactions resulting in vertical spikes can cause localized heating and thermal runaway conditions and, in turn, burnout.

3. Hot Electron Trapping (modified from [20,21,22])

When RF power transistors are driven into heavy gain compression in order to achieve the maximum power or efficiency, they often suffer the so-called "power-slump" problem, which shows up typically as an approximate 1-dB drop in output power over 1,000 h of RF operation. Initially, the power-slump problem was thought to be unique to GaAs devices—a problem related to metallurgical diffusion and electromigration. However, within the last few years, a hot-electron-induced gradual degradation mechanism in MESFETs was uncovered [18,19,20]. Such a degradation mechanism has been known to take place in Si MOSFET devices: Hot electrons can be trapped in the gate oxide, causing the MOSFET threshold voltage to shift. Few investigators suspected that in a GaAs MESFET, hot electrons can also be trapped in the Si_3N_4 passivation between the gate and drain, thereby decreasing the MESFET's transconductance without affecting its threshold voltage [21].

Under RF overdrive, hot electrons are generated near the drain end of the channel where the electrical field is the highest. A few electrons can accumulate sufficient energy to tunnel into the Si_3N_4 passivation to form permanent traps. These traps can result in lower open-channel drain current and transconductance, and higher knee voltage, leakage current, and breakdown voltage. Since the traps are located above the channel (see Figure 4-4), there is usually little change in the dc or small signal parameters near the quiescent point. Further, since the traps are located beside the channel, Schottky-barrier height and the ideality factor often remain constant. This selective change in device characteristics helps distinguish hot-electron effects from thermal or environmental effects. In fact, the most distinct feature of hot-electron effects is a weak or negative temperature dependence. This is because, when the channel is hotter, electrons undergo more scattering and, therefore, are less energetic.

Based on the current understanding of the degradation mechanism, work is now being concentrated on improving the device design to reduce the degradation tendency.

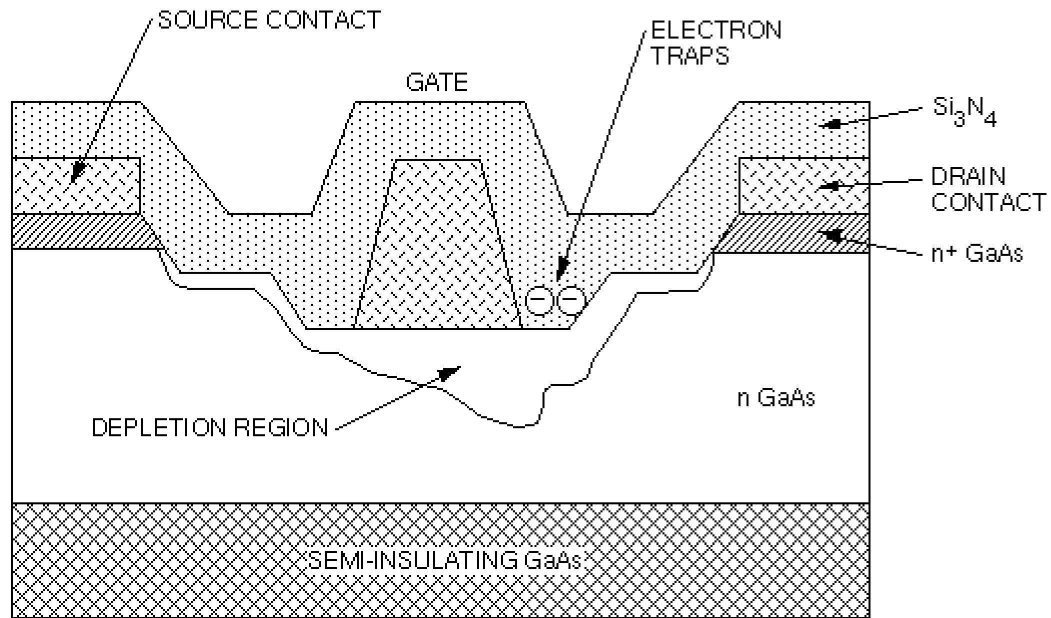

Figure 4-4. Schematic cross section of a degraded MESFET. Hot-electron-induced traps are formed in the SiN passivation layer between the gate and the drain.

This is typically done by trial and error and may take several iterations of wafer processing and device characterization. However, with improved device modeling capabilities and the use of novel measurement techniques, such as high-voltage electron-beam-induced current [22], it is now possible to optimize the shape of the electrical rather than the physical channel without many iterations. Improvement of the Si_3N_4 as a surface passivation is another obvious approach to limiting the described effects. However, perfect passivation of the GaAs surface is yet to be found. Other approaches, such as limiting the operating voltage and including a low-doped drain region as is common in a MOSFET, are either impractical or may actually contribute to further degradation in performance.

4. Electrical Stress

Electrical stress of devices during operation or handling can result in device degradation or catastrophic failure. Electrical overstress (EOS) can result from the improper application or use of the device and may result in parametric degradation or eventual catastrophic failure. Electrostatic discharge (ESD), on the other hand, can result from improper handling and lack of adequate ESD protection during transfer or test of exposed devices. The very small geometry of GaAs devices along with the semi-insulating nature of the material further enhances the sensitivity of the devices to electrostatic discharge effects.

The discharge of large electrical pulses can cause damage to both the gate and ohmic metallization structures, resulting in local melting and pursuant parameter degradation or catastrophic failure. Studies of devices exposed to noncatastrophic ESD levels have observed that MESFETs exhibited an increase in low leakage current and further catastrophic failure at RF power levels below those with no prior exposure to noncatastrophic ESD levels [23]. Other studies have also concluded that damage from

repeated exposure to an ESD level is not cumulative and that noncatastrophic damage does not degrade device lifetime [24].

Other studies have concluded that devices using the AuGeNi ohmic contact structure can exhibit ESD-related interdiffusion of the Au-based ohmic contact with GaAs. The high current densities caused by ESD can result in localized heating at the metal–semiconductor interface leading to Ga diffusion into the metallization and Au diffusion into GaAs [25]. Schottky contacts have also been found to exhibit rapid degradation under ESD stress [26]. The effect is accelerated by the small geometry and the low cross-sectional area of the gate metallization, resulting in very high current densities in response to an ESD stress event. An explosion of the gate metallization can result in response to the heat generated by the high current density; this can result in the gate metallization being physically blown out of the gate recess as shown in Figure 4-5.

Figure 4-5. Blown-out gate recess. (From [12]; reprinted by permission of John Wiley & Sons, Ltd.)

Passive MMIC elements—such as capacitors, resistors, and interconnect metallization—can also exhibit the detrimental effects of ESD. Gold-based interconnect metallization 2 μm thick has shown limited susceptibility to ESD pulses [24]. Thin-film nickel–chromium resistors, on the other hand, have shown a strong susceptibility to ESD effects as shown in Figure 4-6. The amount of ESD pulse voltage required to cause resistor damage was observed to depend on the width and thickness of the structure [24].

Metal–insulator–metal (MIM) capacitors show a strong susceptibility to ESD damage. Failures in MIM capacitors tend to occur at either the edges of the structure (Figure 4-7) where the electric field is the highest, or at the interior of the capacitor (Figure 4-8). Failures occurring at the interior of the capacitor can be attributed to dielectric defects of surface-related anomalies, while failures occurring at the edges indicate that the ESD performance is limited by the strength of the dielectric material (Si_3N_4).

Increased awareness of the effects of ESD on device reliability and the implementation of ESD precautions and controls—at all facets of device fabrication and

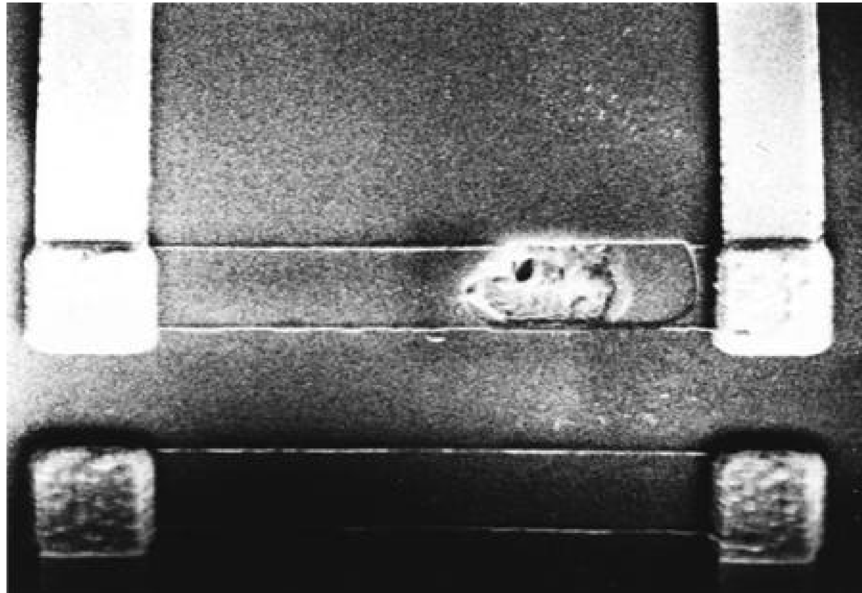

Figure 4-6. SEM photograph of a failed nickel–chromium resistor. (Courtesy of Tri Quint Semiconductor.)

test—can help eliminate this as a device-failure mechanism. If practical, ESD protection circuitry can also be implemented.

C. Mechanically Induced Failure Mechanisms

1. Die Fracture

The difference in the coefficient of thermal expansion (CTE) of GaAs, the carrier or substrate, and the package material can cause mechanical stresses in the die that may result in device failure. Tensile stresses can develop in the central region of the die, while shear stresses can develop at the edges of the die [27]. Thermal cycling either during test or operation may cause surface cracks, which are present at the center or the edges of the die, to reach their critical size and propagate across the surface, resulting in die fracture. Surface cracks can also result from an improper dicing operation, or from an improper die mounting technique.

Die surface cracks and fractures at or close to an active region of the device may result in threshold voltage shifts and general device performance degradation. An increase in leakage current at that location may result in a thermal runaway condition and ultimately catastrophic device failure.

Figure 4-7. Edge-located ESD failure of a MIM capacitor. (Courtesy of Tri Quint Semiconductor.)

2. Die-Attach Voids

Due to the relatively low thermal conductivity of GaAs, die-attach quality and uniformity across the attach surface are essential for proper device operation and reliability. Voids in the die-attach material are one of the most common causes of semiconductor-device thermal runaway and failure. The presence of voids at the edges of the die can induce high longitudinal stresses during power and environmental temperature cycling. Propagation of these voids may result in die delamination and interruption of the thermal path. Physical die detachment from the package or substrate is seldom observed as a result of void propagation.

Although voids can form from a number of sources, process control can limit the effects to an acceptable level. The package or substrate construction, the die-attach material physical properties, the cleaning and application methods, and the overall void concentration and location determine the effect of voids on device reliability [27].

D. Environmentally Induced Failure Mechanisms

1. Humidity Effects

GaAs devices packaged in nonhermetically sealed packages or plastic encapsulated packages suffer from a number of humidity-related or accelerated failure

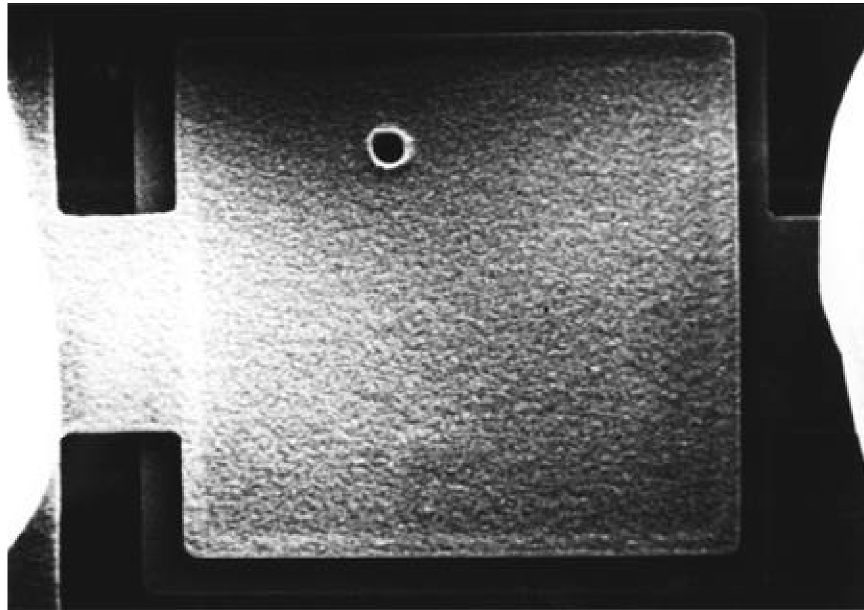

Figure 4-8. Interior-located ESD failure of a MIM capacitor. (Courtesy of Tri Quint Semiconductor.)

mechanisms. Anodic gold corrosion is the main culprit of GaAs device failures in high humidity environments where gold hydroxide ($Au(OH)_3$) has been detected in tests of GaAs ohmic contacts under high humidity conditions [28]. Ni filamentary growth, shown in Figure 4-9, has also been observed along the electric field direction of ohmic contacts adjacent to gate fingers [29].

Arsenic dissolution has also been reported as a humidity accelerated failure mechanism [29]. This effect is theorized to lead to reduction of channel thickness and degradation of device parameters such as I_{DSS} and the channel parasitic resistance.

2. Hydrogen Effects

The effect of hydrogen on the performance and reliability of GaAs devices has been reported over the last few years [30,31,32]. Degradation in I_{DSS}, V_p, g_m, and output power was observed on devices tested in hermetically sealed packages or under hydrogen atmosphere. The source of the degradation has been attributed to hydrogen gas desorbed from the package metals (Kovar, plating, etc.). The exact mechanism by which hydrogen degrades the device performance and the path by which hydrogen reaches the active area of a device are not known and have been under investigation.

Earlier research on GaAs transistors identified the diffusion of atomic hydrogen directly into the channel area of the device where it neutralizes the silicon donors as the

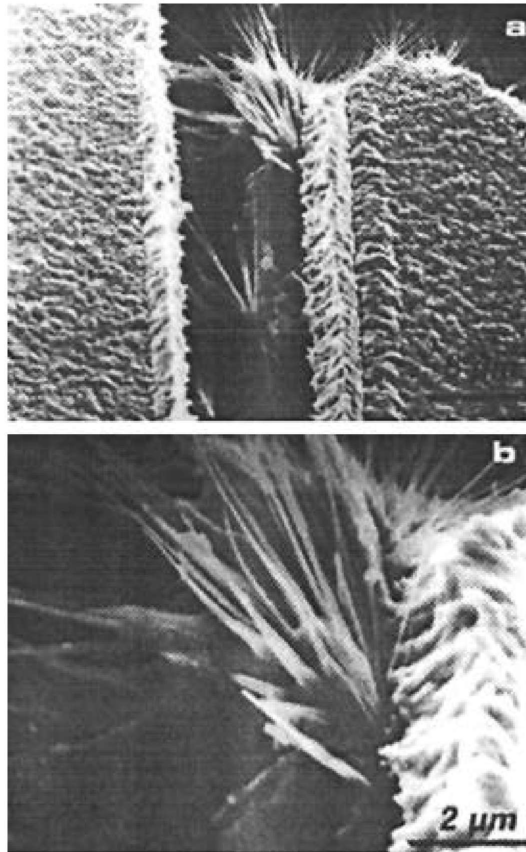

Figure 4-9. Filamentary growth: (a) nickel extrusion from the AuGeNi ohmic contact of an Au/Pd/Ti low-power MESFET passivated by Si_3N_4, submitted to an 85% RH/125°C HAST test and (b) enlarged view, evidencing dimensions of the whiskers. (From [12]; reprinted by permission of John Wiley & Sons, Ltd.)

possible mechanism [31]. It is believed that atomic hydrogen diffuses into the GaAs channel and forms Si-H, thereby neutralizing the donors. Experiments have shown that exposure of Si-doped GaAs to RF hydrogen plasma results in neutralization of the Si donors. Infrared spectroscopy data have also given evidence of $(SiAs_3)As$-H complexes [31,33].

The neutralization of donors can decrease the carrier concentration in the channel, which, in turn, can decrease the drain current, transconductance, and gain of the device. Hydrogen effects in FETs with either Pt or Pd gate metals have been observed. Recent research has concluded that the diffusion of hydrogen may occur at the Pt sidewalls and not at the Au surface of the Au/Pt/Ti gate metal [34].

Other research on GaAs PHEMT and InP HEMT in a hydrogen atmosphere has shown that the drain current may increase in some cases (Figure 4-10). This observation has led to the conclusion that the hydrogen diffuses into the semiconductor surface where it is thought to change the metal–semiconductor built-in potential [35].

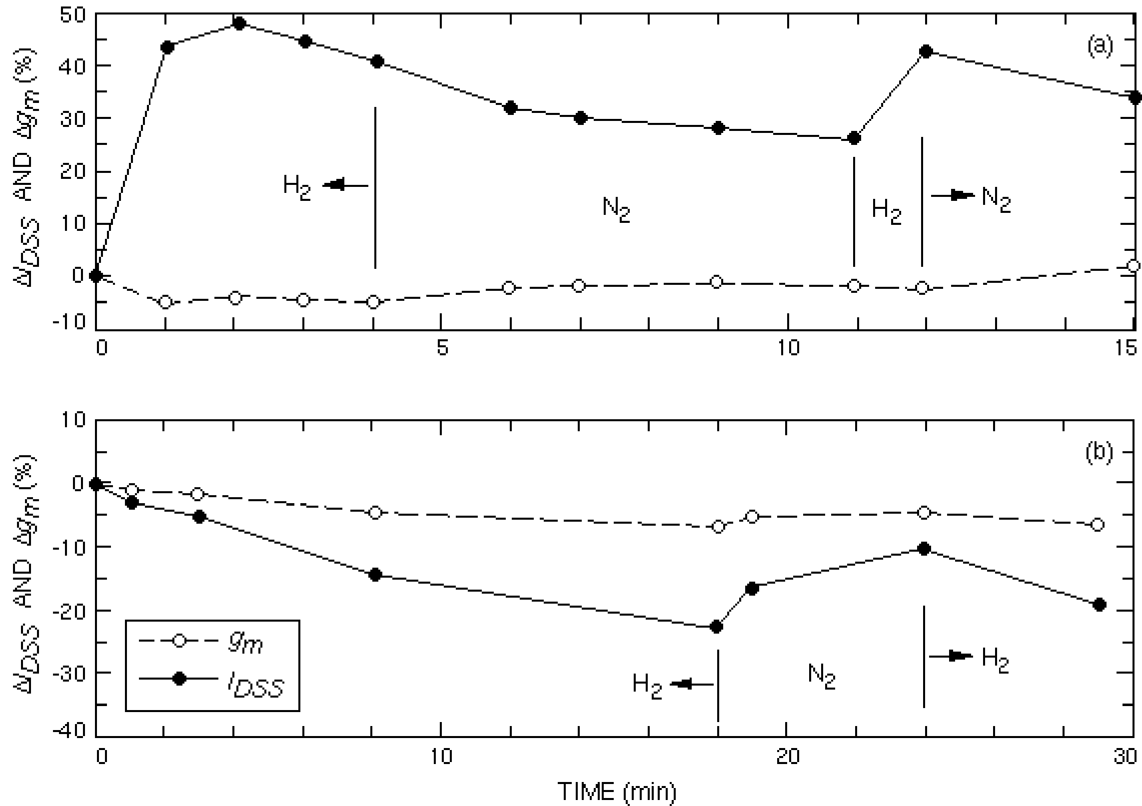

Figure 4-10. Changes in peak transconductance, g_m, and drain current at zero gate bias, I_{dss}, of (a) InP HEMT and (b) GaAs PHEMT under nitrogen and 4% hydrogen treatments at 270°C. The devices were unbiased during the treatments. The measurements were performed at room temperature. (From [35]; ©1994 IEEE.)

Manufacturers and users of GaAs devices used in hermetically sealed packages are currently pursuing an acceptable solution to this problem. Some of the possible solutions include thermal treatment of the packaging materials to reduce the amount of desorbed hydrogen after the seal, the use of hydrogen getter materials in hermetically sealed packages, and the use of barrier materials that do not contain the Pt/Ti or Pd/Ti structures. These solutions have limitations and possible instability problems that must be fully understood prior to implementation in high reliability environments [1].

3. Ionic Contamination

Ionic contamination in semiconductor devices is one of the important failure mechanisms. As a result of mobile ion contamination, GaAs-based devices can suffer changes in the carrier concentration resulting in threshold voltage shifts, an increase in leakage current, and gain reduction. Mobile alkali ions, such as N^+, Cl^-, and K^+, are the most common contaminants and have been identified by spectroscopic analysis to be the

principal causes of failure. The ionic contaminant must be in the form of a solution in order to be mobile and cause the referenced detrimental effects. The ion mobility is thermally and electric-field accelerated.

The existence of surface states and nonuniformities at the material interfaces of GaAs devices promotes the existence of conducting channels. This results in an increase in leakage current and a reduction of breakdown voltage. The surface ions can also contribute to surface leakage currents by creating a conductive path between adjacent metal lines. This may take the form of an electrolytic process involving the corrosion of the metallization, which will result in the formation of voids in the metal, and hence device failure.

Ionic contamination can arise during processing, packaging and interconnect, test, and operation in an unprotected environment. Surface preparation and cleanliness, characterization and control of processing materials and environments, and protection (passivation) of the active area of the devices can reduce or eliminate any ionic-contamination-related failures. High-temperature storage bake and exposure to high temperature during burn-in have been found to be effective methods of detecting ionic contamination problems.

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