III. Flip-Chip Package

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Finite element analysis as well as experimental studies have shown that chips with large edge length and small bump height tend to fail faster than chips with small edge length and large bump height. The reliability of flip-chip contacts is determined by the difference in the CTE between the chip and the ceramic substrate or the organic printed circuit board (PCB) [1,2]. For example, the CTE for GaAs is 5.8 ppm/K, for 96% alumina it is 6.4 ppm/K, and for PCB it is typically 20 to 25 ppm/K. The CTE mismatch between the chip and the carrier induces high thermal and mechanical stresses and strain at the contact bumps. The highest strain occurs at the corner joints, whose distance is the largest from the distance neutral point (DNP) on the chip [1]. For example, the DNP for a 2.5- $\times$ 2.5-mm chip is 1.7 mm. The thermomechanical stress and strain cause the joints to crack. When these cracks become large, the contact resistance increases, and the flow of current is inhibited. This ultimately leads to chip electrical failure. The failure criterion is an increase in resistance in excess of 30 mΩ over the zero time value [1]. The tradeoff in selecting the bump height is that large bumps introduce a series inductance that degrades high-frequency performance and increases the thermal resistance from the MMIC to the carrier, if that is the primary heat path.

The reliability of the bump joints is improved if, after reflow, a bead of encapsulating epoxy resin is dispensed near the chip and drawn by capillary action into the space between the chip and the carrier. The epoxy is then cured to provide the final flip-chip assembly. Figure 9-11 shows a typical flip-chip package. The epoxy-resin underfill mechanically couples the chip and the carrier and locally constrains the CTE mismatch, thus improving the reliability of the joints. The most essential characteristic of the encapsulant is a good CTE match with the *z*-expansion of the solder or the bump material. For example, if one uses 95 Pb/5 Sn solder having a CTE of 28 ppm/K, an encapsulant with a CTE of about 25 ppm/K is recommended. Underfilling also allows packaging of larger chips by increasing the allowable DNP. In some cases, the encapsulant acts as a protective layer on the active surface of the chip. Typical material properties of encapsulant used in flip-chip packaging are presented in [3,4].

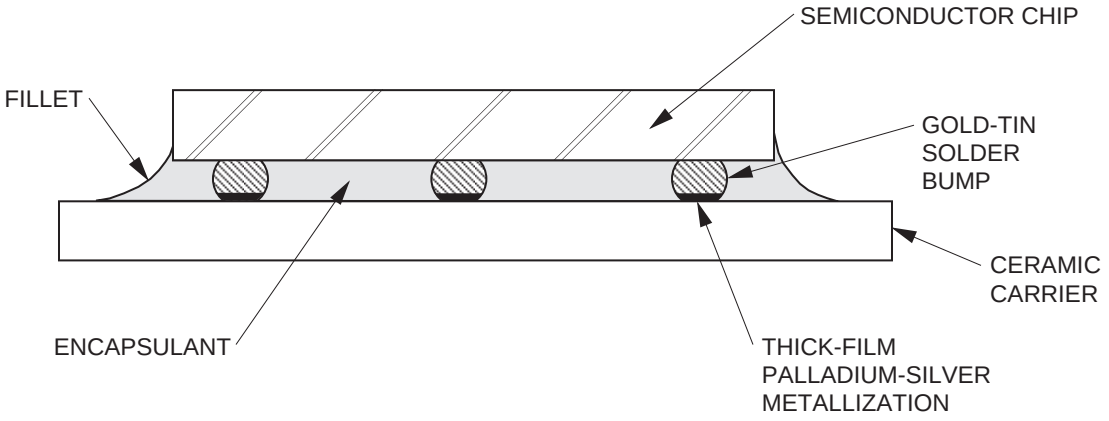

Figure 9-11. Flip-chip package.

Good adhesion between the underfill material, the carrier, and the chip surface is needed for stress compensation. The adhesion between the surfaces can be lost and

delamination can take place if contaminants, such as post-reflow flux residue, are present. For this reason, a fluxless process for flip-chip assembly is desirable [1]. Unfortunately, flip-chip bonding on PCB requires the use of flux [2]. However, on ceramic carriers with gold, silver, and palladium–silver thick-film patterns and via metallizations, fluxless flip-chip thermocompression bonding with gold–tin bumps has demonstrated high reliability [1]. The results of reliability testing [1] are summarized in Table 9-1 and may serve as a guideline for future work.

Table 9-1. Summary of reliability test conditions and results for fluxless flip-chip thermocompression-bonded bump contacts.

Parameter	Value
Bump height	30 to 70 μm
Chip size	A few mm
Chip carrier	Ceramic
Carrier camber	5 μm per cm
Camber compensation	By bump deformation
Underfill	Yes
Thermal cycling	After 6500 cycles (–55°C to +125°C), no contact failure and no change in contact resistance
High-temperature storage	After 1000 h, no increase in contact resistance
Temperature and humidity	After 1000 h (85°C and 85% RH), no change in contact resistance
Pressure-cooker test	After 1000 h (121°C and 29.7 psi), contact resistance increased slightly from 3 mW to 4 mW

Finally, care should be taken that the encapsulant or underfill covers the entire underside without air pockets or voids and forms complete edge fillets around all four sides of the chip. Voids create high-stress concentrations and may lead to early delamination of the encapsulant. After assembly, a scanning acoustic microscope can be used to locate voids in the encapsulant. The encapsulant should also be checked for microcracks or surface flaws, which have a tendency to propagate with thermal cycling and environmental attacks, eventually leading to chip failure [3].

References

[1] J. Kloeser, E. Zake. F. Bechtold, and H. Reichl, "Reliability Investigations of Fluxless Flip-Chip Interconnections on Green Tape Ceramic Substrates," *IEEE Trans. Components, Packaging, and Manufacturing Technology, Part A*, Vol. 19, No. 1, pp. 24–33, March 1996.

[2] J. Giesler, G. O'Malley, M. Williams, and S. Machuga, "Flip Chip on Board Connection Technology: Process Characterization and Reliability," *IEEE Trans. Components, Packaging, and Manufacturing Technology, Part B*, Vol. 17, No. 3, pp. 256–263, August 1994.

[3] D. Suryanarayana, T. Y. Wu, and J. A. Varcoe, "Encapsulant used in Flip-Chip Packages," *IEEE Trans. Components, Packaging, and Manufacturing Technology*, Vol. 16, No. 8, pp. 858–862, December 1993.

[4] G. O'Malley, J. Giealer, and S. Machuga, “The Importance of Material Selection for Flip Chip on Board Assemblies,” *IEEE Trans. Components, Packaging, and Manufacturing Technology, Part B*, Vol. 17, No. 3, pp. 248–255, August 1994.