VIRTEX-5QV STATIC SEU CHARACTERIZATION SUMMARY

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1 VIRTEX-5 OVERVIEW

The Xilinx Virtex-5 device is a static random access memory (SRAM)-based, in-system, reconfigurable field programmable gate array (FPGA). The Virtex-5 architecture includes seven major, programmable block types optimized for specific functions:

- The Configurable Logic Blocks (CLB) provide functional elements for combinatorial and synchronous logic, including configurable storage elements, cascadable arithmetic functions and, newly introduced in Virtex-5, 6-input look-up tables (LUTs).
- The Digital Signal Processing (DSP) Slices provide advanced high-speed arithmetic and comparison functions, including multiply and accumulate.
- The Block Memory modules provide large 18-Kbit storage elements of true dual port RAM.
- The Digital Clock Manager (DCM) blocks provide clock frequency synthesis and de-skew.
- The Phase Lock Loop (PLL) blocks provide clock distribution delay compensation, clock multiplication/division, coarse/fine-grained clock phase shifting, and input clock jitter filtering.
- The bidirectional Input/Output Blocks (IOB) have optional Single Data Rate (SDR) or Double Data Rate (DDR) registers and serializers and deserializers (SERDES) enabling support for many industry input/output (I/O) standards, plus selectable drive strengths and digitally controlled output impedance.
- High speed serial GTX transceivers are capable of running up to 4.25 Gb/s. Each GTX transceiver supports full-duplex, clock-and-data recovery.

The high-reliability, radiation-hard Virtex-5QV product is a family of one part type, the XQR5VFX130. Its counterpart in the commercial Virtex-5 line is the XC5VFX130T and they share exactly the same type and numbers of basic blocks and capabilities except for the removal of the System Monitor and PowerPC blocks and a few I/O's in the corners (including two GTX transceivers) in order to improve package reliability. The rad-hard version incorporates several upset-hard-by-design elements, including:

- Dual-node configuration cells that require charge collection in at least two active nodes before an upset can occur.
- Dual-node master-slave user flip-flops (user registers).
- Single-event transient filters on all flip-flop inputs: data, clock, and control.
- Triple-modular redundancy (TMR) in the control circuitry and registers.

Table 1 lists the main architectural resources of the Virtex-5QV space-grade FPGA in comparison with its commercial-grade counterpart. These two parts share a compatible superset footprint to allow prototyping with the commercial device [1]. See the overview datasheet [2] and the electrical specification datasheet [3] for more details on the Virtex-5QV and pointers to more detailed documentation.

Table 1. Comparison of Architecture Resources

	Description	Commercial-Grade XC5VFX130T	Space-Grade XQR5VFX130
CFG*	Configuration Bits* (millions)	34.1	34.1
BRAM	Block Memory Bits	10.9	10.9
LOGIC	Slices (4 Lookup Tables/slice)	20,480	20,480
DSP	18x25 Multiply, 48 bit Accumulate	320	320
PPC	PowerPC405 Processors	2	0
CMT**	Clock Manager Tiles	6	6
MGT	High-speed Transceivers	20	18
IOBs	Input/Output Blocks	840	836

* Only real memory cells in the Configuration Bit Stream are counted here (not counting BRAM)
** Each CMT includes two Digital Clock Managers (DCM) and one Phase-Locked Loop (PLL)

Like its commercial counterpart, the Virtex-5QV device is fabricated in a 65-nm process geometry. That makes it currently the most highly scaled complementary metal oxide semiconductor (CMOS) technology offered to the aerospace industry. For Xilinx, it is the first product with extensive radiation-hard by design (RHBD) features; Virtex-4QV and earlier space-grade FPGAs use exactly the same mask and circuitry as a particular revision of their commercial counterpart.

This report is the result of the combined efforts of members within the Xilinx Radiation Test Consortium (XRTC), occasionally known as the Xilinx SEE Test Consortium. The XRTC is a voluntary association of aerospace entities, including leading aerospace companies, universities and national laboratories, combining resources to characterize reconfigurable FPGAs for aerospace applications. Previous presentations and publications of Virtex-5QV radiation results have been made by Consortium members, notably at the NSREC and MAPLD conferences and the SEE Symposium.

This report focuses on the measured upset characteristics of the main static (or unclocked) memory elements. A companion report is planned that will cover individual functional blocks including frequency effects. Reports similar to this one documenting the upset susceptibility to heavy ions and protons of the static memory elements in the older space-grade Virtex-4QV [4] and Virtex-2 [5] families are available; Virtex-4QV is still recommended as a viable choice for new designs. A comparison with those results shows that the upset-hard-by-design features of the Virtex-5QV are remarkably successful, making even more of a giant leap forward in improved upset characteristics than the enviable improvements in speed, density and architectural features derived from and accompanying the process scaling to 65 nm.

2 Latchup Testing

Fully tested production Virtex-5QV devices were tested for Single-Event Effect (SEE)-induced latchup events at the Texas A&M Cyclotron Institute in July of 2011. Two prior tests had been run on pre-production samples. There were no beam-induced latchup events recorded during any of those tests.

Table 2 provides a summary of the device under test (DUT) test parameters for the latchup irradiations. Each DUT was heated to a nominal pretest temperature of 120 - 125°C and biased with specification-maximum voltages.

Table 2. Latchup Test DUT Conditions

Parameter	Value	Unit
DUT junction temperature (target)	+120	°C
Internal voltage	1.05	V
I/O voltage	3.45	V
Auxiliary voltage	2.66	V

For the purpose of this experiment, the classic practical definition of a latchup was adopted: any sudden high current mode resulting from the test run that required a power cycle of the DUT in order to recover functionality and nominal current. During the test runs, the DUT core voltage and I/O voltages and their dynamic current consumption were captured and recorded in a running log (strip chart). Current triggers on these were set well above maximum nominal draw; in the event of a latchup condition, software would detect that the thresholds were exceeded, declare a latchup condition and quickly cycle power to prevent device damage. Due to the high fluxes and total fluences used for the latchup testing, it was expected that the DUT would lose its programming early in the run and would likely be subject to multiple Single Event Functional Interrupt (SEFI) conditions during the run. The purpose of the experiment was to demonstrate hardware survivability and soft recovery without the need for a device power cycle. Therefore, the test procedure adopted was as follows:

1. Program and readback to verify DUT configuration memory; verify design functionality.
2. Heat DUT to +120°C.
3. Record initial temperature, voltage, and current conditions.
4. While irradiating the DUT to a fluence of at least 10^7 particles/cm^2, record DUT power (voltages and currents) and internal diode temperature.
5. Scrub and readback DUT configuration memory after end of irradiation and verify design functionality.

The tests were performed with backside-thinned samples in vacuum to assure sufficient range that the ions would exit the silicon before passing the Bragg peak energy. Photo 1 shows the test motherboard and a DUT card mounted in the vacuum chamber.

Table 3 shows the run parameters and results for each DUT. A 15 MeV/amu Au ion beam was used to deliver an effective Linear Energy Transfer (LET) > 105 MeV/mg/cm^2 to a fluence greater than $2 \cdot 10^7$ particles/cm^2 in the active layer. In some cases, multiple

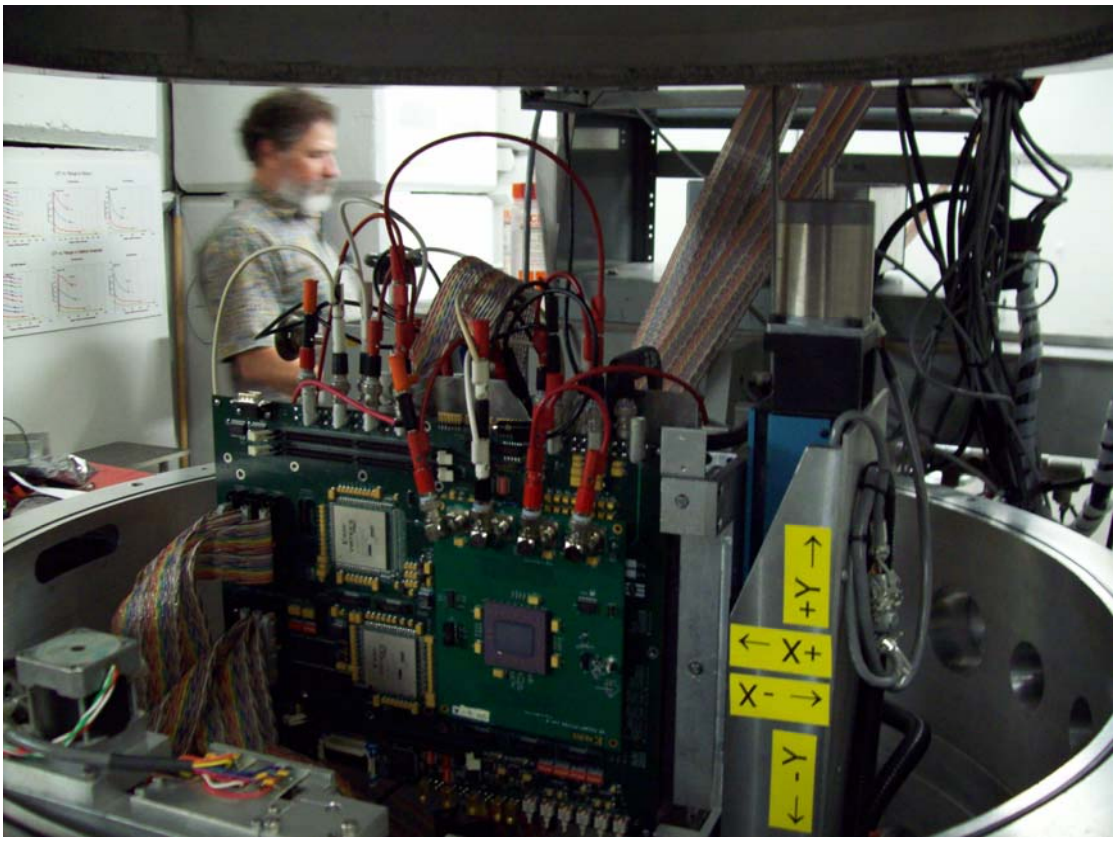

Photo 1. Test Apparatus Setup in Vacuum Chamber at Texas A&M

test runs were conducted in order to obtain the total fluences shown in Table 3. Tilting the samples with respect to the beam was employed to increase the effective LET to the values shown. The effective range listed is the Si-equivalent depth the ions would penetrate after exiting the top of the active silicon before stopping; these were chosen to ensure that the bombarding gold ions had not yet reached the their maximum energy deposition at the Bragg peak.

Table 3. Latchup Test Data
Using the Texas A&M Cyclotron's 15 MeV/amu Gold (Au) Beam

XQR5VFX130 DUT serial #	Effective LET, MeV-cm^2/mg	Effective Range, µm	Average Flux, #/ cm^2-s	Total Fluence, #/cm^2	Max Temp °C	Min Temp °C	Single -Event Latchups
s/n:515	104.8	65.2	$1.8\text{x}10^5$	$8.0\text{x}10^7$	125	117	none
s/n:515	132.2	40.6	$2.8\text{x}10^5$	$2.0\text{x}10^7$	126	115	none
s/n:515	145.2	30.6	$3.1\text{x}10^5$	$2.0\text{x}10^7$	127	120	none
s/n:514	145.5	35.6	$1.9\text{x}10^5$	$2.0\text{x}10^7$	126	114	none
s/n:592	135.7	67.5	$0.90\text{x}10^5$	$2.0\text{x}10^7$	126	110	none

Because Virtex-5 devices are only offered in flip-chip packaging, irradiation is done through the top or backside of the silicon substrate. In order to reach the active layer at the bottom with a high-LET, short-range heavy ion, the backside of the silicon must be thinned to less than 100 µm. The range given in column 4 of Table 3 is the residual silicon-equivalent penetration depth after the ion goes through the thinned backside

substrate and the epitaxial layer, i.e. it is the residual effective range after exiting the active layers. Figures 1a-1c show the recorded current and temperature before, during, and after the irradiations listed in the last three rows of Table 3.

Because the bottom of the silicon is solder "bumped" to a fully populated ball-grid package, it is difficult to heat the device enough for latchup testing with an external heating element. In order to obtain the target temperature (near 125°C junction temperature) in vacuum, the devices were configured with a "heater" design meant to increase dynamic current consumption sufficient to heat the transistor junctions to a desired temperature. The core temperature of the device is monitored by measuring the resistance of an internal diode specifically provided for this purpose.

The heater design is a long shift-register chain of CLB flip-flops. Typically, this chain is long enough to consume more than 75% of the available device resources. The start of the register chain is fed by a one-bit counter so that alternating ones and zeros advance through the chain with each clock pulse. In order to obtain a high enough frequency to meet the dynamic consumption requirements, a DCM is used to multiply the input clock frequency. The clock on/off is a manual control; the vertical current changes in the strip charts of Figure 1 correspond to the experimenter exercising that manual control.

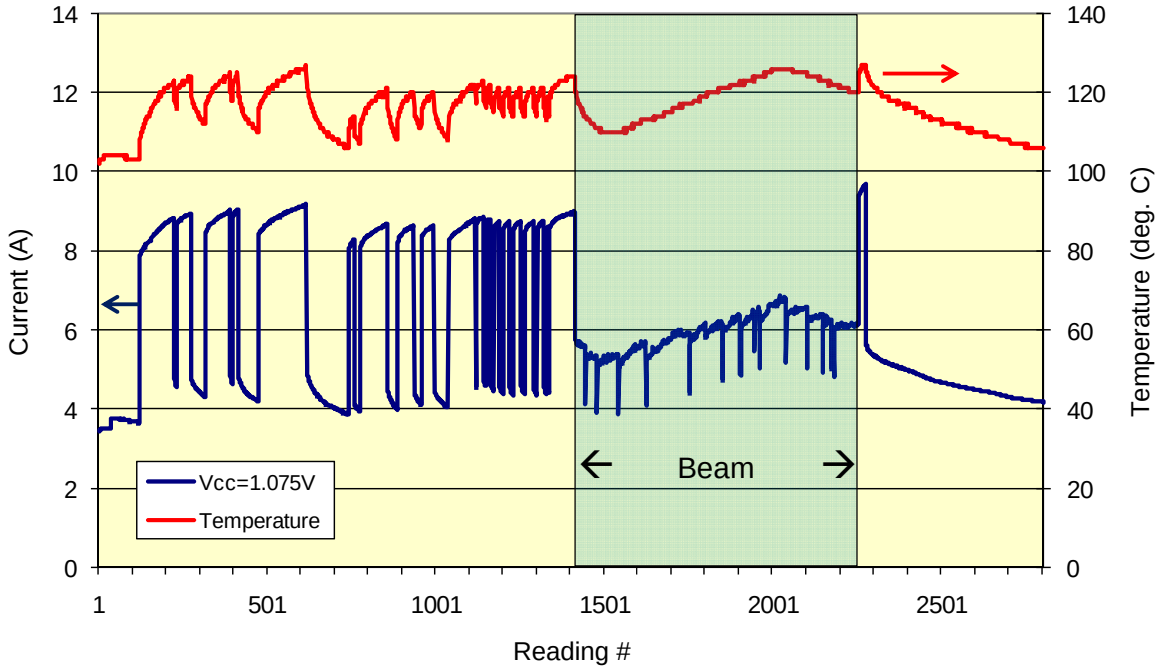

Figure 1a. Current and temperature for s/n: 592 during latchup testing: angle=50 degrees, fluence =2.0x10^7 gold ions per sq.cm, effective LET=135.7 MeV per mg/cm^2

Early in each irradiation, the configuration of the device was upset and self heating would stop. In spite of the high fluxes used, sometimes scrubbing was able to briefly restore functionality; those are seen as positive current spikes during the irradiation in Figure1b and 1c. Note that negative spikes correspond to SEFI events (detailed in Section 3.2); these were automatically detected and cleared via subsequent reconfiguration from pulsing the PROG_B input. Supplemental heating was provided under the DUT on the daughterboard with ohmic flat strip heaters driven by a manually controlled power supply. In Figure 1b, two adjustments of the strip heating are clear, one increase early in the run

when the temperature had dropped to 110°C near the beginning of irradiation and one decrease near the end when the temperature reached 126°C. The instrumentation used had one degree resolution and maxed out at 127°C, that is, an indicated 127°C could be hotter. Maximum and minimum temperatures over the course the irradiations are noted in Table 3.

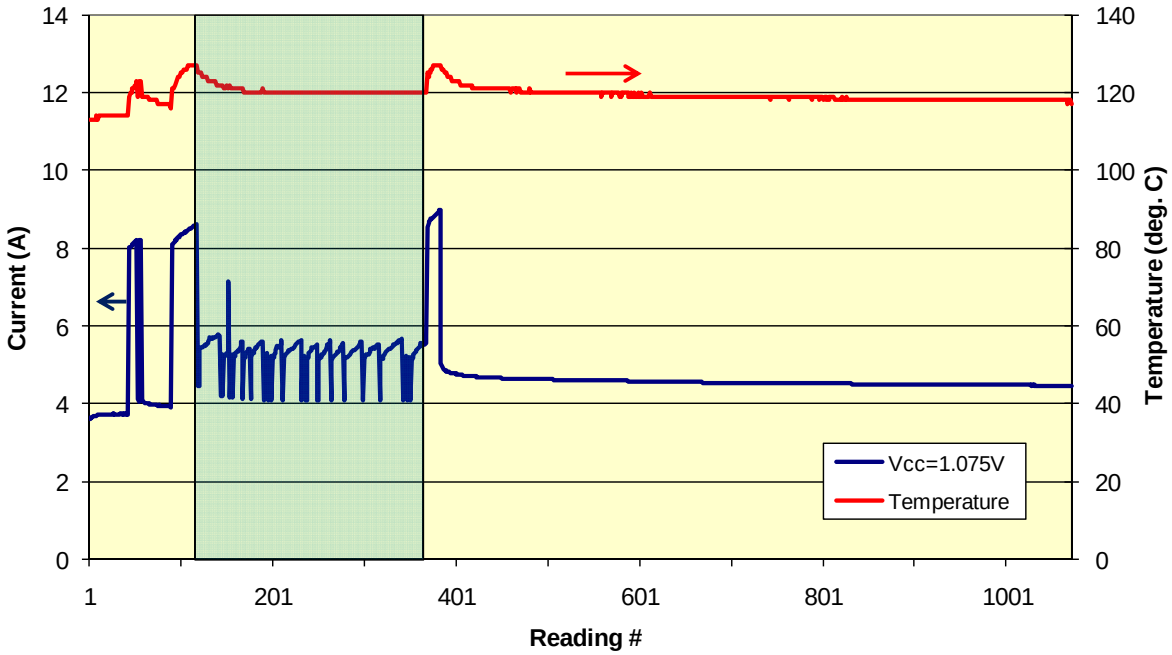

Figure 1b. Current and temperature for s/n:515 during latchup testing: angle=50 degrees, fluence =2.0x10^7 gold ions per sq.cm, effective LET=145.2 MeV per mg/cm^2

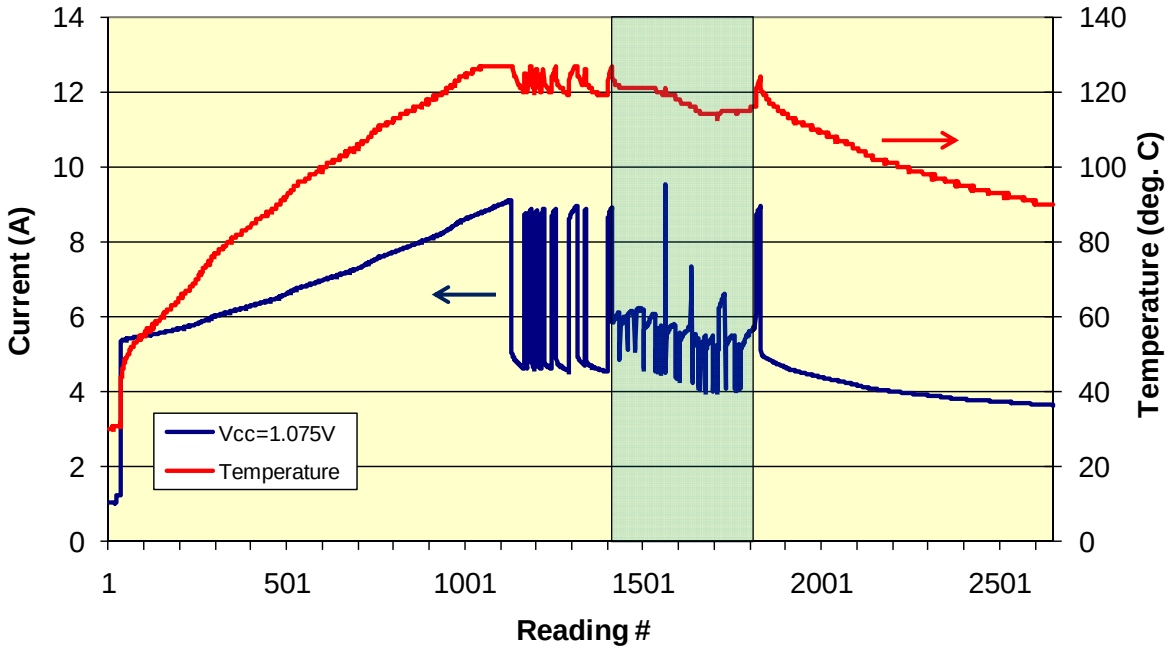

Figure 1c. Current and temperature for s/n:514 during latchup testing: angle=50 degrees, fluence =2.0x10^7 gold ions per sq.cm, effective LET=145.5 MeV per mg/cm^2

It should be noted that the power supply software reported one high current reading just before the shutter opened and one latchup event just after the shutter was closed for the irradiation of s/n:592. Initially, the experimenters and facility personnel suspected that this was the result of shutter-induced electromagnetic noise pulse (EMP) because recent beam shutter replacements had left out the usual noise-suppression capacitor/resistor circuitry. However, while some shutter-coincident anomalous upsets were seen by some XRTC experiments- as well as other experimenters- in June 2011, a detailed examination of the logs revealed that the DUT, in fact, did not experience latchup. The software current threshold setting was exceeded due to an overheating mistake by the experimenters. As can be seen in Figure 2, the temperature was pegged at 127°C; the measured current never exceeded 10.005 A and the voltage never sagged due to current limiting above that as would have been the case in the event of a latchup event. With no clock for 170 seconds after the ≈6.7 second irradiation (the experimenter's reaction time plus shutter lag), the temperature reading finally comes back into range indicating that heating lag had significantly overheated the DUT and the high current reading seen by the software indicated correct operation for the out-of-spec high temperature, not latchup. Buttressing this conclusion, the Functional Monitor and Configuration Monitor logs (shown at the top of Figure 3) recorded that the DUT was operating normally and correctly after the shutter opened for a few seconds. At that point, the software cycled the power supply after consecutive readings that the current was 10.005A, slightly in excess of the selected threshold of 10.000A. Note that the following irradiation of the same DUT (s/n:592) using identical conditions - except for more careful temperature control - is the one shown back in Figure 1a where the software detects no latchup through a fluence of 2.0×10^7 ions/cm^2.

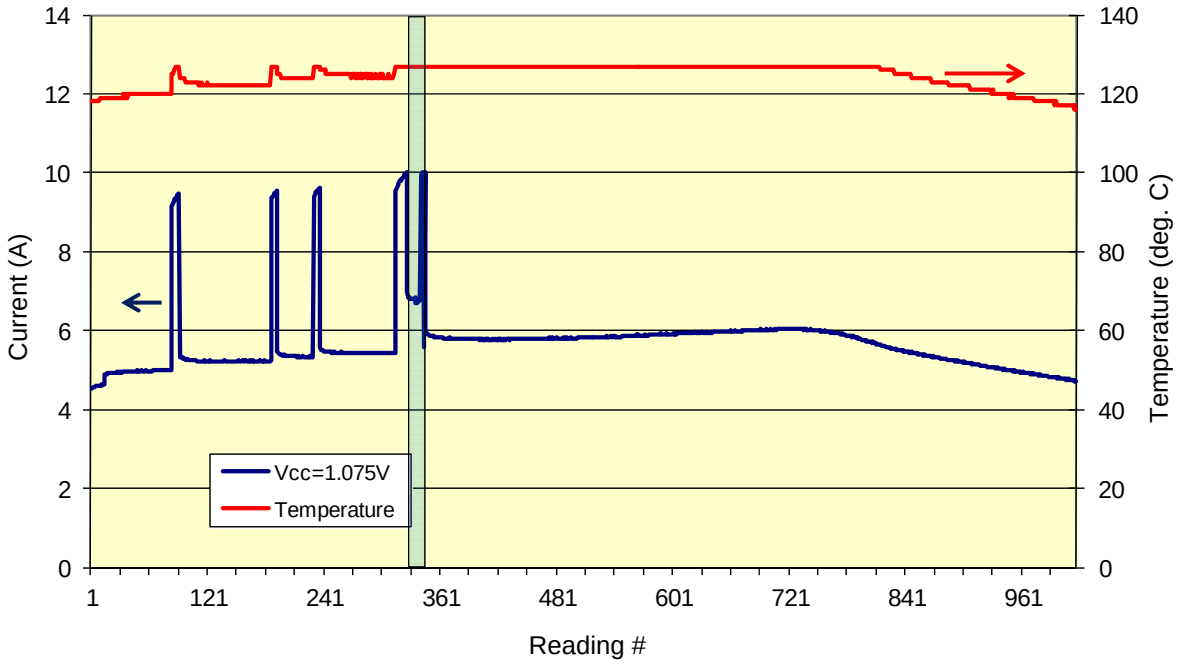

Figure 2. Current and temperature for s/n: 592 during latchup testing: angle=50 degrees, fluence <2.8×10^5 gold ions per sq.cm, effective LET=135.7 MeV per mg/cm^2

3 STATIC TESTING

The static Single-Event-Upset (SEU) experiments' goal is to measure the upset susceptibility of memory elements incorporated in XQR5VFX130 FPGA for both heavy ions and protons in order to allow calculation of the expected space upset rates. For the dual-node based cells (configuration memory and user flip-flops), a special test chip (dubbed TC-65nm) is required because of the importance of grazing angles to the space upset rate. Other static characterizations were carried out on the pre-production FPGA samples (dubbed FX-1) and, more recently, on production FPGA samples. In addition, as an adjunct to all FPGA static, dynamic, and mitigation testing, each DUT is carefully monitored for any SEFI conditions during all experiments conducted. For all these tests, the same basic experimental setup was used: the XRTC motherboard with an appropriate daughter DUT board to support the particular test . Note that the Configuration Monitor capability is not used when testing the TC-65 DUTs as they are more like mini-ASICs and do not have a programmable configuration.

It is important to understand that what we mean by static testing is more phenomenological than physical. Static testing is done without clocking the design during irradiation or clocking it at frequencies that are proven to have little effect on the results (typically, slow speed). Physically, this does not mean that all upsets are direct upsets of the memory cell under test. Some (or even most) of the upsets may be due to Single-Event Transients (SETs) on clock lines or asynchronous control signals, especially on the upset-hardened-by-design elements.

3.1 Experiment Setup

Figure 3 shows the test setup in vacuum as needed for the latchup testing. JPL's 5-40 pin bulkhead was used to run five of the six communication cables through the vacuum chamber. The sixth was run through the 50 pin D-Sub connector provided by the irradiation facility at the Texas A&M University (TAM) cyclotron. Three parallel cables were also sent through the 50 pin connectors (one for a DUT readback Parallel-IV cable, one for a motherboard/DUT design programming Parallel-IV cable, and one for the temperature monitoring circuit).

A mounting platform with integrated power breakout cables was used for mounting the motherboard to the rotating chassis in the vacuum chamber and for extracting the four power supplies from the 40-pin cable. The four supplies were sent through the vacuum chamber bulkhead over BNC connectors then re-integrated to the 40-pin cable. Force and sense were tied together at the power supply (HP6629) for all four supplies and provided the necessary 2.5V, 3.3V, and 3.3V I/O for the motherboard; the last supply was used to control heater strips attached to the back of the daughter card. The receiver/driver cards were powered by the 3.3V of the motherboard I/O. The 5V for the Parallel-IV cables and temperature sensor circuit were powered by an external Agilent E3610A, and also run through a BNC bulkhead (provided by TAM). The DUT power supply was an HP6623, which provided three supplies, with currents of 5A, 10A, and 2A on supplies one, two, and three respectively. Supply one provided 2.5V to V_{AUX} , supply two provided 1.0V to V_{INT} and supply three provided 3.3V to two V_{CCO} DUT I/O banks that talk to the

motherboard. Force and sense were tied together at the bulkheads on supplies one and three which were run through BNC bulkhead feedthroughs. High current cables were used to run force for supply two in through a 40-pin cable and bulkhead connector and were separated back into banana cables with a second custom 40-pin connected to an additional banana cable; 20 pins were used for power and 20 for ground. Sense for supply two was sent through a BNC over banana cables and connected to force at the daughter card.

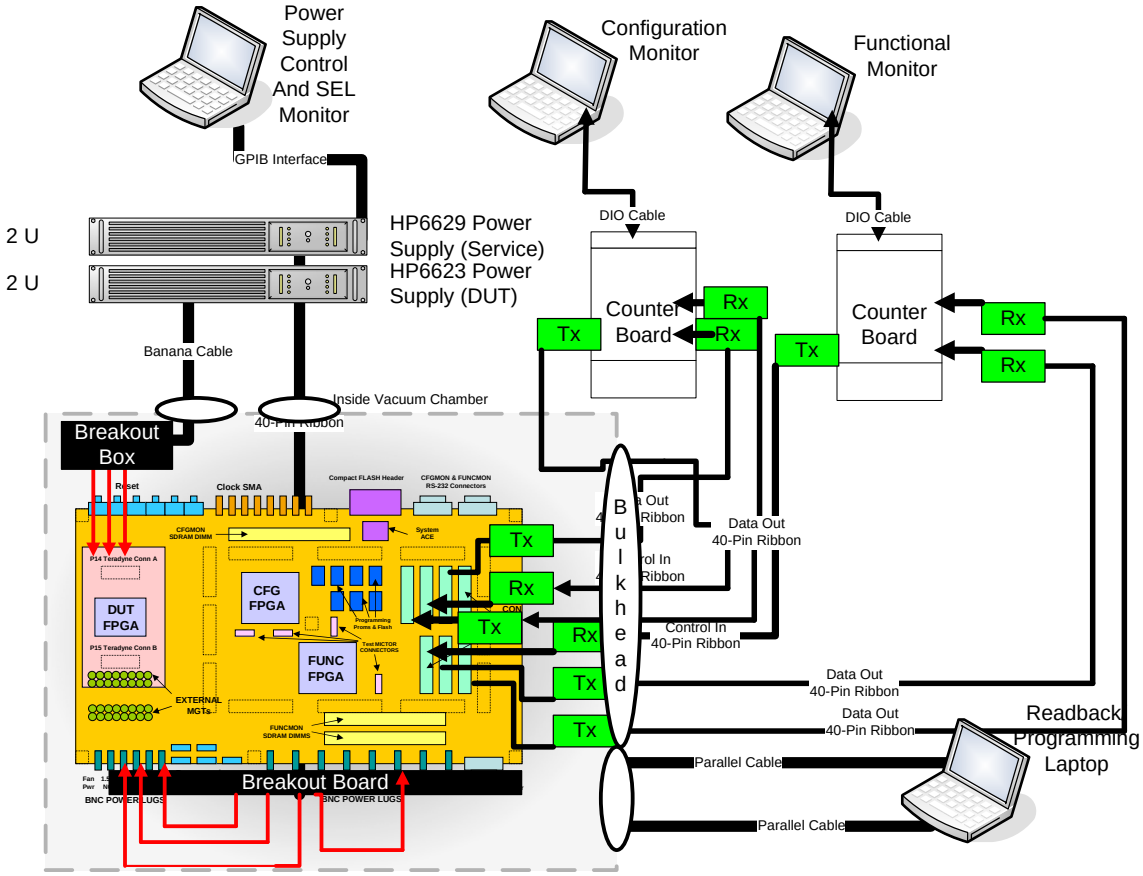

Figure 3. SEU Test Hardware Setup

More conveniently, most of the SEU testing was conducted in air with long enough ion ranges and thin enough DUTs to ensure penetration; LETs were adjusted for the intervening materials including the air gap. The setup for in-air testing was essentially the same as in-vacuum testing, the main exception being that the adapted connections for getting through the bulkheads were discarded. Also, USB programming cables were used via high speed hubs for the in-air irradiations.

3.2 SEFI Results

The heavy ion irradiation testing on the Virtex-5QV FPGA have been performed at the BASE Facility at Lawrence Berkeley National Laboratory (LBL) and The Cyclotron Institute, Texas A&M University (TAM) starting in November 2008. Many static, dynamic, and mitigation tests have been performed with the equivalent of many millions of years in the space radiation environment. During all this testing, the DUT was monitored for device SEFIs, the result of SEUs in FPGA control logic that are not accessible to the aerospace designer. To recover from a device SEFI, the FPGA must be re-configured via pulsing the PROG pin or cycling power.

The Virtex-5QV has been tested with a variety of ions at different incidences covering an LET range of 0.11–145.5 MeV-cm^2/mg. A combination of beam energy degraders and DUT angles were used to achieve higher LETs for a given ion. Note that, in some cases, the effective LET from an angled DUT gives a different cross section than the same LET from a heavier ion at normal incidence; this disagreement seems clear at the 65-nm node and will likely grow as scaling continues. Because of the aim of using this data is to predict space rates, normal incidence and, thus, energy-tuned and/or -degraded data is preferred.

The data graphs shown in this report all show two sigma statistical error bars; in some cases, the error bars are smaller than the plotting symbol and, thus, don't show in the plots.

Typically, device SEFIs are low probability and are almost never seen while in orbit. Nevertheless, Xilinx designers have significantly reduced the Virtex-5QV's susceptibility to device SEFIs. However, in test environments where event rates are hugely accelerated in order to obtain statistical significance and accurate measurements of events even with negligible cross-sections, SEFIs are observed. The criterion for a SEFI is that it requires either a complete reconfiguration or power-cycle of the device before returning fully to normal operation. Early testing observed a very rare SEFI mode that seemed to require power-cycling, but it is now understood that it can be eliminated by following the recommendations in XAPP 588.

A great deal of effort has been undertaken to categorize SEFIs into understandable phenomenological buckets and to recognize their signatures in key status registers. The knowledge gained is incorporated into these results as well as recommendations for on-orbit configuration management and SEFI detection, if needed [6]. As the results below demonstrate, the chance of an on-orbit SEFI is very low; thus, only missions with the most stringent reliability requirements will need to concerned with them

The observed SEFIs for the Virtex-5QV are placed into two main categories:

1. Design-intrusive
2. Visibility-intrusive

In the design-intrusive category are the Power-On-Reset-like (POR) and the Global Signal (GSIG) SEFIs. The second category includes the malfunction of the SelectMap Port (SMAP) or the auto-incrementing or ability to write to the Frame Address Register (FAR).

The so-called Start-Up (SU) SEFI has proven to not actually be a SEFI as issuing a start-up command restores the DONE pin and neither the design nor configuration visibility is interrupted. Thus, there is a third category of device SEFI: the fake or false or non-SEFI. The so-called Readback (or RB) SEFI experienced by the Virtex-4 [5] where some bits cannot be scrubbed without unmasking them also falls into the third category as it is more a scrubbing annoyance than a design or visibility intrusion. The SCRUB SEFI seen in the Virtex-4 [5] was not observed. Most of the testing was done with the Xilinx recommended frame-based scrubbing where checking for an SMAP SEFI between each frame prevents accidentally putting in more than a frame's worth of bad or misaligned data. In theory, it is still possible for this SEFI to occur so following the frame-based scrubbing recommendation is prudent.

The POR SEFI results in a global reset of all internal storage cells and the loss of all program and state data. Observation of this mode is that when it occurs it is almost always accompanied by the DONE pin dropping low, a sudden change of the DUT current to its starting value, , and loss of all configured functions. If a configuration readback is attempted, then an unusually large readback error count will be seen (millions of bits in error).

The SMAP SEFI is the loss of either read or write capabilities through the SelectMAP port. This SEFI is indicated either by the retrieval of only meaningless data or inability to refresh data. In a few cases, the port could be re-activated by using the Joint Test Action Group (JTAG) port to find and correct errors in the control registers. In the remaining occurrences, a complete reconfiguration was required to regain full port access and functions.

The FAR SEFI results in the frame address register continuously incrementing uncontrollably. It is detected by an inability to write and read control values to the FAR while all other aspects of the SelectMAP port are still fully functional. For the purpose of orbital error rate calculations, the FAR SEFI is considered a sub-set of SMAP SEFI modes. However, for characterization purposes, it is individually scrutinized.

The Global Signal SEFI was separated from other design-disrupting SEFIs following the Virtex-4 testing [5]. These signals include GSR (Global Set/Reset), GWE_B (Global Write Enable), GHIGH_B (Global Drive High), and others. They can all be observed through the status (STAT) register or one of the control (CTLx) register. Some of them can be scrubbed, but others require a reconfiguration.

Readback stucks or un-scrub-able bits (no longer categorized as a SEFI) occur when a masked portion of the readback data has been upset and, thus, cannot be corrected. This condition is caused by the use of the GLUTMASK, which enables the use of SRL16s in conjunction with partial reconfiguration. If GLUTMASK is not invoked then this condition does not occur. Although these bits do not affect the operability of the configured design, this condition will cause a false-positive detection of a SMAP (cyclic redundancy check [CRC] error sub-type) SEFI in the SEFI detection algorithm because the upset bits cannot be corrected through partial reconfiguration. In Virtex-5QV, configuration bits that can be accessed through DRP bits fall into this category even when the resource they are associated with is not implemented. In that case and, in fact, in most cases, the upset of an un-scrub-able bit does not affect design operation.

Scrub SEFIs were observed for the first time in the Virtex-4 testing [5]; but they were not observed in the extensive Virtex-5QV test campaigns. This extremely rare SEFI mode seems to be the result of an upset causing corruption of the data stream being scrubbed into the DUT. This obviously can disrupt the design operation and may be accompanied by some large internal contention currents. On the Virtex-4 a key characteristic of the Scrub SEFI is that it is the only SEFI that has ever been observed to have any design dependence.

The selected parameters to draw the Weibull curves are given in Table 4. The measured data points and the cross section curve for the combined SEFI modes are displayed in Figure 4. The POR and the SMAP SEFI are the most prominent components. While the exact proportions are difficult to determine due to the low statistics (even with massive ion fluences) and they appear to vary some with LET, the design-intrusive SEFIs are about 70% while visibility SEFIs are about 20%. The remaining 10% are the events that show SU-type signature; these are included even though the XRTC has not yet observed a design intrusion or a case where the startup command fails to restore the DONE pin which, if it were possible, would make POR SEFI detection less reliable).

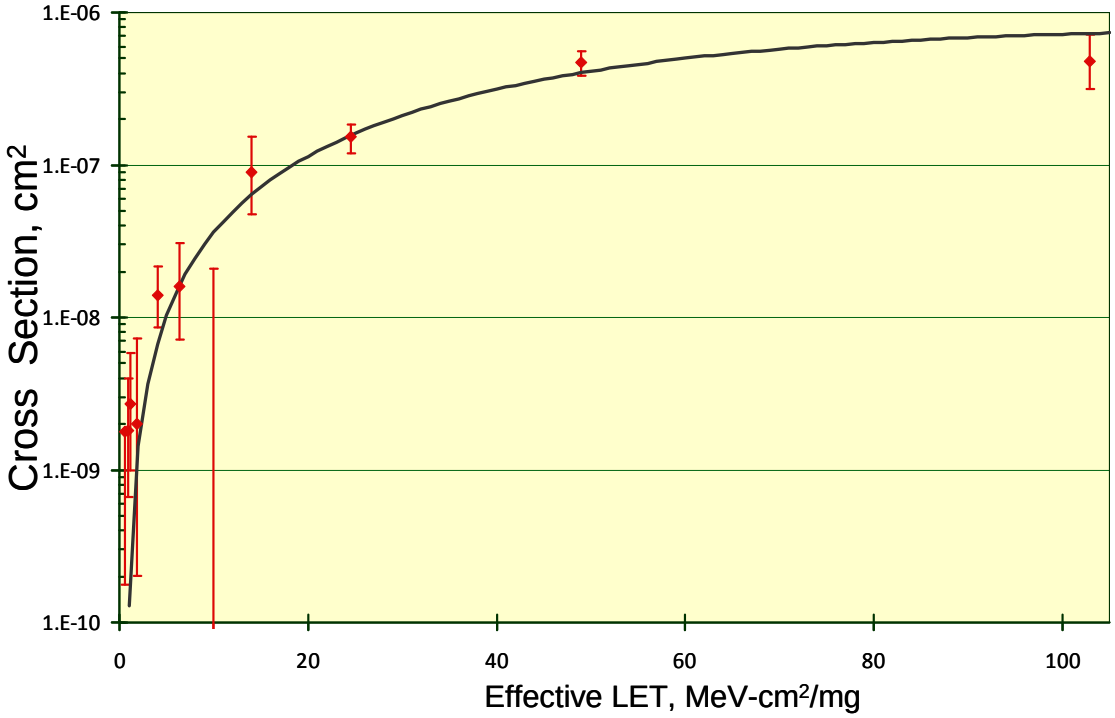

Figure 4a. Virtex-5QV SEFI Susceptibility due to Heavy Ion Strikes

It is likely that the SEFI curve is overly conservative because of the way the data had to be taken. Both the dominant POR SEFI as well as the design-intrusive GSIG SEFI are mitigated using Xilinx-style triple modular redundancy in the chip's built-in circuitry. This type of mitigation shows a strong dependence on flux because the probability of upsets in two domains is a quadratic function of the upset rate which is proportional to flux in a given experiment. The higher fluxes used by necessity in the beam testing are

will cause orders of magnitude more TMR-mitigated SEFIs for a given fluence than the same fluence at the much lower rate of irradiation of the real space environment.

Table 4. Weibull Fit Parameters for Virtex-5QV SEFIs

	Weibull Parameters			
SEFI	**Limit (cm^2/device)**	**Onset** -	**Width** -	**Power** -
Heavy-Ion Combined	$8.0x10^{-7}$	0.7 MeV-cm^2/mg	60	1.65
Proton* Combined	$1.7x10^{-13}$	5 MeV	20	0.8
Proton*, NOT incl. SUs	$3.2x10^{-14}$	5 MeV	20	0.8

* statistics still very low

Preliminary proton SEFI testing was undertaken in June 2010 at the University of California at Davis (UCD) cyclotron. While only tentative conclusions could be drawn due to the upset rate of the supporting equipment from secondary neutrons, it seemed clear that the Virtex-5QV shows extremely low proton sensitivity for SEFIs as well as for configuration upsets, with a device cross section of approximately $5x10^{-14}$ cm^2 for 60 MeV protons. The XRTC motherboard has been re-worked to accept Virtex-5QV devices for the configuration and functional monitoring service roles. Using this apparatus, three proton test campaigns at the UC-Davis cyclotron have been accomplished in November 2011 and January and June 2012. However, the number of SEFIs observed so far is small so the 95% confidence error bars are still quite large as can be seen in Figure 4b, except for 63 MeV which is dominated by SU SEFIs.

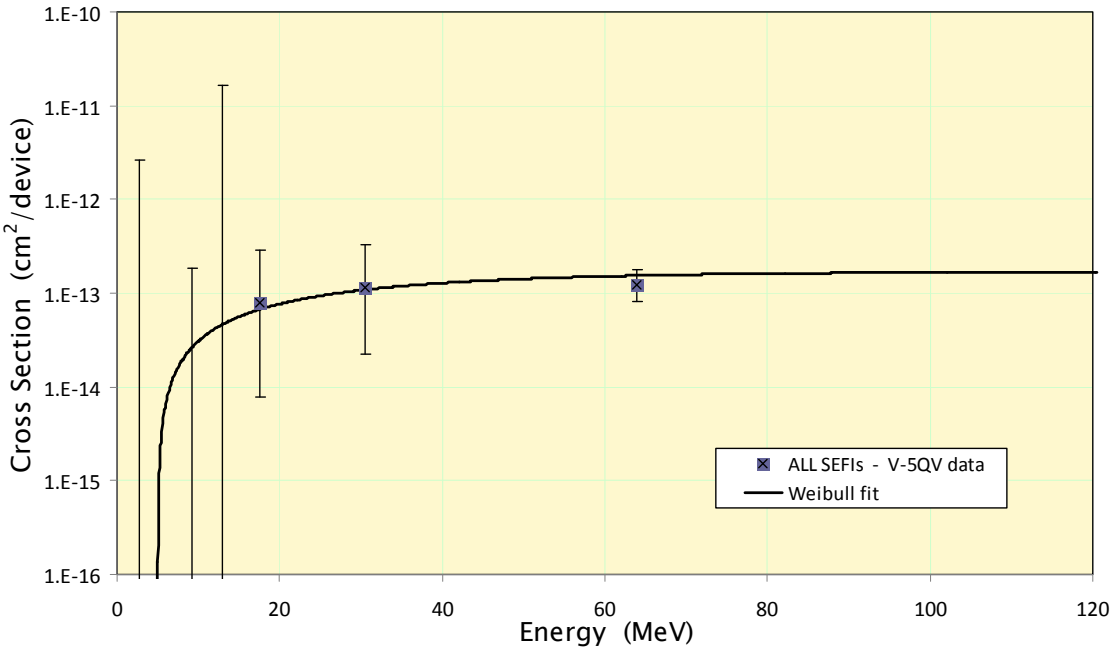

Figure 4b. Virtex-5QV SEFI Susceptibility due to Protons

Along with the change to Virtex-5QV service FPGAs, two other procedural changes accompany the 2011-2012 proton tests: (1) strict monitoring of the Configuration

Monitor FPGA's configuration for upsets and (2) no PROG_B assertion on SU SEFI detection. Thus, runs were terminated immediately if SEFI monitoring became potentially untrustworthy. The latter change means that SUs should not be included in the total SEFIs for proton results, but, in order to be consistent with the heavy ion results of Figure 4a, SU (false) SEFIs are also included in the proton results and fit of Figure 4b. The agreement with the preliminary result on the more shaky apparatus is fortuitously quite good- about a factor of two higher for all SEFIs and, when SUs (which are not 'real' SEFIs because they are not design or visibility intrusive) are subtracted the earlier results are about 2x high.

3.3 Other Static Results

This section presents results for three distinct memory element types included in the Virtex-5QV- Block RAM, User Registers, and DSP Registers. Summarizing the results, Weibull parameters for heavy ion fits to the data are given in Table 5 and Table 6 is a placeholder for the proton fits. Select data plots for each are given in the following sub-sections while additional details are in the referenced papers and reports.

Table 5. Virtex-5QV Heavy-Ion Weibull Fit Parameters for Static Tests

	Weibull Parameters			
Memory Type	**Limit, cm^2/bit**	**Onset, MeV-cm^2/mg**	**Width -**	**Power -**
BRAM	1.15×10^{-7}	0.01	200	0.86
User F/F's, Filter=OFF	2.80×10^{-8}	0.50	20	2.0
User F/F's, Filter=ON	2.76×10^{-9}	0.89	26	2.2
DSP, M register	5.5×10^{-6}	0.1	67	1.12
DSP, other registers	2.0×10^{-6}	0.1	35	1.25

Table 6. Virtex-5QV Proton Weibull Fit Parameters for Static Tests

	Weibull Parameters			
Memory Type	**Limit, cm^2/bit**	**Onset, MeV**	**Width -**	**Power -**
BRAM	4.7×10^{-14}	0.8	12	0.6
User F/F's, Filter=OFF	tbd $\times 10^{-15}$	tbd	tbd	tbd
User F/F's, Filter=ON	tbd $\times 10^{-15}$	tbd	tbd	tbd
DSP, M register	tbd $\times 10^{-15}$	tbd	tbd	tbd
DSP, other registers	tbd $\times 10^{-15}$	tbd	tbd	tbd

3.3.1 Block Memory

Normal incidence static heavy ion and proton cross section curves are given in the paper published last year [7] and reproduced in Figures 5 and 6.

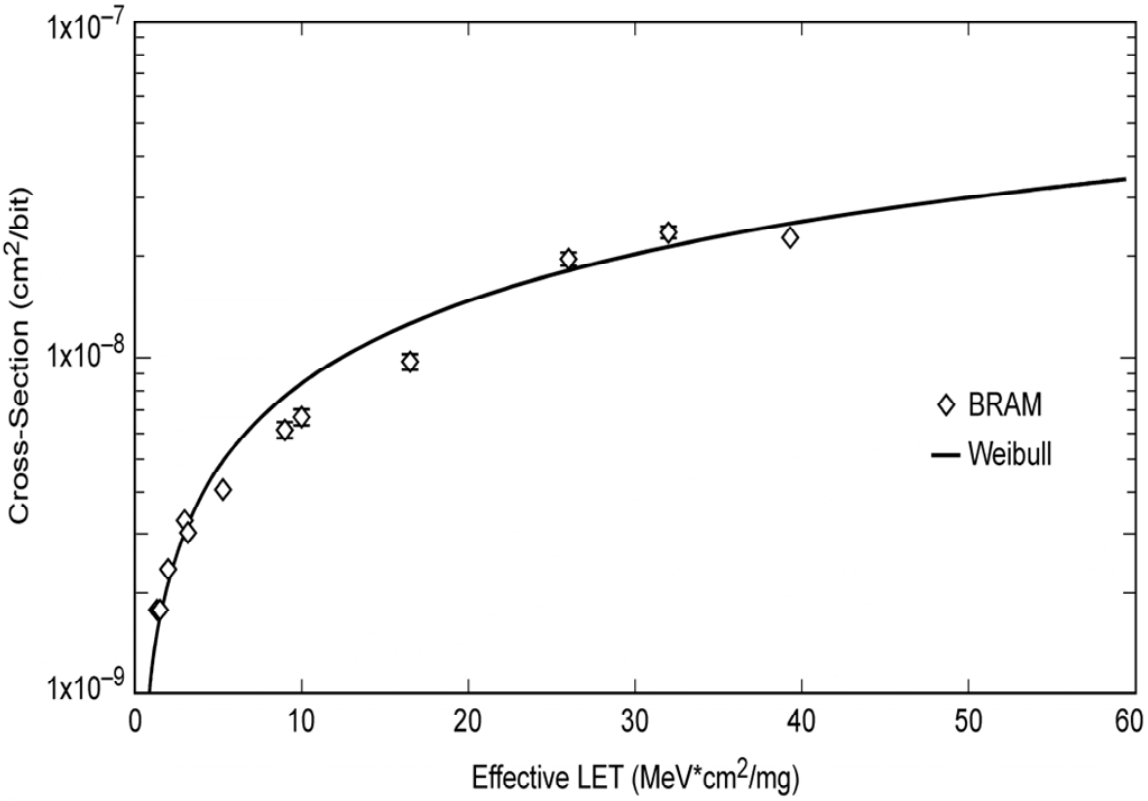

Figure 5. Virtex-5QV BRAM Susceptibility due to Heavy Ion Strikes

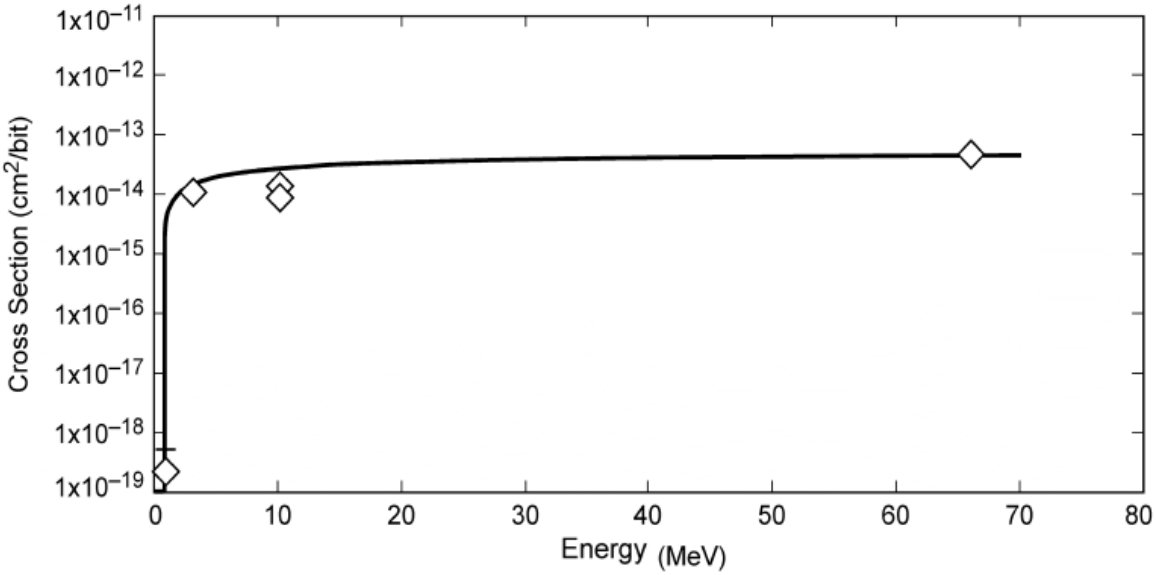

Figure 6. Virtex-5QV BRAM Susceptibility due to Proton Strikes

In July 2011 at TAM, an XRTC experiment under the direction of Munir Shoga using a variety DUT angles was undertaken. Analysis of this data should shed light on the

BRAM multiple-bit upset (MBU) susceptibility. Physical interleaving of the bits should make the error detection and correction circuitry robust to MBUs.

3.3.2 User Flip-Flops

Pseudo-static (1.5MHz) data and results are available thanks to George Madias and Eric Miller of Boeing and are summarized in this section. Because the flip-flops are implemented with master-slave dual-node cells, they are very hard to direct hit upset. Almost all of the upsets observed in the pseudo-static tests are the result of single-event transients on flip-flop inputs, one of: (1) a large enough SET on an asynchronous reset, (2) a clock transient coincident with inverse data line input, or (3) a data transient coincident with the clock edge. As a result, the measured upset susceptibility depends heavily on whether the input SET filters are turned on or not. Also, mainly due to #3, the results are frequency dependent; high speed measurements have been done, but those results are presented elsewhere.

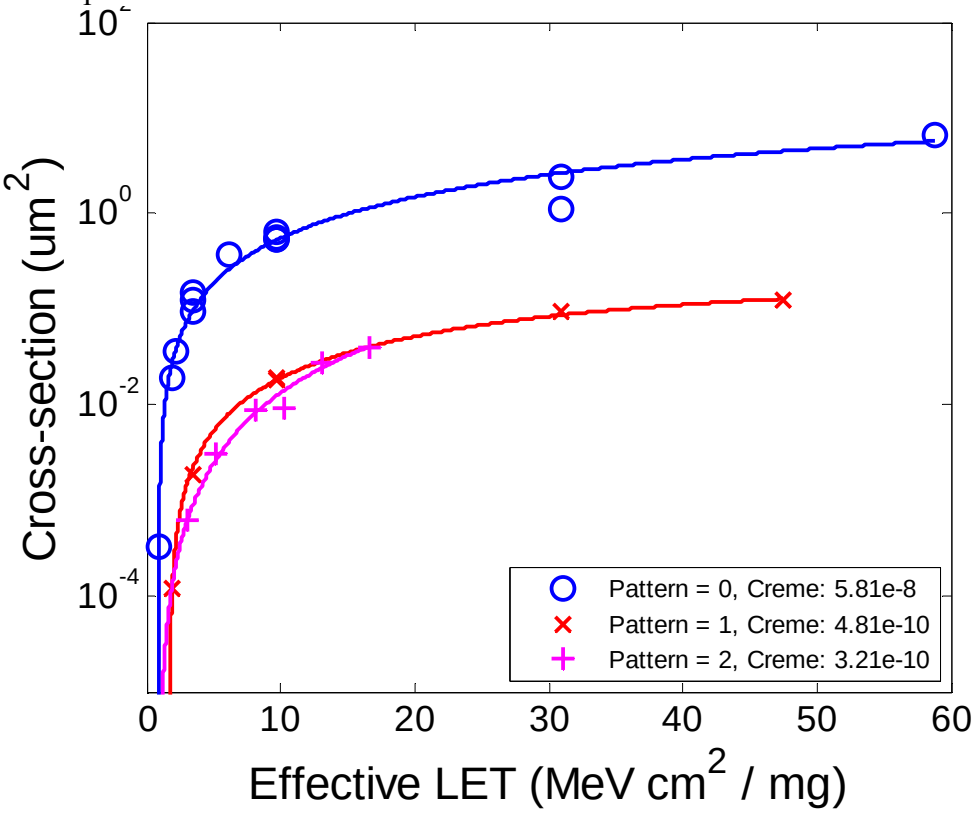

Figure 7. Virtex-5QV User Flip-Flop (with filters OFF) Susceptibility to Heavy Ions

Proton data collection for the pseudo-static case remains largely to be done as proton data collection so far has focused on higher speed testing where upsets susceptibilities are higher than the static case. These dynamic results are so low that static proton results (especially with the filters ON) will be only of extreme academic interest.

3.3.3 DSP Registers

A full report [9] on the XRTC static and dynamic testing of the Digital Signal Processing blocks (DSPs) of the Virtex-5QV by Roberto Monreal of SwRI includes detailed DSP SEU results. This section presents only a brief digest of the static results. Note that the full report calculates that static contribution to the overall space upset rate is only a fraction of the total measured dynamic cross section, about one third to one half depending on the particular op code tested. Extrapolating to higher speeds might lower the static contribution by as much as a factor of ten as high speed dynamic DSP testing remains to be done.

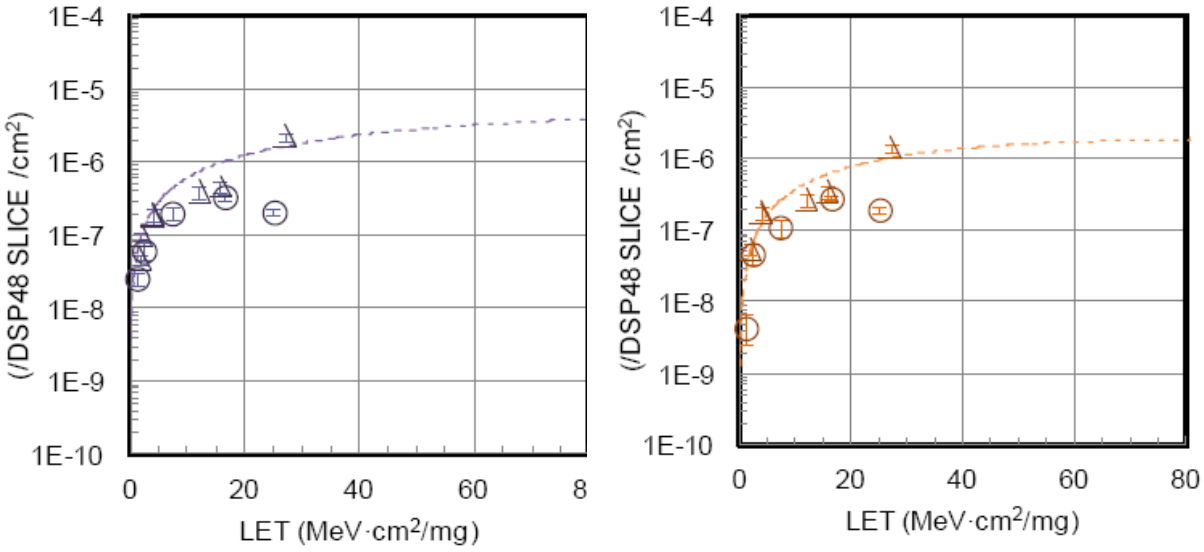

Figure 8. Virtex-5QV DSP Register(left= M, right=others) Susceptibility to Heavy Ions

The DSP registers all appear to have about the same static upset susceptibility except for the M register which is more susceptible so they are shown separately in Figure 8. Many upset events affect more than one bit in a given register so the cross sections in this digest are all per register. In practice, the bit error rate is of less importance than the register error rate because a calculation uses registers, not bits, as their fundamental granularity; thus, predicting the register upset rate is the way to predict the calculation error rate after folding whether a particular register is used in the calculation and its duty cycle.

Static proton data on the DSP registers has been taken and is currently awaiting analysis before inclusion here.

3.4 Orbital Rate Calculations

The CREME96 (Cosmic Ray Effects on Micro-Electronic Circuits) orbital event rate estimation model originally provided by the Naval Research Laboratories and now supported by Vanderbilt University [8] can be used to calculate orbital error rates based on the Weibull fits in the previous sections. Table 7 shows the input parameters for the CREME96 HUP and PUP files for calculating heavy ion and proton induced events, respectively. Although the SEFI data is measured in events per device, for modeling purposes, the bits per device used in CREME96 calculations are adjusted to give a relative per bit cross-section value more typical of a standard register. Even though most SEFI events are caused by logic gate transients, CREME96 models events as static upsets on a storage cell. The same is true for the configuration cells (CFGs); what's calculated here are transient-induced and while determining how many gates can generate those transients is theoretically needed, it is convenient - and doesn't change the calculation much anyway - to use the actual CFG count.

Table 7. CREME96 HUP and PUP Parameters for Static SEE Rate Calculation

CREME96 Input Parameters								
Device	**CFG***	**BRAM**	**User F/F**		**DSP M-Reg**	**DSP other**	**Intrusive SEFI**	**Units**
			f=OFF	**f=ON**				
FX130	30×10^6	10.9×10^6	81,920		320	1280	4	bits / device**
Sigma(HI)	1×10^{-8} ***	1.15×10^{-7}	2.80×10^{-8}	2.76×10^{-7}	5.5×10^{-6}	2.0×10^{-6}	2.0×10^{-7}	cm^2/bit
Sigma (P)	2.5×10^{-18}	4.7×10^{-14}	tbd	tbd	tbd	tbd	8.0×10^{-15}	
Proton (PUP)								
Onset	5	0.8	tbd	tbd	tbd	tbd	5	MeV
Width	50	12	tbd	tbd	tbd	tbd	20	w
Power	1	0.6	tbd	tbd	tbd	tbd	0.8	s
Limit	0.0000025	0.047	tbd	tbd	tbd	tbd	0.008	$cm^2/10^{-12}$
Heavy Ion (HUP)								
X & Y	1 ***	3.39	1.67	0.525	23.5	14.1	4.5	μ
Z	1 ***	1	1	1	1	1	1	μ
Onset	0.25 ***	0.01	0.5	0.89	0.1	0.1	0.7	$MeV/cm^2/mg$
Width	100 ***	200	20	26	67	35	60	w
Power	2.95 ***	0.86	2.0	2.2	1.12	1.25	1.65	s
Limit	1 ***	11.5	2.80	0.276	550	200	20	μ^2

* Not all configuration cells control design elements (so, in those, upsets can't make a design malfunction).
** For DSP registers (not bits): there are 320 of each type in a device and the sigma units are cm^2/register
*** "Equivalent" single-node Weibull for actual dual-node response when storing a one (worst case); see Section 4.4

Representative CREME96 orbital error rate estimates for several select orbits will be done for Quiet Solar Minimum conditions and assuming 100 mils aluminum-equivalent spacecraft shielding. All the rates make the conservative assumption that all bits are used; for more accuracy in a given application, scale these results by the fraction of the resources actually used.

4 CONFIGURATION (DUAL-NODE) RESULTS

The RHBD configuration cell used in the Virtex-5QV has internal redundancy so that, if any single node collects charge, it will not upset, although it is possible that there may be a brief transient on the cell output. Indeed, unless two nodes collect at least the minimum charges Q_{crit1} and Q_{crit2} , the cell will not upset. The pairs of nodes that can induce upset by simultaneously collecting charge are intentional spaced a good distance apart. This results in an upset susceptibility for a given ion that varies widely (a few orders of magnitude) depending on the ion's direction vector. The most sensitive direction has the ion vector aligned with the straight line between the two nodes.

4.1 Test Chip Static Results

Because the most sensitive direction goes through the pair of active nodes, the most sensitive angles of incidence are in the plane of the "top" of the silicon, i.e., grazing angles. Experimentally, this is a problem as the apparent thickness of any intervening dead layer increases rapidly (with the cosine of the angle) near those grazing angles. Available accelerator beams have limited penetration depth and, if the angle is too steep, will not reach the active silicon layer. Thus, two painful conclusions arise:

1. It is impossible to measure at the most important angles, and
2. Using a flip-chip device (even with aggressive backside thinning) exacerbates this problem.

Therefore, an experimental data set has been taken using a face-up test chip incorporating an array of the configuration cells. Sample plots of that extensive dataset are given on the following pages. The circles are the measured data points and the solid lines are the fit to the Edmonds dual-node physical model described briefly below in Sec. 4.4 and more extensively in Ref. 10.

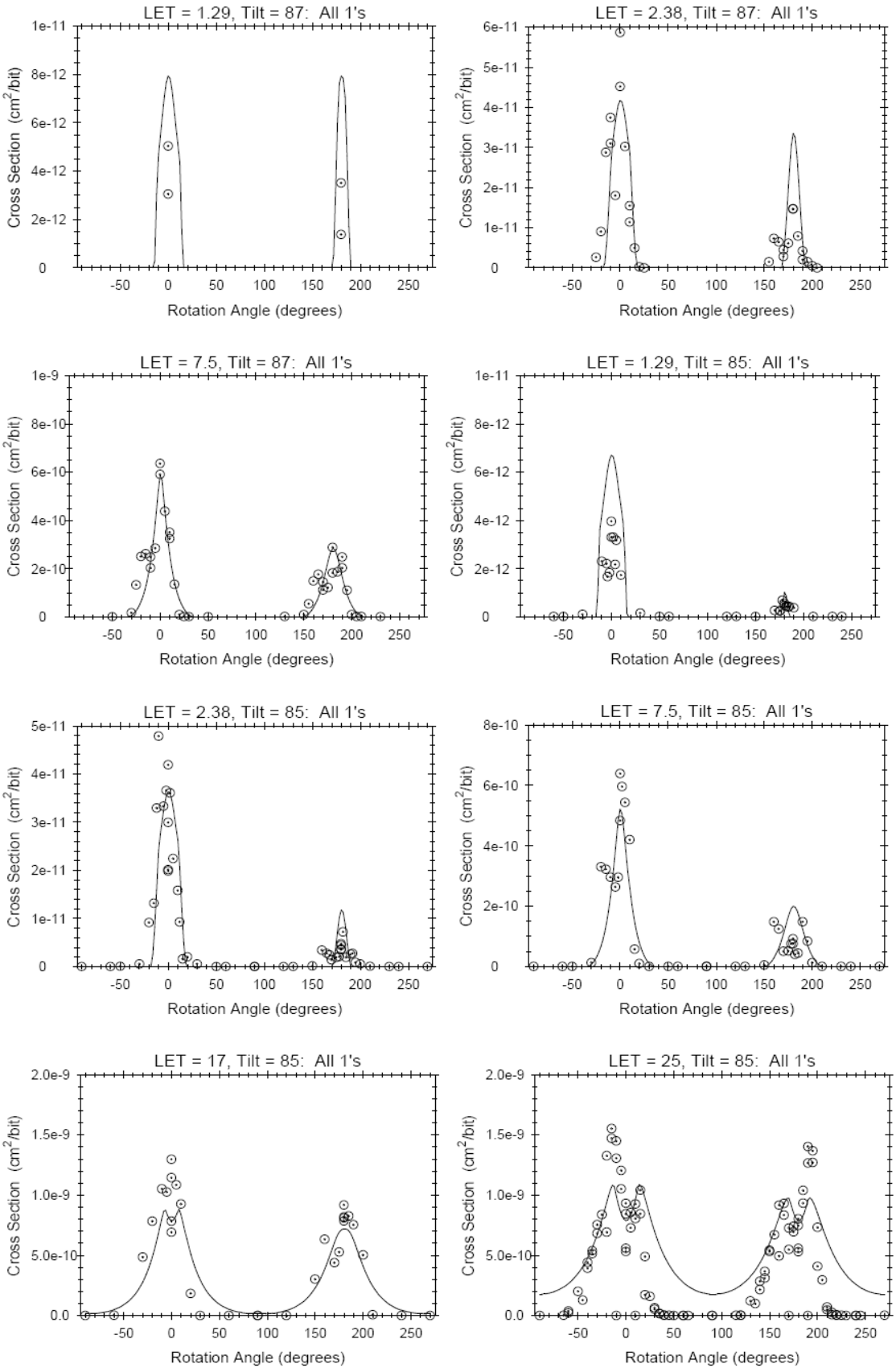

Fig. 9a. Rotation sweeps for dual-node the configuration cell storing ones [from Ref. 10, Fig. 23 pt 1]

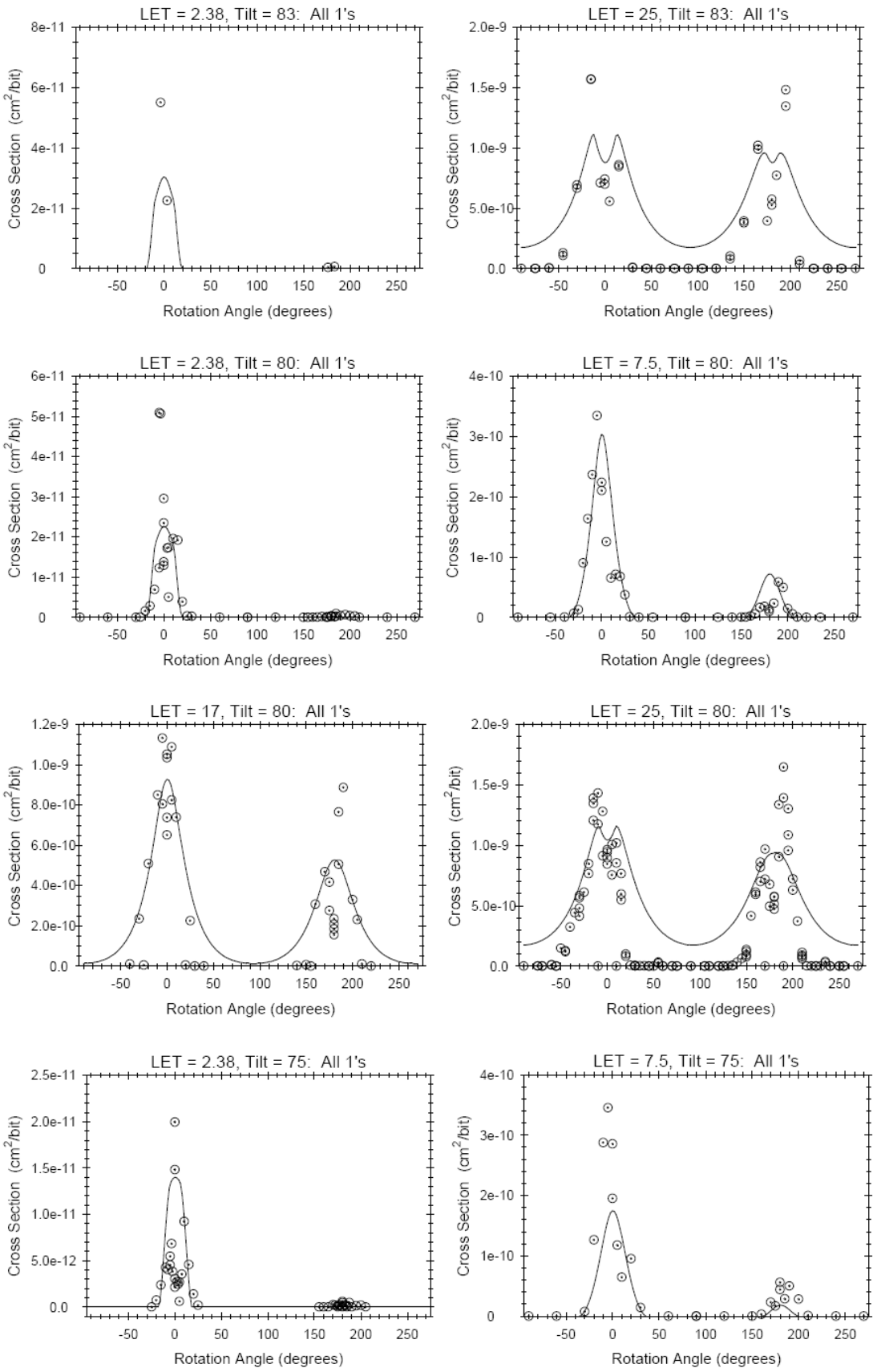

Fig. 9b. Rotation sweeps for dual-node the configuration cell storing ones [from Ref. 10, Fig. 23 pt 2]

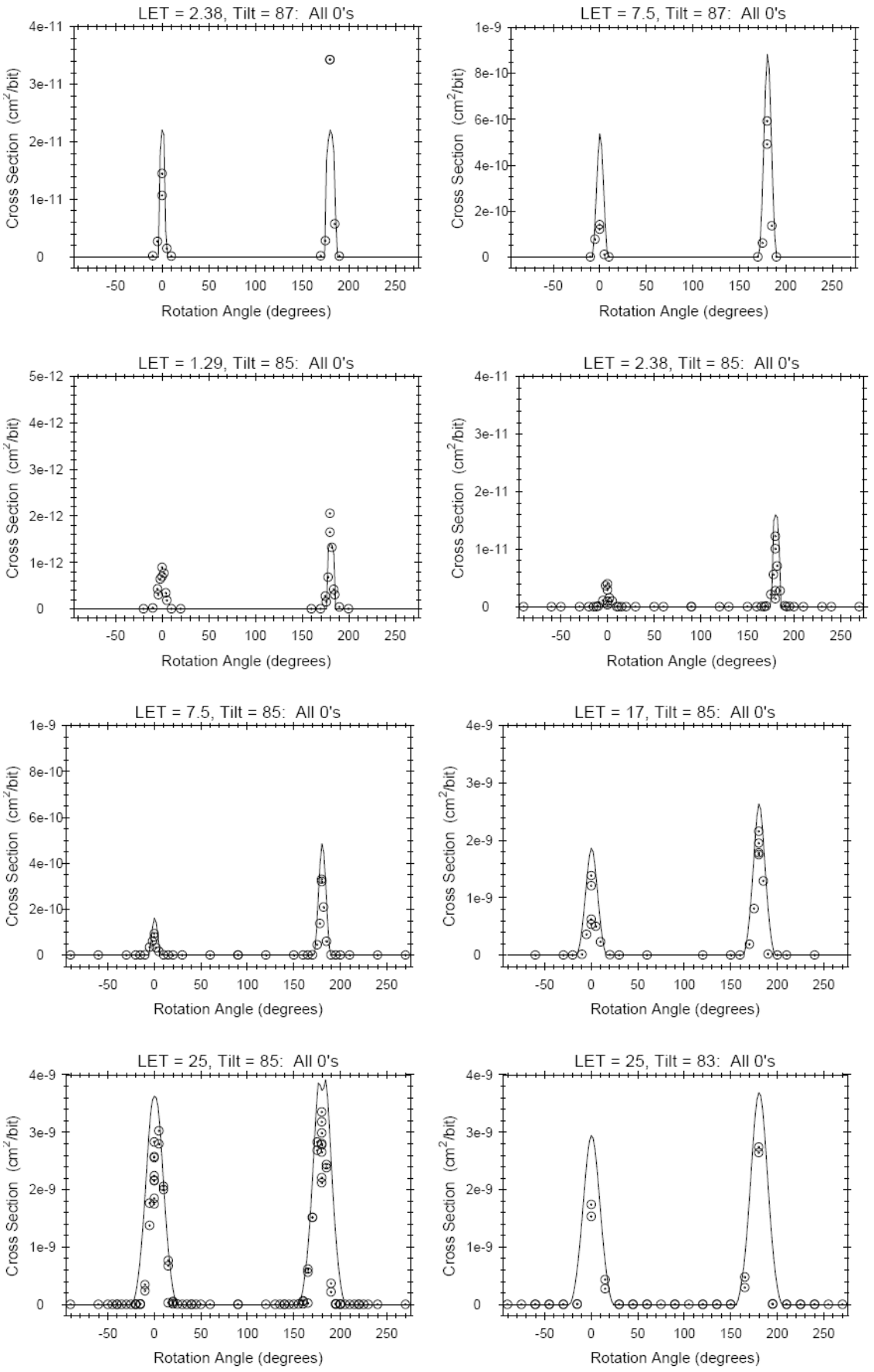

Fig. 10a. Rotation sweeps for dual-node the configuration cell storing zeros [from Ref.10, Fig.28 pt.1]

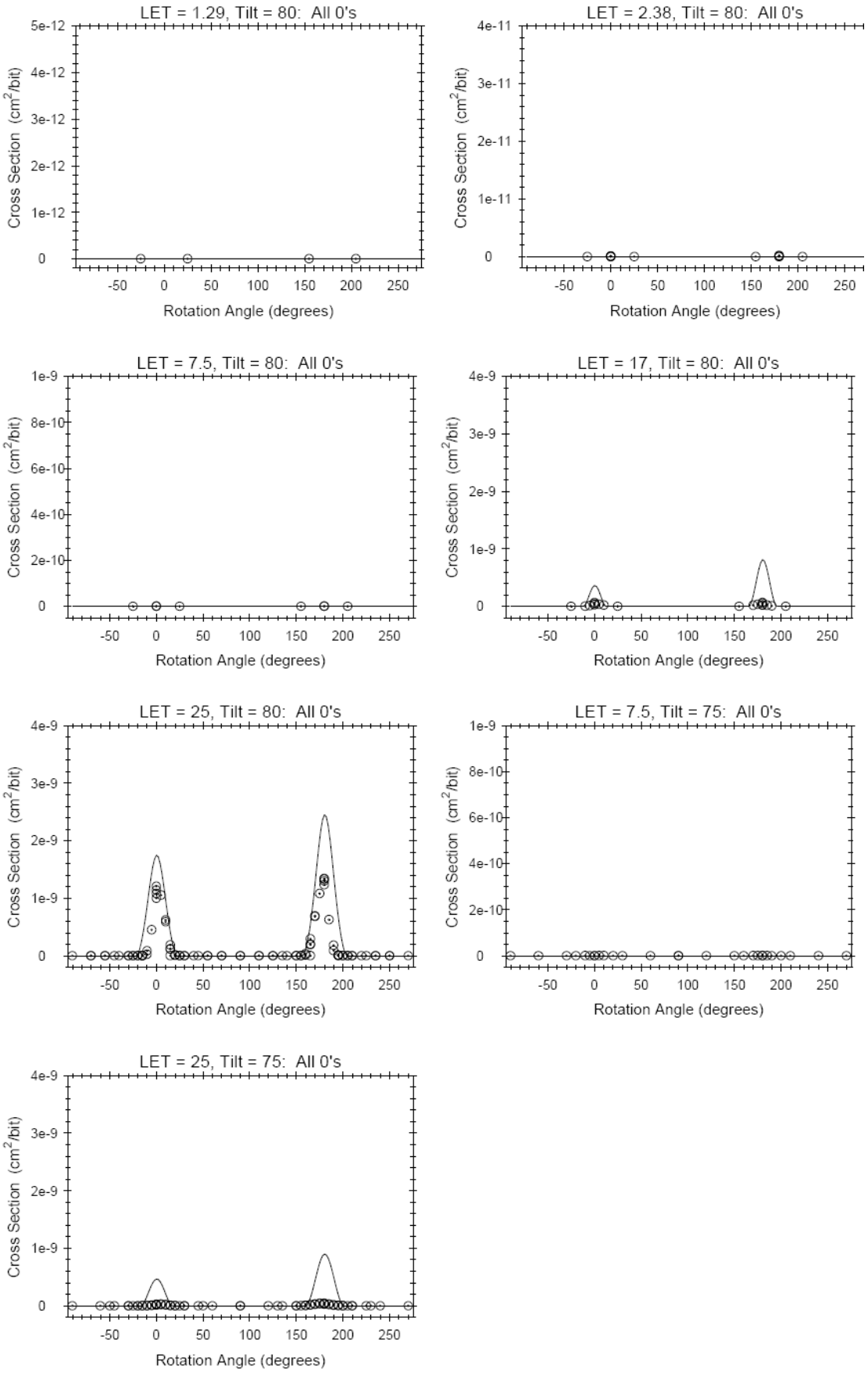

Fig. 10b. Rotation sweeps for dual-node the configuration cell storing zeros [from Ref.10, Fig.28 pt.2]

4.2 FPGA Direct-Upset Static Results

At shallower angles and using higher energy ions and/or lighter ions, it is possible to get upset data on the FPGA itself to compare to the test chip data. Testing was performed at the TAM cyclotron in July 2011 to obtain such data. Unfortunately, comparable test chip data with statistical significance for the low LET used has not yet been taken. The comparison is expected to yield only roughly similar results since the sensitivity of the measurements to slight variations in angle and/or LET is, of necessity and unfortunately, large.

In an investigation led by Munir Shoga and Gary Swift, the lower LETs of the steep angle dataset help rule out any significant contribution to direct ionization upsets from protons. For example, 40 MeV/amu N (with an incident LET calculated to be ~0.72 MeV-cm^2/mg) at 85 degrees in alignment with the dual nodes yielded a statistically significant number of upsets and a (non-effective) cross section of about $2x10^{-13}$ cm^2 per bit. Although a proton can directly deposit more than an LET of 0.7 as it slows down near the Bragg peak, it cannot do so to two nodes with any distance between them. Also note that the cross section is about as low as that obtained from proton-induced reactions in single-node devices; dual-node devices get an additional "geometrical" factor from having a narrow acceptance cone.

4.3 SET-triggered FPGA Results

Using upset-hardened-by-design techniques, it is possible to drive the direct upset rate down to such a low level that SET-triggered upsets dominate. In the static case, SETs coincident with a clock edge are ruled out, but SETs on asynchronous control lines (say reset or write signals) or on the clock lines themselves can cause an upset.

Two main categories of SET-triggered upsets of the dual-node configuration cells have been observed:

1. triggered events in "capture" cells, and
2. unintended "writes" to configuration cells.

Category 1 cells are not truly configuration cells in that they don't control or route anything; as a result, whether they are upset or not is irrelevant to correct design operation. However, upsets will add to the "false alarm" rate for detection schemes because Category 1 bits do appear in the readback bitstream.

On the other hand, category 2 upsets may break a design and so definitely add to the static cross section of the FPGA a component that adds to what was seen on the test chip.

Real-time sorting and masking capabilities of the Configuration Monitor allows the XRTC test apparatus to collect data on both these SET-induced upset types simultaneously with any other testing of the Virtex-5QV. More than 100 hours of testing in the July and October 2011 TAM campaigns yielded heavy ion data for defining these cross section vs LET curves, but the analysis is still proceeding. Similarly, proton data has been collected in the November 2011 and January and June 2012 UC-Davis tests. The expectation is that the responses will be the standard single-node type and, thus, can be fit with Weibull curves that can be fed into CRÈME. The analysis is a bit painful, but

the result for the category 2 upsets for LET=88.7 (normal incident gold ions) is encouraging. The event cross sections are $4x10^{-11}$ and $7x10^{-12}$ cm^2 for ones and zeros, respectively. Thus, it likely that they will be overshadowed by the direct upset rate which is less than 5 per year in GEO (see the next section).

A detailed manual analysis of effective LET=145 (gold at 55 degrees) shows event cross section for category 2 climbs about a factor of six to $2.4x10^{-10}$ cm^2/bit. For the whole device, the category 1 (capture bits) event cross section is pretty close at 8.3 $x10^{-3}$ cm^2/device, but a much bigger per bit cross section as there are less than 200,000 capture bits, but over 30,000,000 'real' configuration bits. Interestingly, for both categories (and in the absence of the huge capture bit 'clobbers' of thousands of bits), the cells storing zero rarely show events with more than one upset while cells storing one have an average event size of three to five. For category 2 upsets (inadvertent writes), this is likely the result of the predominance of zeros; zero is much more likely to be the value on the bus when an SET induced write event happens and, in that case, stored ones are much more likely to be upset. Under this explanation, writing a zero into a cell storing zero is, by far, the most likely event happening, but, of course, that event looks exactly like no event. Note that another implication of this explanation is that there is a design dependent component to the experimental results: the ratio of ones to zeros in the configuration matters. For this data point, the "heater" design used for latchup testing was the design-under-test.

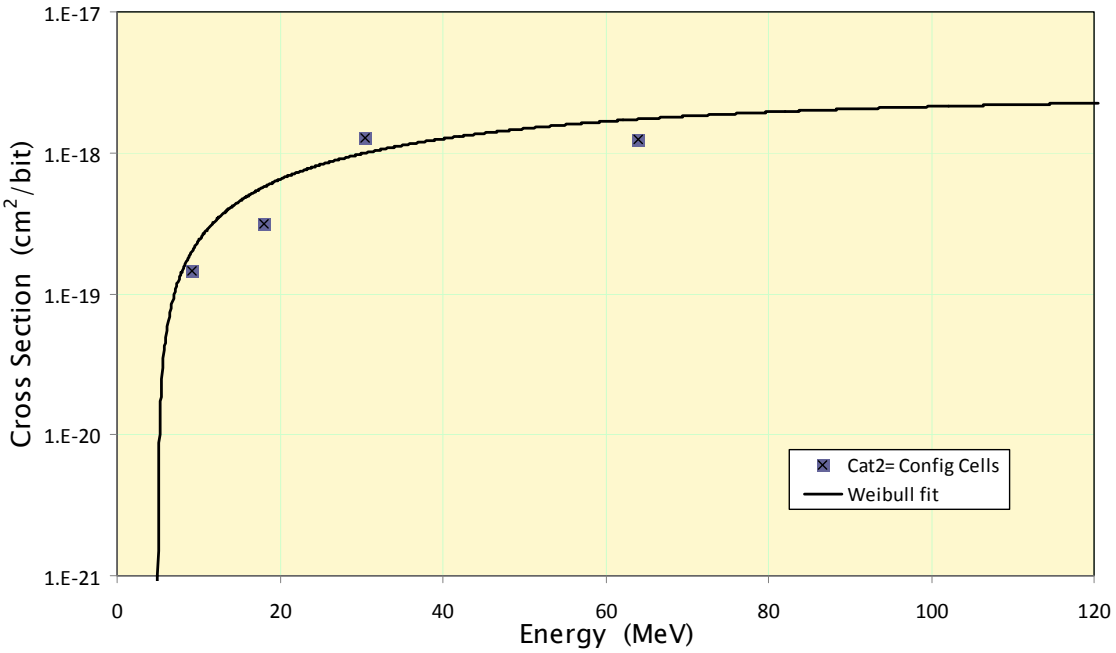

Figure 11. Virtex-5QV Configuration Bit Upset Susceptibility due to Protons

Preliminary proton results and Weibull fit for category 2 errors are shown in Figure 11. These results are extracted from the data taken at UC-Davis in November 2011 and January and June 2012 and are 'raw' results as upset rates and event rates are not yet extracted. This is not too important as it appears the event rate will not be substantially lower than the upset rate except perhaps for cells storing ones. The device cross sections

for category 1 upsets is more than an order of magnitude larger even though the number of bits is over two orders of magnitude smaller. To reiterate, category 2 upsets are not important in the sense that they do not affect design operation.

4.4 Orbital Rate Calculations

There is no industry-accepted model of how to turn a set of dual-node susceptibility measurements over angles into rate predictions for particular space radiation environments. Larry Edmonds of JPL has considered this problem for a long time and has developed a physical model (albeit with ten fitting parameters) to overcome the necessary extrapolation problem. He has written a formal JPL report [10] that contains the model's derivation and its application to the Virtex-5QV test chip data set. He concludes that the solar minimum GEO rate behind 100 mils of Al-equivalent shielding is 2.1×10^{-10} and 5.3×10^{-11} upsets per bit-day for ones and zeros, respectively.

Interestingly, he also obtains equivalent single-node Weibull parameters that give approximately the same answer for the same environment and he does recommend using these to estimate the rates in other space environments. This is basically averaging a very peaked angular distribution over all directions so that an equivalent device, but with an isotropic response, is used for projecting rates. This approach works because space rate calculators assume the environments are directionally homogeneous. The parameters are given in Table 8. They give 1.6×10^{-10} and 4.2×10^{-11}.or about 25% lower than the answers from the full model.

Table 8. Virtex-5QV Heavy-Ion Weibull Fit Parameters for an Equivalently Hard Single-Node Configuration Cell

	Weibull Parameters			
Cells	**Limit, cm^2/bit**	**Onset, MeV-cm^2/mg**	**Width -**	**Power -**
storing "ones"	3.1×10^{-9}	0.20	61	2.55
storing "zeros"	8.0×10^{-9}	0.25	103	2.95

5 CONCLUSION

The Virtex-5QV, a megarad(Si) RHBD SRAM-based reconfigurable FPGA designed for space, performed well in these heavy-ion and proton irradiations, exhibiting no single-event latchup (SEL) even at elevated temperature and spec-max voltages to effective LETs above 130 MeV cm^2/mg and fluence above 10^8 per cm^2.. The XQR5VFX130 exhibited extremely low total SEFI susceptibility to heavy ions and protons with a resulting rate of approximately one per 10,000 years in the geosynchronous orbit's (GEO) radiation environment. Upsets of the unhardened Block RAMs might be a significant concern based on these data; however, the enhanced ECC capabilities built into the FPGA are more than sufficient to maintain error-free design operation; in-beam testing has proven their effectiveness [7]. The projected configuration upset rates (a few bits per year in GEO) are likely acceptable for most applications; based on a fairly conservative architectural vulnerability factor (AVF) of 10x, an actual error (circuit malfunction) is expected to occur less than about once every two years of on-orbit operation on average. The most critical applications can use selective TMR to operate error-free in spite of the presence of an upset. Employing design-level mitigation reduces the system error rate due to upsets to well below that of the SEFI rate for even the worst-case space environments.

6 FUTURE WORK

Work continues on analyzing recent proton data for user flip-flops and DSP registers. In addition, interesting data on BRAM heavy-ion upset response at increasing tilt angles and resulting multiple bit upsets (MBUs) has been taken. Finally, the most important remaining analyses, for both protons and heavy ions, are aimed at a fuller understanding of the configuration cells' static upsets in the FPGA, as opposed to the test chip array, where transients causing writes cause most of the upsets at normal and near-normal incidence. These analyses are complicated by the need to separate out non-configuration bit upsets due to transients on their capture triggers; although these are only a small fraction of total bits and they don't affect functionality, they dominate the raw upsets seen in the readback stream.

7 REFERENCES

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[10] L. D. Edmonds, *Estimates of SEU Rates from Heavy Ions in Devices Exhibiting Dual-Node Susceptibility*, JPL Publication 11-6, June 2011, http://parts.jpl.nasa.gov/wp-content/uploads/Dual-Node-JPL-pub1.pdf

8 APPENDIX

The single-node, heavy-ion SEU response data sets have been fit with Weibull curves to facilitate orbital rate calculations. The fitting equation is:

$$\sigma(LET) = \sigma_{sat}(1 - \exp\{-[(LET - L_{th})/W]^S\})$$

σ_{sat} is the limiting or plateau cross section (or "limit"),

L_{th} is the LET threshold parameter (or so called "onset"),

W is the width parameter, and

S is a dimensionless exponent dubbed "power."